Application Note

Configuring TX73L64 into a 32-channel, 2A Drive Ultrasound Transmitter

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ABSTRACT

The TX73L64 is one of the latest generation ultrasound products from Texas Instruments. The device integrates a total of 64 three-level pulser circuits, with 1A drive current per channel. The device also integrates 32-LNAs with a 2:1 multiplexing from the transmit side to the receiver. The TX73L64 is used in conjunction with AFE5932/AFE59D32, mainly intended for portable ultrasound systems that require a ratio of 2:1 transmit to receive channels.

However, certain systems and applications require a current drive of more than 1A per channel or a 1:1 transmit to receive channel connections, can be even both. For such systems, the TX73L64, in the default configuration, is not the right choice of Tx design. This application note explores how TX73L64 can be configured into a 32-channel, 2A drive design and describes the required register settings and system level connections for use in ultrasound systems that require a 1:1 multiplexing between Tx and Rx with a higher current drive of 2A.

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Trademarks

1 Introduction

The TX73L64 is a highly integrated, 64-ch, 3-Level Pulser with an integrated T/R Switch. The device supports a current drive of 1A for each channel. Figure 1-1 shows the output stage of the TX73L64 Pulser. As shown, the TX73L64 has a 3-level Pulser with a single set of HV supply, namely AVDDP_HV and AVDDM_HV. Each transistor/level has a maximum current drive of 1A and the device is designed to operate for a range of HV Supplies from 1.5V to 100V.

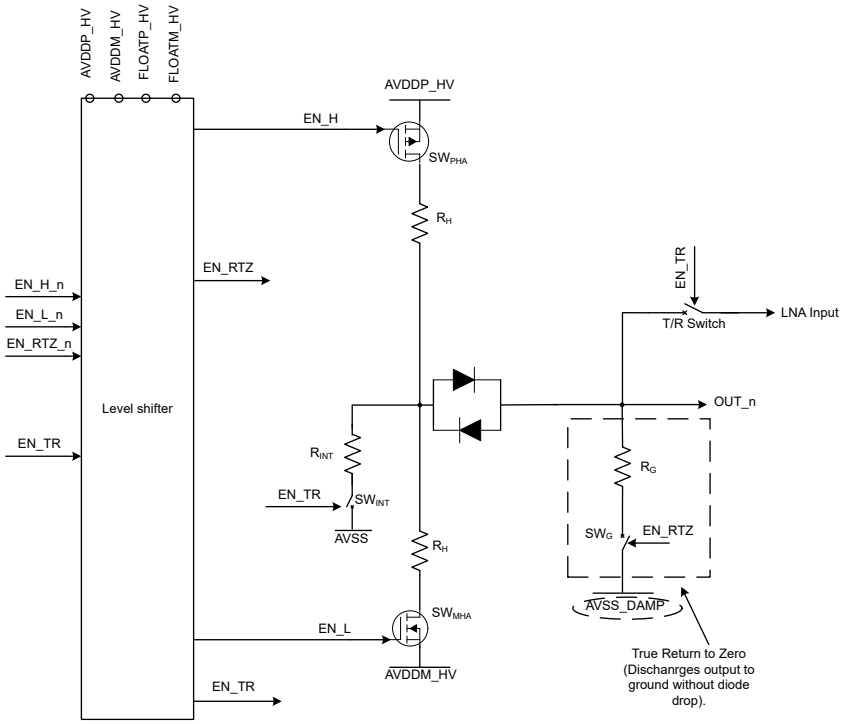

Figure 1-1. Output Stage of the Pulser

On the receiver side, the device incorporates 64 T/R Switches, one for each channel, and 32 LNAs. The T/R Switches are configuring into a 2:1 multiplexing mode, connecting two TX channels to one LNA as shown in Figure 1-2. Out of the two channels, only 1 TX channel can be connected to the LNA at any instant of time.

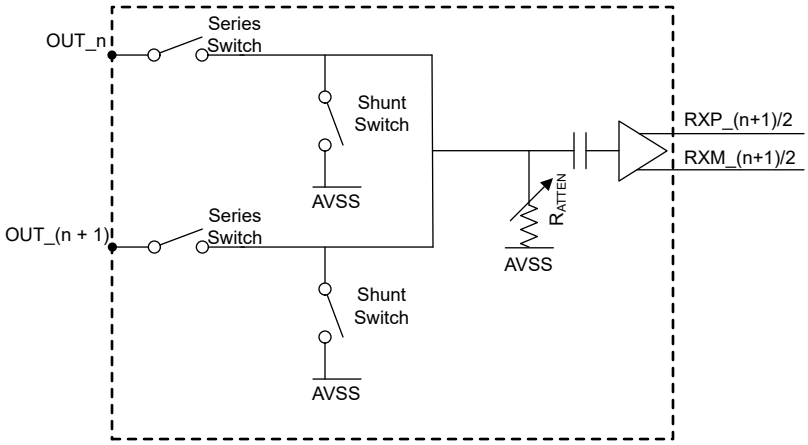

Figure 1-2. Receiver Side 2:1 Multiplexing

2 Register Setting for 32-Channel, 2A Drive Mode

Table 2-1 provides the register settings to configure the device into a 32-channel transmitter with 2A current drive per channel.

Table 2-1. Register Configuration for 32-Ch, 2A-Drive Mode

Address (Decimal)	Data (Hex)	Comment
2	0x8000_0000	Page Select operation
148	0xC	Internal Register Setting
2	0x0	Page Select operation

The register setting in Table 2-1 can be made part of the initialization sequence to be written to the device post Hardware Reset assertion.

3 System Level Connections Under the New Configuration

After the register settings provided in Section 2 are written, the device effectively has 32-channels on the transmit side and 32-LNAs on the receiver side, forming a 1:1 connection between Tx and Rx.

Under this new configuration, transmit channels *2n-1* and *2n* (n=1 to 32) behave the same way and are treated as a single channel. The Pulser and T/R Switch circuits of these channels have common control under the new configuration and cannot be independently controlled as both channels are shorted together on the PCB to behave as a single channel. The register controls are explained in detail in Section 5. Therefore, these channels can be shorted close to the device and connected to a single transducer element. Table 3-1 provides the system level connections between the transducer, TX73L64 and the AFE under the new configuration.

Table 3-1. System Level Connections between the Transducer, Tx and AFE

Transducer Element	TXL64 Channel Number	New TX Channel Number	LNA Channel Number	AFE Channel Number	Comment
1	1,2	1	RXP/M_1	AFE Channel 1	Short older Tx chs 1 and 2 and name it ch 1
2	3,4	2	RXP/M_2	AFE Channel 2	Short older Tx chs 3 and 4 and name it ch 2
3	5,6	3	RXP/M_3	AFE Channel 3	Short older Tx chs 5 and 6 and name it ch 3
4	7,8	4	RXP/M_4	AFE Channel 4	Short older Tx chs 7 and 8 and name it ch 4
5	9,10	5	RXP/M_5	AFE Channel 5	Short older Tx chs 9 and 10 and name it ch 5
6	11,12	6	RXP/M_6	AFE Channel 6	Short older Tx chs 11 and 12 and name it ch 6
7	13,14	7	RXP/M_7	AFE Channel 7	Short older Tx chs 13 and 14 and name it ch 7
8	15,16	8	RXP/M_8	AFE Channel 8	Short older Tx chs 15 and 16 and name it ch 8
9	17,18	9	RXP/M_9	AFE Channel 9	Short older Tx chs 17 and 18 and name it ch 9
10	19,20	10	RXP/M_10	AFE Channel 10	Short older Tx chs 19 and 20 and name it ch 10
11	21,22	11	RXP/M_11	AFE Channel 11	Short older Tx chs 21 and 22 and name it ch 11
12	23,24	12	RXP/M_12	AFE Channel 12	Short older Tx chs 23 and 24 and name it ch 12
13	25,26	13	RXP/M_13	AFE Channel 13	Short older Tx chs 25 and 26 and name it ch 13
14	27,28	14	RXP/M_14	AFE Channel 14	Short older Tx chs 27 and 28 and name it ch 14

Table 3-1. System Level Connections between the Transducer, Tx and AFE (continued)

Transducer Element	TXL64 Channel Number	New TX Channel Number	LNA Channel Number	AFE Channel Number	Comment
15	29,30	15	RXP/M_15	AFE Channel 15	Short older Tx chs 29 and 30 and name it ch 15
16	31,32	16	RXP/M_16	AFE Channel 16	Short older Tx chs 31 and 32 and name it ch 16
17	33,34	17	RXP/M_17	AFE Channel 17	Short older Tx chs 33 and 34 and name it ch 17
18	35,36	18	RXP/M_18	AFE Channel 18	Short older Tx chs 35 and 36 and name it ch 18
19	37,38	19	RXP/M_19	AFE Channel 19	Short older Tx chs 37 and 38 and name it ch 19
20	39,40	20	RXP/M_20	AFE Channel 20	Short older Tx chs 39 and 40 and name it ch 20
21	41,42	21	RXP/M_21	AFE Channel 21	Short older Tx chs 41 and 42 and name it ch 21
22	43,44	22	RXP/M_22	AFE Channel 22	Short older Tx chs 43 and 44 and name it ch 22
23	45,46	23	RXP/M_23	AFE Channel 23	Short older Tx chs 45 and 46 and name it ch 23
24	47,48	24	RXP/M_24	AFE Channel 24	Short older Tx chs 47 and 48 and name it ch 24
25	49,50	25	RXP/M_25	AFE Channel 25	Short older Tx chs 49 and 50 and name it ch 25
26	51,52	26	RXP/M_26	AFE Channel 26	Short older Tx chs 51 and 52 and name it ch 26
27	53,54	27	RXP/M_27	AFE Channel 27	Short older Tx chs 53 and 54 and name it ch 27
28	55,56	28	RXP/M_28	AFE Channel 28	Short older Tx chs 55 and 56 and name it ch 28
29	57,58	29	RXP/M_29	AFE Channel 29	Short older Tx chs 57 and 58 and name it ch 29
30	59,60	30	RXP/M_30	AFE Channel 30	Short older Tx chs 59 and 60 and name it ch 30
31	61,62	31	RXP/M_31	AFE Channel 31	Short older Tx chs 61 and 62 and name it ch 31
32	63,64	32	RXP/M_32	AFE Channel 32	Short older Tx chs 63 and 64 and name it ch 32

4 Memory Map in New Configuration

There is a total of 16 memory blocks in the device. Table 4-1 provides the default memory configuration of the device for memory block 'N' (N=1 to 16).

Table 4-1. Memory Block N (N can have any value from 1 to 16)

Address <8:0>	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]	Remarks
0	TR_SW_ON_DEL of Channel 2N + 31	TR_SW_OFF_DEL of Channel 2N + 31	TR_SW_ON_DEL of Channel 2N - 1	TR_SW_OFF_DEL of Channel 2N - 1	The first address of the memory has the T/R Switch OFF and ON delay information of channels 2 N + 31 and 2N - 1. This address is hard-coded and so does not have any memory pointer associated with the address
1	TR_SW_ON_DEL of Channel 2N + 32	TR_SW_OFF_DEL of Channel 2N + 32	TR_SW_ON_DEL of Channel 2N	TR_SW_OFF_DEL of Channel 2N	The second address of the memory has the T/R Switch OFF and ON delay information of channels 2N and 2N + 32. This address is hard-coded and so does not have any memory pointer associated with the address
Address <8:0>	**Data <31:16>**		**Data<15:0>**		**Remarks**
…					
K	Channel Delay of Channel 2N + 31		Channel Delay of Channel 2N - 1		Delay Profile 0. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 2 to 510 and made to be an even number)
K+1	Channel Delay of Channel 2N + 32		Channel Delay of Channel 2N		
K+2	Channel Delay of Channel 2N + 31		Channel Delay of Channel 2N - 1		Delay Profile 1. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 2 to 510 and has even number)
K+3	Channel Delay of Channel 2N + 32		Channel Delay of Channel 2N		
…					
Pattern Start Address (M0)	Pattern profile 0 starts here				Pattern Profile 0 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that the number is odd)
M0+1					
…					
Pattern End Address (M0+L0)	Pattern profile 0 ends here				
…					
Pattern Start Address (M1)	Pattern profile 1 starts here				Pattern Profile 1 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that the number is odd)
M1+1					
…					
Pattern End Address (M1+L1)	Pattern profile 1 ends here				
…					
511					

As seen from the table, each memory block contains information for a group of 4 channels. However, under the new configuration, the device effectively has 32 channels, therefore, each memory block contains information for group of 2 channels. The memory map of the device under new configuration is provided in Table 4-2.

Table 4-2. Memory Block N (N can have any value from 1 to 16)

Address <8:0>	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]	Remarks
0	TR_SW_ON_DEL of Channel N+16	TR_SW_OFF_DEL of Channel N+16	TR_SW_ON_DEL of Channel N	TR_SW_OFF_DEL of Channel N	The first address of the memory should always have the T/R Switch OFF and ON delay information of channels N and N+16. This address is hard-coded and does not have any memory pointer associated with it.
Address <8:0>	**Data <31:16>**		**Data<15:0>**		**Remarks**
…					
K	Channel Delay of Channel N+16		Channel Delay of Channel N		Delay Profile 0. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 1 to 511)
K+1	Channel Delay of Channel N+16		Channel Delay of Channel N		Delay Profile 1. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 1 to 511)
K+2	Channel Delay of Channel N+16		Channel Delay of Channel N		Delay Profile 2. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 1 to 511)
K+3	Channel Delay of Channel N+16		Channel Delay of Channel N		Delay Profile 3. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 1 to 511)
…					
Pattern Start Address (M0)	Pattern profile 0 starts here				Pattern Profile 0 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that it should be a odd number)
M0+1					
…					
Pattern End Address (M0+L0)	Pattern profile 0 ends here				
…					
Pattern Start Address (M1)	Pattern profile 1 starts here				Pattern Profile 1 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that it should be a odd number)
M1+1					
…					
PatternEnd Address (M1+L1)	Pattern profile 1 ends here				
…					
511					

5 Register Map under New Configuration

Under the new configuration, the register controls behave slightly differently as compared to the original functionality in the default configuration. Table 5-1 lists the register fields of TX73L64 that cannot be used in the new configuration, while Table 5-2 lists the register fields whose functionality is modified under the new configuration.

Table 5-1. Registers Not Required in New Configuration

Register Address (Hex)	Register Field Name	Comment
0x16	TR_SW_EN_n (n = 2, 4, 6…64)	These are the TR_SW_EN bits of even channels of the device which do not have to be used under the new configuration
0x1B	EN_AUTO_DIS_RX, TR_SW_MUX_EN_1, TR_SW_MUX_EN_2	These control the T/R Switch multiplexing in TX73L64 which do not have to be used under the new configuration.
0x2D	PDN_PUL_n (n = 2, 4, 6…64)	These are the PDN_PUL bits of even channels of the device which do not have to be used under the new configuration
0x2F	PAT_INV_CH_n (n = 2, 4, 6…64)	These are the PAT_INV_CH bits of even channels of the device which do not have to be used under the new configuration

Table 5-2. Registers whose Functionality is Modified in New Configuration

Register Address (Hex)	Register Field Name	Comment
0x17	TR_SW_EN_n (n = 1, 3, 5…63)	These are the TR_SW_EN bits of odd channels of the device. The TR_SW_EN_n bit controls both channel ‘n’ & ‘n+1’ (n = 1, 3, 5…63).
0x18	TR_SW_DIS_n (n = 2, 4, 6…64)	The value written in Register 0x18 & 0x19 must match each other. Different values can lead to improper device function.
0x19	TR_SW_DIS_n (n = 1, 3, 5…63)	The value written in Register 0x18 & 0x19 must match each other. Different values can lead to improper device function.
0x2E	PDN_PUL_n (n = 1, 3, 5…63)	These are the PDN_PUL bits of odd channels of the device. The PDN_PUL_n bit controls both channel ‘n’ & ‘n+1’ (n = 1, 3, 5…63).
0x30	PAT_INV_CH_n (n = 1, 3, 5…63)	These are the PAT_INV_CH bits of odd channels of the device. The PAT_INV_CH_n bit controls both channel ‘n’ & ‘n+1’ (n = 1, 3, 5…63).

The fields that are not used (mentioned in Table 5-1) must be kept to ‘0’ while using the device under the new configuration.

6 Output Waveform in New Configuration

Figure 6-1 shows the Pulser output for a 5MHz, 5-cycle waveform in default configuration and new configuration. The load used is 220 || 220pF.

In the default configuration, a single channel is connected to the load, while in new configuration, two pulser channels are shorted and connected to the load.

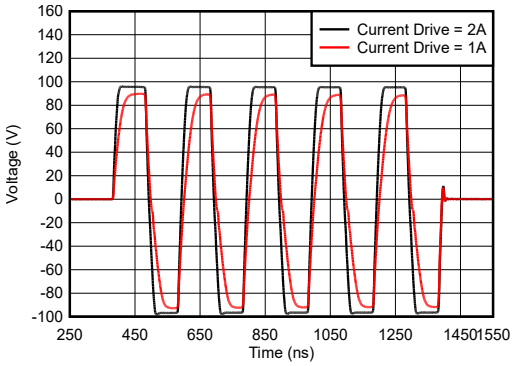

Figure 6-1. Time Domain Waveform of 5MHz Signal in 1A Drive and 2A Drive Mode

Note

Failing to write the register settings in Section 2 allows the device to operate as a 64-ch part which can lead to unexpected behavior/device damage if 2-channels are shorted in the hardware for 32-channel configuration.

7 Summary

This application note introduces TX73L64, a 64-channel, 3-level, 1A drive transmitter with a 2:1 T/R Switch multiplexing. The app note goes on to show how the device can be configured into a 32-channel, 2A drive transmitter for those applications which require a higher current drive and a 1:1 multiplexing from transmit to receive side. The application note describes the register setting required for the 32-channel, 2A drive configuration as well as explains the system level connections required to operate in the new configuration. Finally, the application note summarizes the user control difference between the default configuration and the new configuration to operate the device as a 32-channel, 2A drive transmitter with a 1:1 multiplexing from Tx to Rx side.

8 References

- Texas Instruments, *TX73L64 3-Level, 64-Channel Transmitter with On-Chip Beamformer, T/R Switch, 32-Channel Multiplexed Receivers with LNA*, datasheet.

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