Application Note

TDP20MB421 Schematic Checklist

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ABSTRACT

This schematic checklist provides a brief explanation of each TDP20MB421 device pin and the recommended configuration of TDP20MB421 device pins for default operation. The TDP20MB421 is a DisplayPort™ (DP) linear redriver with an integrated 2:1 MUX. The device complies with the VESA DisplayPort standard Version 1.4, 2.0, and 2.1; and supports a 1-4 lane Main Link interface signaling up to UHBR20 (20Gbps per lane). Additionally, this device is position independent. The TDP20MB421 can be placed inside source, cable, or sink, effectively providing a negative loss component to the overall link budget. The TDP20MB421 has the ability to be configured via GPIO or the SMBus/I2C bus. This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the TDP20MB421 DisplayPort 2.1 24Gbps 4-Channel Linear Redriver with 2:1 MUX, and associated documents to gain a full understanding of device functionality.

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Trademarks

1 Introduction

This document includes the functionality, provides a recommendation and additional considerations for each pin of the TDP20MB421. This data is encapsulated in Table 2-1.

2 TDP20MB421 Schematic Checklist

Pin Name	Pin Numbers	Pin Description	Recommendation	Additional Pin Considerations
Main Link Input Pins				
RX[0:3] P/N	37,38,33,34,28,29,24,25, 35,36,31,32,26,27,22,23	DisplayPort main link differential input	AC-coupled connection from GPU to the TDP20MB421	In the case of a DP receptacle being connected to the TDP20MB421 input, the AC-coupling capacitor may already be populated on the GPU side. If so, then the TDP20MB421 input can be DC-coupled. If the TDP20MB421 input still needs to be AC-coupled, use 0.22uF size 201 capacitors
Main Link Output Pins				
TX[0:3] P/N	4,3,8,7,11,10,15,14	DisplayPort main link differential output	0.22uF size 201 capacitor coupled connection from the TDP2004 to the sink or the DP receptacle	
Control Pins				
PD	18	2-level logic controlling the operating state of the TDP20MB421. Active in all device control modes. The pin has internal 1MΩ weak pull-down resistor.	Leave floating or pull to GND through a 1kΩ resistor	
MODE	41	Selects between configuration modes: L0: Pin-strap mode L1 or L2: SMBus/ I2C secondary mode	Tie 1kΩ to ground for pin strap mode Tie 8.25kΩ or 24.9kΩ to ground for external I2C control	
SEL	17	Selects the MUX path. Active in both Pin Mode and SMBus/I2C Mode. The pin has a weak internal pulldown resistor. Exercise the SEL pin in system implementations for MUX selection between Port A vs Port B. L: Port A selected. H: Port B selected.		
EQ0/ADDR	40	In Pin Mode: The EQ0 and EQ1 pin set receiver linear equalization CTLE (AC gain) for all channels. In SMBus/I2C Mode: The ADDR pin in conjunction with the MODE pin sets SMBus / I2C secondary address. The pin is sampled at device power-up only	Refer to Table 6-1 of the TDP20MB421 datasheet for the 5-Level EQ control settings. Refer to Table 6-2 of the TDP20MB421 datasheet for the EQ boost value	Refer to Table 6-4 in TDP20MB421 datasheet for SMBus/ I2C secondary mode address setting

Pin Name	Pin Numbers	Pin Description	Recommendation	Additional Pin Considerations
EQ1	20	In Pin Mode: The EQ0 and EQ1 pins sets receiver linear equalization CTLE (AC gain) for all channels according to Table 6-2. These pins are sampled at device power up only.	Refer to Table 6-1 of the TDP20MB421 datasheet for the 5-Level EQ control settings. Refer to Table 6-2 of the TDP20MB421 datasheet for the EQ boost value	Leave it floating in SMBus / I2C secondary mode
TEST/SCL	26	In pin-strap mode this is a TI internal test In SMBus/ I2C mode this pin serves as serial clock of the I2C bus	This needs to be pulled down via a 10kΩ resistor in pin-strap mode	External 4.7kΩ pull up resistor required for SMBus/ I2C mode
GAIN/SDA	1	In pin-strap mode this pin selects the flat gain (AC & DC) from the input to the output. This pin is sampled at power-up only. In SMBus/ I2C mode this pin serves as serial data of the I2C bus and an external pull-up is required	Refer to Table 6-1 of the TDP20MB421 datasheet for the 5-Level GAIN control settings. Recommend to leave it floating as default setting. Refer to Table 6-3 for the flat gain value	External 4.7kΩ pull up resistor required for SMBus/ I2C mode
RSVD3	19	TI Internal Test Pin	Leave it floating	
VCC	5,13	Power supply pins. VCC = 3.3V ±10%	The VCC pins on this device must be connected through a low-resistance path to the board VCC plane	Install decoupling capacitors to GND near each VCC pin
GND	2,6,9,12,16,21,30,39,EP	Ground reference for the device	The exposed pad must be connected to one or more ground planes	

3 Summary

Please follow the guidelines found in this schematic checklist when designing the TDP20MB421, but also consider the surrounding system requirements as well. Additionally, when designing the TDP20MB421 in a system, it is very important to consider functional flexibility. Having the option for the pin-strap and the SMBus/I2C mode when implementing the device allows for much easier debug and better control of the configuration and status of the TDP20MB421.

4 References

1. Texas Instruments, *TDP20MB421 DisplayPort 2.1 24Gbps 4-Channel Linear Redriver with 2:1 MUX* datasheet.

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