Application Note

Discrete Active Cell Balancing(ACB) Design

Jiemo Zhu, Will Tai

ABSTRACT

Due to the decline in battery capacity and lifespan caused by battery cell imbalance issues, this article introduces an active balancing scheme using a switch matrix combined with isolated DC/DC, which can achieve cell balancing while enabling inter-module balancing.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

There are differences in capacity and internal resistance between individual batteries, coupled with the passage of time, the increase in the number of cycles, the difference in temperature and humidity, and many other factors. This makes the individual differences more obvious, especially the performance of lithium iron phosphate batteries is more prominent. If the batteries are used in series, and if the current of charging and discharging is equal, and the amount of charge and discharge is consistent, there can be a large capacity battery that is not filled or can not be fully utilized, or the small capacity of the battery overshoot or over discharge. As a result, the capacity of the battery is not fully used or the service life is greatly reduced, so the voltage of the battery must be equalized and used in series to keep all the batteries safe and to maximize the use of the battery.

Therefore, a discrete active balancing design is proposed, relying on a switching matrix and converter to construct an active balancing topology that can achieve cross-module balancing.

2 Discrete Topo Comparison

Discrete active cell balancing typically has the following topologies: switch capacitor method

1. Flying capacitor method
2. Inductance energy storage method
3. Transformer method
4. DC/DC converter with switch matrix method

Among these, the DC/DC converter with switch matrix method stands out due to the high flexibility, allowing for energy transfer between any cell and balancing across modules. The modular design also facilitates maintenance.

Next, take two types of charge and discharge circuit modes as examples to analyze the working modes of the circuit.

Take cell2 charging as an example, turn on PWM2, PWM3, and PWMB:

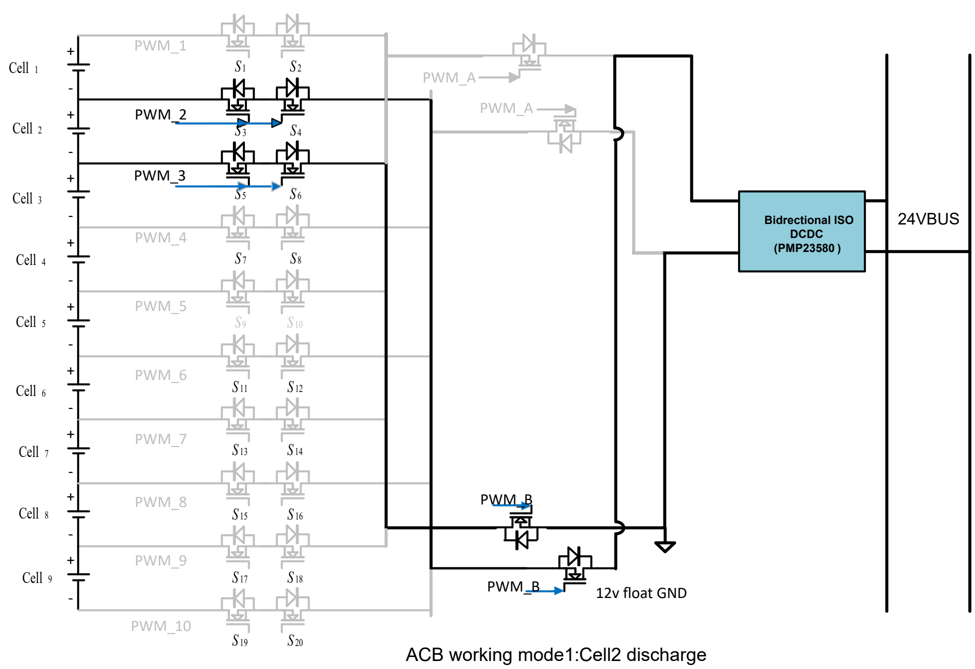

Figure 2-1. ACB Working Mode1: Cell2 Discharge

Take cell9 discharging as an example. Turn on PWM9, PWM10 and PWMA. The charging path is shown in Figure 2-2. The bidirectional DC/DC operates in boost mode, transferring the excess voltage from the battery cell to the bus.

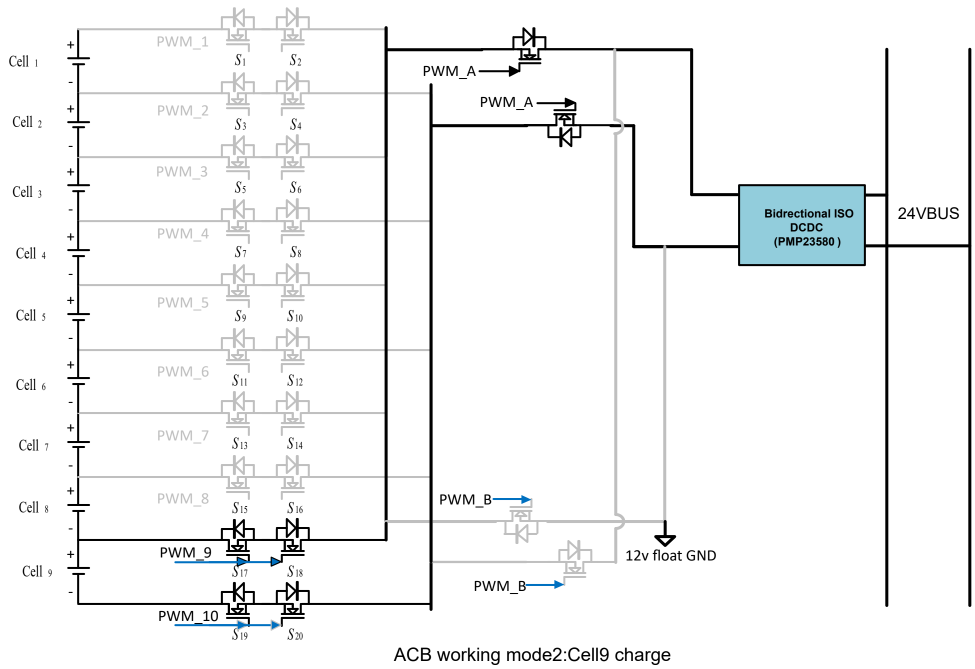

Figure 2-2. ACB Working Mode2: Cell9 Charge

Based on the status of the charging and discharging switches, the following operating mode table can be obtained. The bidirectional DC-DC operates in buck mode, transferring energy from the 24V bus to the lower voltage cells.

Table 2-1. Discrete ACB Control Logic Table

Status	Cell	Channel
Charge	Odd	PWM_A
	Even	PWM_B
Discharge	Odd	PWM_B
	Even	PWM_A

3 TI Design

The high-voltage bus uses a flyback converter to convert from the high-voltage bus to 24V as a low-voltage bus. The PMP23580 achieves bidirectional 3.0-4.2VDC to 18-36VDC, with an peak efficiency that can reach 82.3% while charging and 86.2% while discharging. The power supply rail is designed in two paths, with one non-isolated supplying power to the MCU and the other isolated supplying power to the driver circuit for the transistors. The driver circuit uses a combination of PNP and NPN forms to provide drive to the back-to-back MOSFETs in front. At the same time, the circuit can achieve balancing between modules. When discharging or charging one cell in a module, the user must select a corresponding cell in another module for charging or discharging to make sure that the bus voltage remains balanced. The 24V bus can be reused with other bus systems, and TI recommends that the reference for bus voltage control be slightly higher than the actual 24V to verify energy retrieval from other batteries during balancing, preventing energy extraction from the flyback.

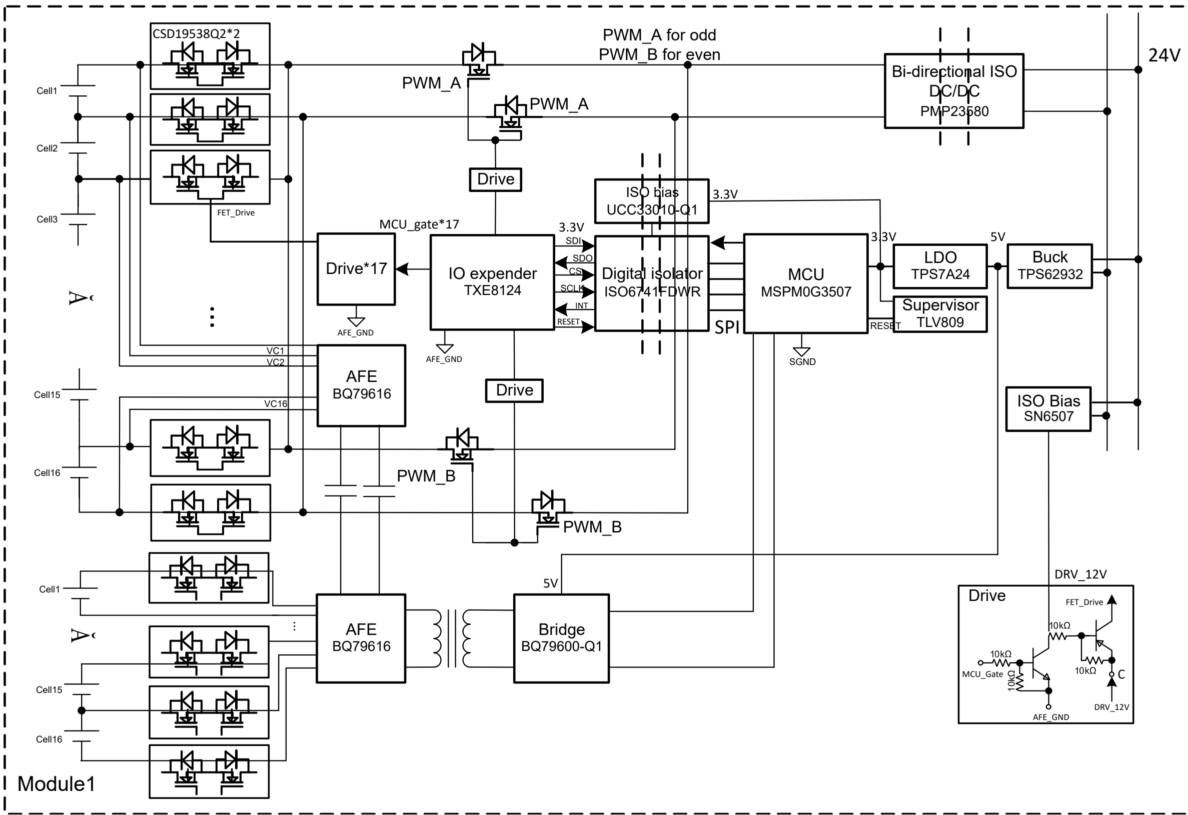

Figure 3-1. Discrete ACB System Block Diagram

4 Key Devices

4.1 TXE8124

The TXE81xx-Q1 devices provide general purpose parallel input/output (I/O) expansion for the four wire Serial Peripheral Interface (SPI) protocol and is designed for 1.62V to 5.5V VCC operation.

The device supports 10MHz from 3.3V to 5.5V and 5MHz from 1.62V to 5.5V. I/O expanders such as the TXE81xx-Q1 provide a simple design when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so on.

The TXE81xx-Q1 devices have I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable pull-up and pull-down resistors, latchable inputs, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs and a fail-safe register mode in situations of watchdog events

4.2 MSPM03507

MSPM0G350x microcontrollers (MCUs) are part of the MSP highly integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at up to 80MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62V to 3.6V. The MSPM0G350x devices provide up to 128KB embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with hardware parity option. These MCUs also incorporate a memory protection unit, 7-channel DMA, math accelerator, and a variety of high-performance analog peripherals such as two 12-bit 4Msps ADCs, configurable internal shared voltage reference, one 12-bit 1Msps DAC, three high speed comparators with built-in reference DACs, two zero-drift zero-crossover op-amps with programmable gain, and one general-purpose amplifier. These devices also offer intelligent digital peripherals such as two 16-bit advanced control timers, five general-purpose timers (with one 16-bit general-purpose timer for QEI interface, two 16-bit general-purpose timers for STANDBY mode, and one 32-bit general-purpose timer), two windowed-watchdog timers, and one RTC with alarm and calendar modes. These devices provide data integrity and encryption peripherals (AES, CRC, TRNG) and enhanced communication interfaces (four UART, two I2C, two SPI, CAN 2.0/FD). The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets project requirements. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

4.3 ISO6741

The ISO674x devices are high-performance, quad channel digital isolators ideal for cost-sensitive applications requiring up to 5000 VRMS isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO674x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications. The ISO6740 device has all four channels in the same direction, ISO6741 device has three forward and one reverse-direction channels, and ISO6742 device has two forward and two reverse direction channels. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. See *Device Functional Modes* for further details.

4.4 UCC33010

UCC33410 is an industrial DC/DC power module with integrated transformer technology designed to provide 1W of isolated output power. UCC33410 can support an input voltage operation range of 4.5V to 5.5V and regulate 3.3V output voltage with a selectable headroom of 3.7V. UCC33410 features a proprietary transformer architecture that achieves a 3kVRMS isolation rating, while simultaneously supporting low EMI and excellent load regulation. The UCC33410 integrates protection features for increased system robustness such as enable pin with fault reporting mechanism, short circuit protection and thermal shutdown. The UCC33410 comes in a miniaturized, low-profile design VSON (4.0mm × 5.00mm) package with 1mm height and > 4.1mm creepage and clearance.

4.5 LM51561

The LM5156x (LM5156 and LM51561) device is a wide input range, non-synchronous boost controller that uses peak current mode control. The device can be used in boost, SEPIC, and flyback topologies. The LM5156x device can start up from a 1-cell battery with a minimum of 2.97V if the BIAS pin is connected to the VCC pin. This device can operate with the input supply voltage as low as 1.5V if the BIAS pin is greater than 3.5V.

5 Simulation Results

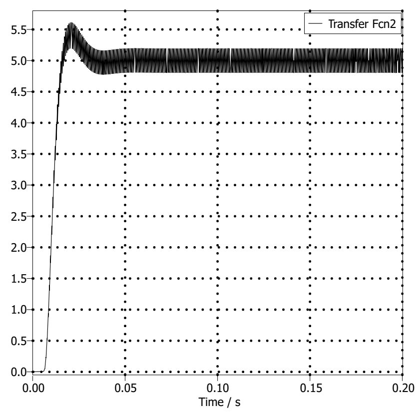

Figure 5-1. Charge Curve

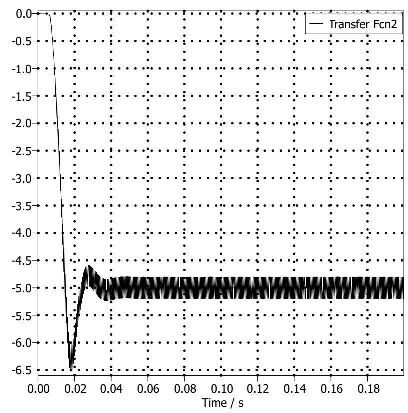

Figure 5-2. Discharge Curve

6 Summary

This discrete active balancing design can achieve balancing across battery cells while naturally enabling the balancing of the battery pack. This is also a cost-effective, relatively simple to control, and highly flexible active balancing topology with a switch matrix plus isolated DC/DC, which accelerates customers' development design of the system.

7 References

1. M. -Y. Kim, C. -H. Kim, J. -H. Kim and G. -W. Moon, "A Chain Structure of Switched Capacitor for Improved Cell Balancing Speed of Lithium-Ion Batteries," in IEEE Transactions on Industrial Electronics, vol. 61, no. 8, pp. 3989-3999, Aug. 2014, doi: 10.1109/TIE.2013.2288195.
2. A. K. Sadigh, V. Dargahi and K. Corzine, "New active capacitor voltage balancing method for five-level stacked multicell converter," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2016, pp. 1191-1197, doi: 10.1109/APEC.2016.7468020.