Application Note

Board Design and Simulation Guidelines for High-Speed Parallel Interfaces

Sitara MPU Hardware Applications

ABSTRACT

This application note contains guidelines applicable to the board design and simulations for high-speed parallel interfaces.

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1 Introduction

This document contains information applicable to board designs and simulation of high-speed parallel interfaces. These interfaces include those which employ LVCMOS I/O buffers. For supported data rates, see the device-specific data manual. This includes interfaces such as Octal Serial Peripheral Interface (OSPI), RGMII (Reduced Gigabit Media-independent Interface) and others. These interfaces are typically implemented with the use of LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) IO Buffers on respective devices. The high-speed parallel interfaces specifications are governed by the JEDEC standards such as RGMII EIA/JESD 8-6 1995.

2 Board Design and Layout Guidance

2.1 General Board Design Guidance

To verify good signaling performance, the following general board design guidelines must be followed:

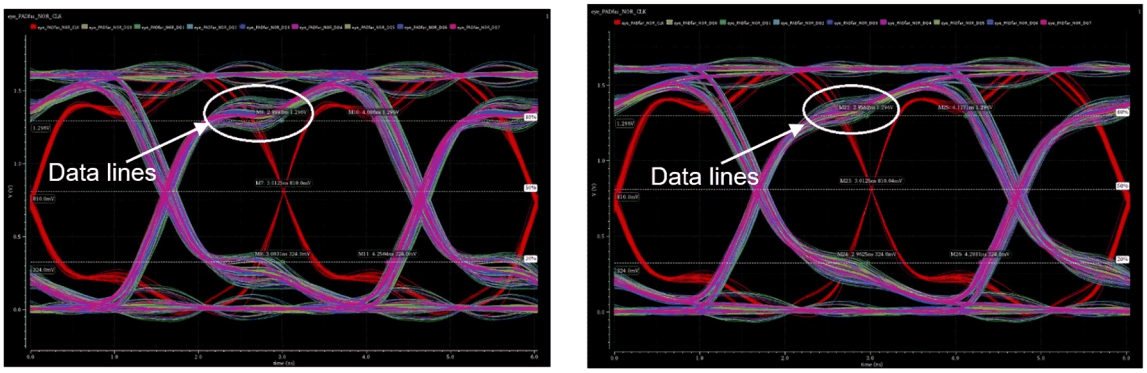
- All signals need ground reference (strongly suggest on both sides).
- Avoid crossing plane splits in the signal reference planes.
- Use the widest trace that is practical between the decoupling capacitors and the supply pin.
- Minimize inter-symbol interference (ISI) by keeping impedance matched.
- Minimize crosstalk by isolating sensitive signals, such as strobes and clocks, and by using a proper PCB stack-up.
- Avoid return path discontinuities by adding stitching vias whenever signals change layers and reference planes.
- Minimize reference voltage noise through proper isolation and proper use of decoupling capacitors.
- Keep the signal routing stub lengths as short as possible.
- Add additional spacing for clock and strobe nets to minimize crosstalk.
- Maintain a common ground (also called GND) reference for all signals and for all bypass and decoupling capacitors.
- Consider the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.
- Via-to-via coupling can be significant part of PCB-level crosstalk. Dimension and pitch of vias is important. For high speed interfaces, consider GND shielding vias. This via coupling is one factor for recommending data signals be routed on layers closest to processor.
- Via stubs affect signal integrity. Via back-drilling can improve signal integrity and is required in some instances.

2.2 Additional Board Design Guidelines for Signal Integrity

- Several factors contribute to signal integrity, and this is a system level optimization challenge.
- Various options exist to fix signal quality. Suggested options are listed in Signal Quality Options.

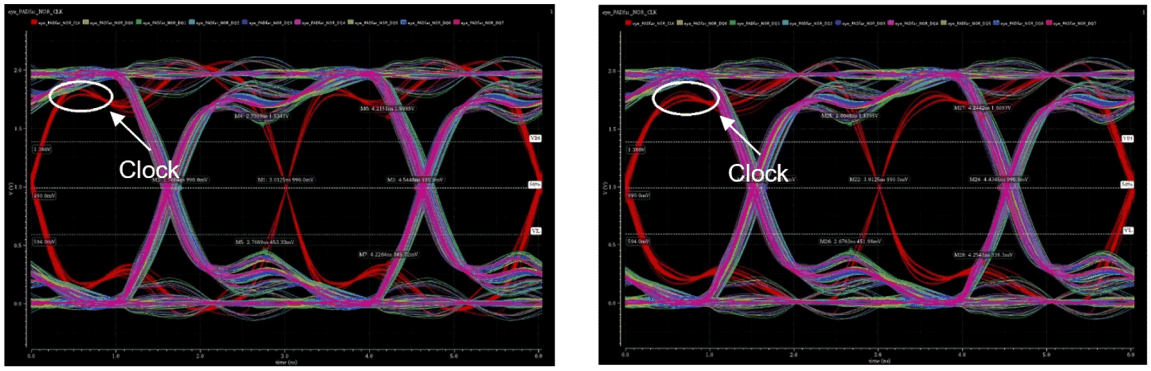
Table 2-1. Signal Quality Options

Options	Recommendation	How does this help?
A	Add series termination	Helps reduce reflections and helps with better signal quality.
B	Add load cap	Helps reduce the return reflections. Balancing cap on both ends reduces the overall reflections.
C	Increase in trace length	Prevent the out-of-phase reflection from impacting the incident signal while the signal is still transitioning.
D	Increase drive strength and combination of A, B, C	Better rise/fall and improves overall eye along with a combination of A, B, C to reduce reflections.



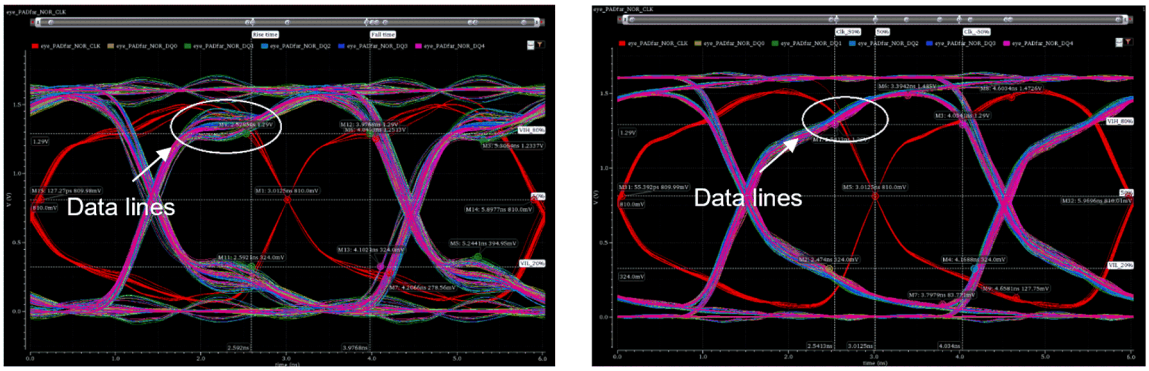
Before After

Figure 2-1. Series Termination Added on Data Lines



Before After

Figure 2-2. Load Capacitor Added on Clock



Before After

Figure 2-3. Combination of A and B on Data Lines

2.3 Design Example

This section offers some guidance for a board design to improve signal quality:

Cload represents the total capacitive load of the peripheral (Package, IO, and so on).

For Cload of approximately 2pF:

Option 1: Keep trace length very short (around 0.5 inch -0.6 inch), add a small resistor (use 10Ω or 22Ω) inserted in the middle of the trace.

Option 2: If trace length cannot be reduced to the 0.5 inch length, and trace length is between one inch and five inches, try the following options.

- Inserting the resistor in the middle of the trace as in option 1
- Adding a small lumped capacitor (use different values 1pF, 2pF, 3pF, and so on) close to the PHY BGA.

Option 3: If Option 1 and 2 are not feasible, increase trace length to the maximum allowable by the PHY spec (six inches) Adding a small lumped capacitor similar to option 2b can also be used in addition to increased trace length.

Note that these are possible suggestions to help improve signal quality. Option 1 is expected to provide the best overall signal quality but the customer must simulate and evaluate which of these options works best for a specific system.

3 Board Design Simulations

3.1 Board Model Extraction

The board level extraction guidelines listed below are intended to work in any EDA extraction tool and are not tool-specific. Follow the steps outlined in Section 3.2 immediately after completing extraction of s-parameter. The design must be checked with these steps prior to running IBIS simulations.

- For signal extractions, a 2.5D extraction is sufficient.
- Check the board stack-up for accurate layer thickness and material properties.
- If the board layout is cut prior to extraction (to reduce simulation time), then define a cut boundary that is at least 0.25 inch away from the signal and power nets.
- Use s-parameter or RLC package models (typically available from the vendor) for further simulation.

3.1.1 IBIS Model Simulations

The methodology for validating these High-speed parallel interfaces is outlined in this section. Channel simulations using IBIS models and extracted PCB models are exercised with targeted data attack bit patterns to generate signal waveforms and eye diagrams. These results need to be checked for conformity with setup/hold time, slew rate, clock high and low etc., as defined in the device data sheet. Additional checks need to be performed for ring back with respect to VIH/VIL voltage levels.

3.2 Simulation Setup

Setup the IBIS simulation with the following steps:

- Extract S-parameter files for signals on the board.
- 3D extraction tool is preferrable but not feasible due to run time limitations. If run-time limitations are a concern, use of a 2.5D extraction tool for board signals is permitted.
- Obtain the SoC IBIS model at TI.com under the product page.
- Obtain the device IBIS model from the PHY vendor. This IBIS model must include package, RLC model for device.
- Build up the simulation netlist as shown in a simulator of your choice.
- Set up the SoC IBIS model, board model, and device IBIS model.
- Build up the process, voltage, temperature corners that are going to be simulated.
- Recommended to simulate across all process, voltage, temperature supported by the IBIS model:
  - Typical
  - Minimal
  - Maximal
- Analyze the results in a waveform analysis tool and use the pass/fail checks from device data sheet specification to assess the quality of results.

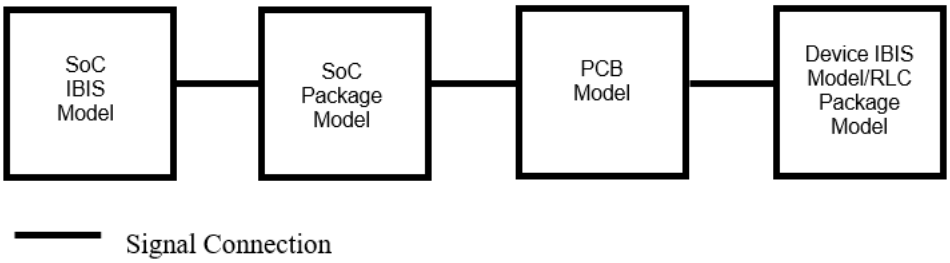


Figure 3-1. Typical System-Level Simulation Setup

4 Summary

This application report describes how to plan, route, and simulate a PCB for successful high-speed parallel interface operation. As mentioned earlier, the customer must simulate and evaluate which of these options (or any others that have been used) works best for the specific system.

5 References

1. Texas Instruments, *AM62Px eMMC HS400 Board Design and Simulation Guidelines*, application note.
2. Reduced Gigabit Media Independent Interface (RGMII)- EIA/JESD 8-6 1995.

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