Application Note

Solving TLC696x1/2/4/8-Q1 Long CCSI Daisy Chain Challenges with TLC69699-Q1 Connectivity IC

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ABSTRACT

Local dimming backlight is widely used and gets more popular in automotive display application to provide excellent user experiences such as better image contrast ratio. The TLC696xx-Q1 family is TI's 16-channel automotive local dimming LED driver that supports both direct and 2/4/8 time-multiplexing control.

The latest display backlight board can implement thousands of LEDs to achieve higher contrast ratio and thinner module thickness. More dimming zones require more local dimming LED drivers in a single daisy chain. The TLC696xx-Q1 family can have clock duty cycle increase challenges under long a Continuous Clock Serial Interface (CCSI) daisy chain configuration, which limits the maximum cascaded number.

This application note explains the clock duty cycle increase issue root cause and proposes an effective design to support more cascaded drivers based on the TLC69699-Q1 connectivity IC.

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Trademarks

1 Introduction

Local dimming backlight design selects different dimming zones based on the brightness, contrast ratio and module thickness requirements. Increased LED dimming zones require more LED drivers. The TI TLC696xx-Q1 family provides both direct drive and time-multiplexing option to meet customer dimming zone requirements. TLC696x1-Q1 is 16-channel direct-drive LED driver while the TLC696xx-Q1 can support 2/4/8 time-multiplexing matrix to achieve up to 32/64/128 dimming zones control.

Typically, local dimming LED drivers must connect all LED drivers in a single SPI loop for simple brightness control. Signal integrity challenge for the Star-Connection-SPI interface limits the maximum cascaded number. The TI TLC696xx-Q1 family is different from the traditional SPI interface, using two-wire CCSI with built-in buffer to strengthen the signal quality. As shown in Figure 1-1, the TLC696x0-Q1 connects to the TLC696xx-Q1 by a two-wire interface in a daisy chain. The CLK_I (clock input) and SIN (data input) pass through internal buffer and regenerate as CLK_O (clock output) and SOUT (data output) then pass to the next device. This type of connection can improve signal integrity and reduce system board layout complexity.

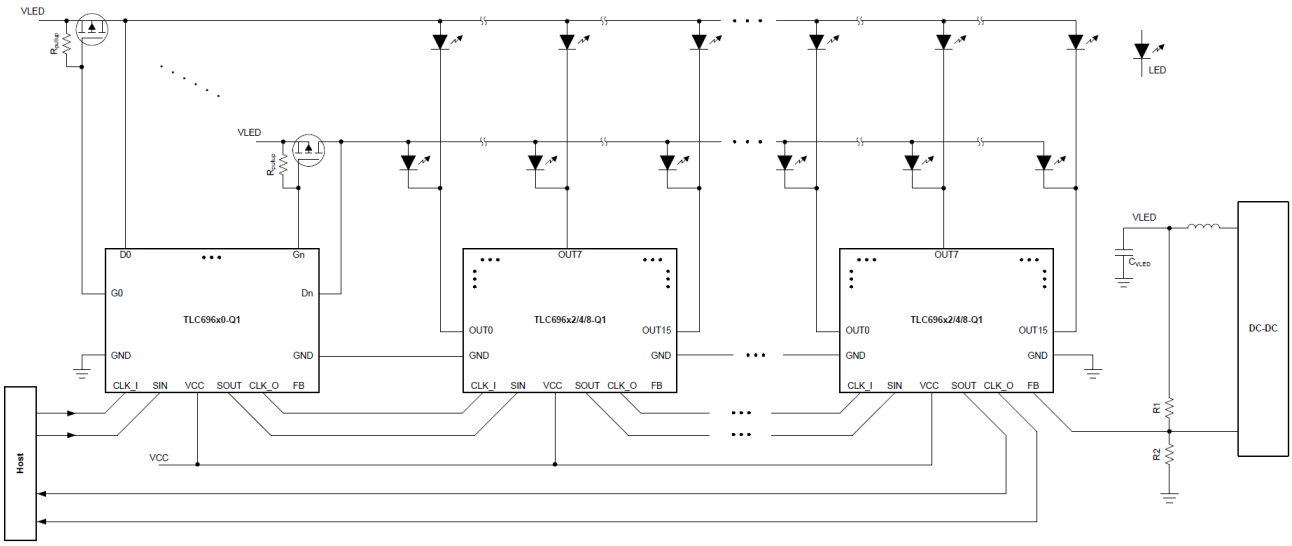

Figure 1-1. TLC696x2/4/8-Q1 CCSI Connection under Time-Multiplexing Scheme

2 Long CCSI Daisy Chain Challenges

The TLC696xx-Q1 family CCSI interface improves the clock signal quality with built-in buffer, but the maximum cascaded device number is limited by the CCSI CLK_O duty cycle increase issue. The CLK_O waveform at the end of the daisy chain device can violate the CCSI timing requirement in long daisy chain applications.

2.1 CCSI CLK_O Duty Cycle Increase Issues

The I/O voltage of the TLC696xx-Q1 family is designed to be compatible with both 1.8V and 3.3V voltage to connect to different kinds of host devices (such as a timing controller). For a logic level design of a traditional interface, the logic low voltage must refer to 0.3 × VCC, and the logic high voltage should refer to 0.7 × VCC, and the actual logic high and low value must refer to the real VCC applied to the device. The SIN/CLK_I of the TLC696xx-Q1 family logic low and high level refers to the fixed value for VCC=1.8V, as listed in Table 2-1.

Table 2-1. TLC696xx-Q1 Input Logic Level Voltage Threshold

PARAMETER		MIN	TYP	MAX	UNIT
Logic Interface					
VLOGIC_IL	Low level input voltage, SIN, CLK_I			0.54	V
VLOGIC_H	High level input voltage, SIN, CLK_I	1.26			V

With the fixed threshold, the TLC696xx-Q1 family has a CLK_O duty cycle increase behavior when the VCC voltage equals 3.3V. Figure 2-1 shows the input and output signal for the internal buffer of the first LED driver, the left side is the input signal of the first device and the right side is the output signal. Assume the host device supports to send a 3.3V/50%-duty cycle clock signal, the TLC696xx-Q1 is expected to recognize the logic high until the rising edge reaches VIH_3.3V and recognize the logic low until the falling edge reaches VIL_3.3V, but the TLC696xx-Q1 family recognizes the logic high earlier(Δt1) and recognizes the logic low later((Δt2). The logic-high period for a 50%-duty cycle clock input is recognized as T/2+Δt1+Δt2, so the LED driver regenerates a clock signal with a higher duty compared to the input.

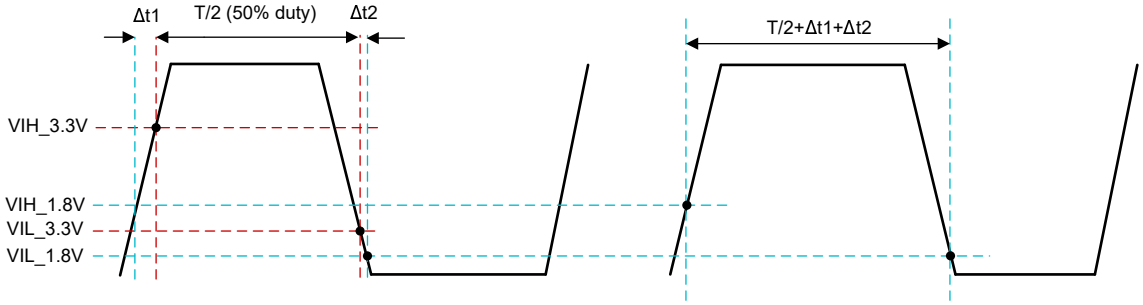

Figure 2-1. TLC696x1/2/4/8-Q1 Input and Output Clock Signal Duty Cycle Increase

The clock duty cycle increases across the daisy chain, so one of the limits for the maximum cascaded number is the minimum of the CLK_I low time, as shown in The TLC696xx-Q1 family requires a minimum of 18ns CLK_I low time to recognize a valid clock signal. Situations such as these can worsen, such as when the slew rate of the signal is slower, or the signal frequency is higher (T/2 is smaller).

Table 2-2. TLC696xx-Q1 Minimum CLK_I Low Time Requirement

PARAMETER		MIN	TYP	MAX	UNIT
SPI timing requirements					
Tw(h)	CLK_I high time	18			ns
Tw(L)	CLK_I low time	18			ns

Figure 2-2 shows a 15.6-inch display backlight design example with one FET controller (TLC69610-Q1) and a 43 piece LED driver (TLC69614-Q1) in a single daisy chain to support up to 2730 dimming zones. As shown in Figure 2-2 , when the CCSI clock frequency is 8MHz, the top side is the input of the first device, and the bottom side is the CLK_O of the last device, the duty cycle increases over the daisy chain, where the CLK low time is only 10ns. The CLK_O of the last device in the daisy chain fails to meet the minimum CLK_I low time requirement for proper readback diagnostic operation. The CLK low time of the last six devices all fail to meet the 18ns requirement, which is aligned with the actual LED backlight board bring up status. (The last six devices control the dimming zones in the black area in real LED mapping) in Figure 2-3.

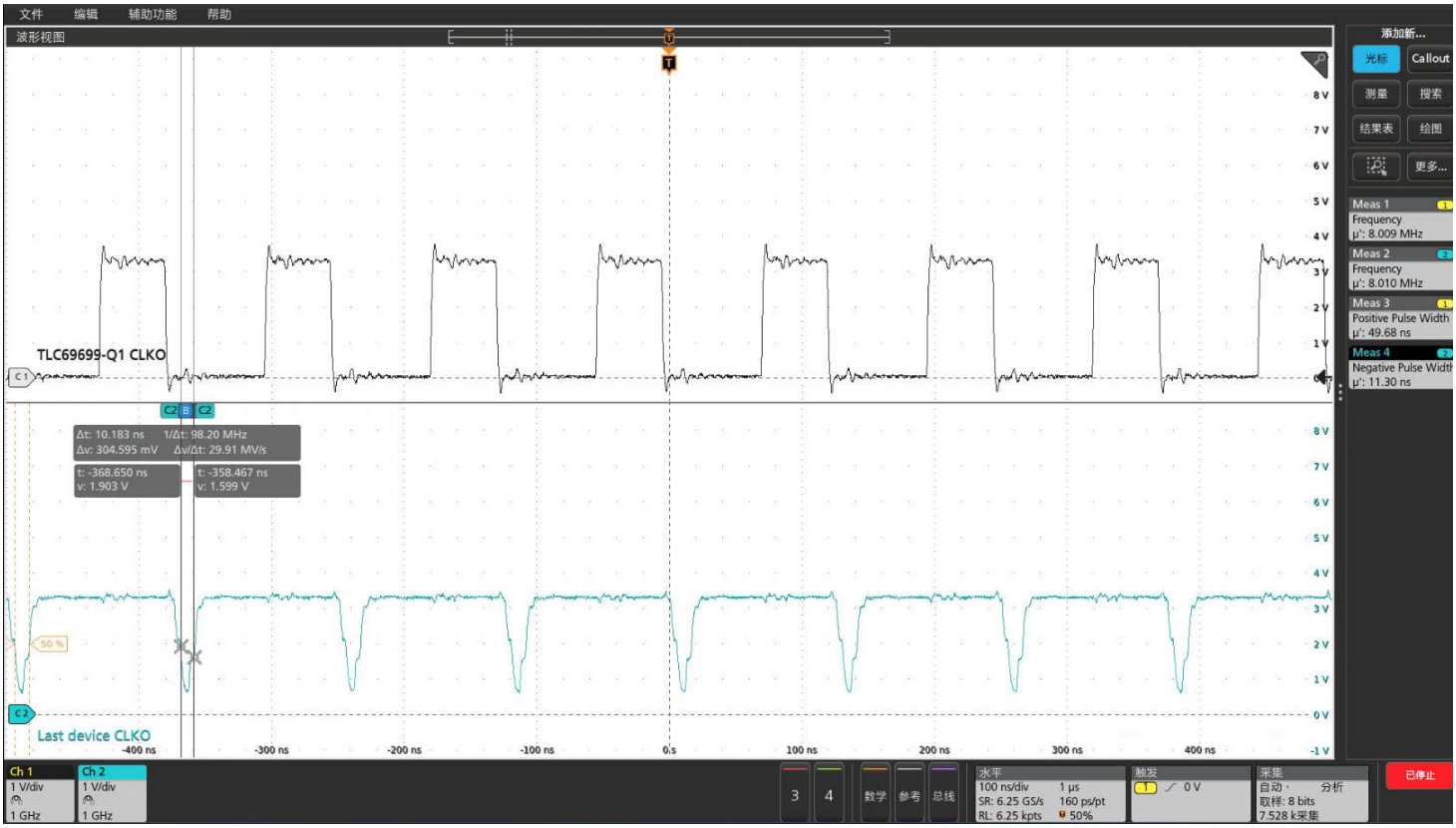

Figure 2-2. CLK_O for the 38th LED Driver

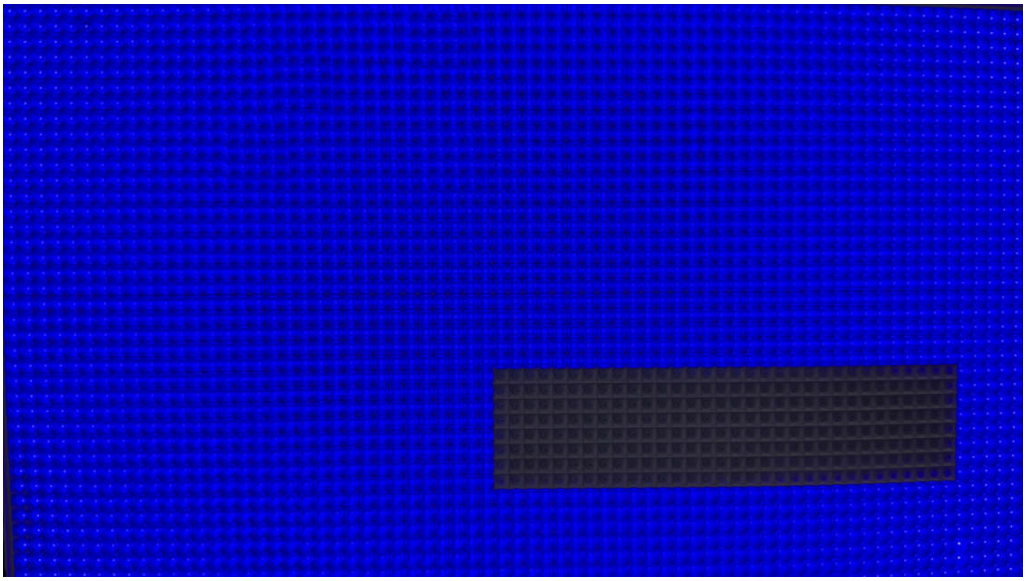

Figure 2-3. LED Board Bring Up

2.2 CCSI Frequency Design Consideration

Adjusting the CCSI frequency is the effective way to solve the CLK_O duty cycle increase challenge and support a higher cascaded number. Because the increased time ($\Delta t1+\Delta t2$) over each LED driver can be assumed to be a fixed value if the slew rate from the host controller is the same, then a lower CCSI frequency allows for a longer logic-low period(T/2). A lower CCSI frequency must pass more daisy-chained LED drivers until the CLK low time reach the minimum limit.

The TLC696xx-Q1 family CCSI frequency is related to some system level performance including EMI and audio noise cancellation. In this application note, the focus is on the basic rule to calculate the minimum CCSI frequency required, which is to display and transmit the required brightness data in a single frame. Table 2-3 lists the 43 piece LED drivers the design requirements of the cascaded system, which is an example to calculate the required frequency.

Table 2-3. Design Requirements for 43 Piece LED Driver Cascaded System

Parameter	Detailed Requirements
Part number	TLC69614-Q1
Line number	4
Frame rate	60 frames per second
Brightness resolution	12 bit
Chip number	43 pieces

Minimum frequency for PWM brightness display:

F_ Min_Display = (frame rate) × (2^brightness resolution) × (line number) = 0.98MHz

Minimum frequency for transmitting brightness (See the brightness write command in the data sheet):

F_Min_Transmission = (frame rate) × [16x3+16x (chip number) + 16 + (chip number) × 16x(line number) × 16+16] = 2.75MHz

The calculated minimum CCSI frequency for TLC696x4-Q1 to transmit and display the LED zone brightness data in one frame is 2.75MHz. But in most applications, a higher CCSI frequency must be selected to reserve more time for the TCON local dimming algorithm calculation and LED driver fault diagnostic. That's why TCON selected 8MHz as a starting point to bring up this system. In the following sections, how to further reduce the CCSI frequency required without sacrificing the system level requirements is discussed.

3 TLC69699-Q1 Connectivity IC Design

The TLC69699-Q1 is an SPI-compatible connectivity IC between an SPI and a Continuous Clock Serial Interface (CCSI). This is designed to solve the CCSI compatibility challenge with some SPI-interface TCON as shown in Figure 3-1. Adding additional TLC69699-Q1 between the host controller and the original LED driver daisy chain can help solve the CLK_O duty cycle increase limit in three ways:

1. Reducing the high-level duty cycle of CLKI and then forward to the first LED driver;
2. Saving time for polling the LOD, LSD, TSD and status every frame with fault interrupt feature;
3. Reducing the CCSI output frequency in internal TXFIFO.

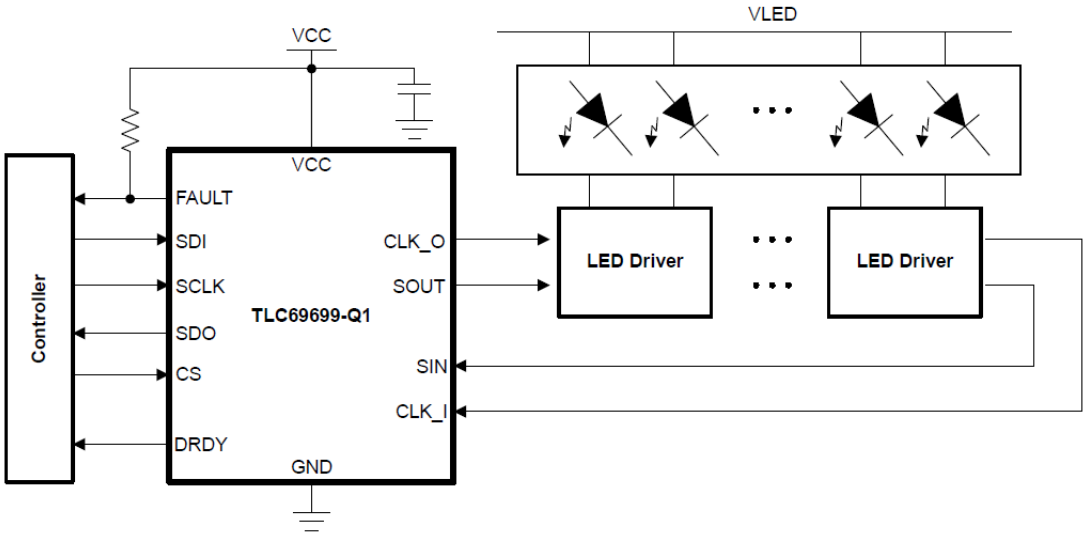

Figure 3-1. TLC69699-Q1 Typical Application

3.1 CCSI Control on the CLK_O Duty Cycle and Data Rate

The TLC69699-Q1 offers two options for duty cycle control. Apart from the traditional 50% duty cycle option, the user can also force the CLK_O high-level pulse duration as 50ns. As listed in Table 3-1, with the CCSI_DC_CTRL combined with CCSI_DATA_RATE, the CLKO high-level pulse duration can be decreased from 50% to a lower percentage. So even with CLKO duty accumulation, the low-level pulse duration can be enlarged from the start and the daisy chain device number can be enlarged.

Table 3-1. CCSICTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
6	CCSI_DC_CTRL	R/W	0x0	Duty cycle control for CCSI 0x0 = Duty cycle of CLK_O is 50% except for CCSI_DATA_RATE[3:0] = 4b'1110 (33.33%) and CCSI_DATA_RATE[3:0] = 4b'1100 (40%) 0x1 = CLK_O high level pulse duration is kept at 50ns except for CCSI_DATA_RATE[3:0] = 4b'111X where it is 25ns
5-4	RESERVED	R/W	0x0	Reserved
3-0	CCSI_DATA_RATE	R/W	0x0	Data rate for CCSI 0x0 = 1Mbit/s 0x1 = 1.25Mbit/s 0x2 = 1.43Mbit/s 0x3 = 1.67Mbit/s 0x4 = 2Mbit/s 0x5 = 2.22Mbit/s 0x6 = 2.5Mbit/s 0x7 = 2.86Mbit/s 0x8 = 3.33Mbit/s 0x9 = 4Mbit/s 0xA = 5Mbit/s 0xB = 6.67Mbit/s 0xC = 8Mbit/s 0xD = 10Mbit/s 0xE = 13.33Mbit/s 0xF = 20Mbit/s

Figure 3-2 shows the test results under 5MHz CCSI data rate when the CLK_O high-level pulse duration is forced as 50ns, which means the first LED driver in the daisy chain can receive an input clock with lower duty cycle. The low-level pulse duration of the last LED driver can reach 85.9ns, which reserves enough margin from the 18ns minimum requirement.

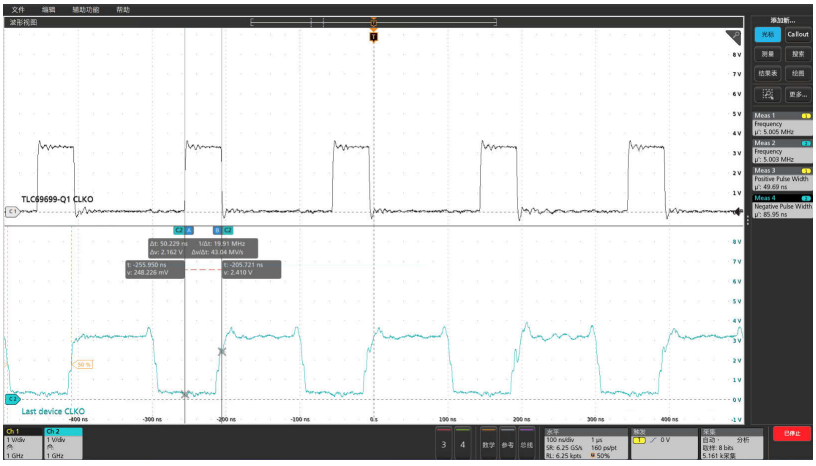

Figure 3-2. CLK_O for TLC69699-Q1 and the Last LED Driver at CCSI = 5MHz, CLK_O High-Level Pulse Duration= 50ns

3.2 Optimized Fault Readback Scheme with FAULT Signal

The TLC696xx-Q1 family support diagnostics features including the LED short detection (LSD), LED open detection (LOD) and thermal shutdown detection (TSD). As shown in Figure 3-3, the FC27 register records the current chip fault status and the FC26 register records the previous chip fault status including the chip index and the fault types. In the normal system without the additional TLC69699-Q1 device, the host controller needs to read the FC26 and FC27 register for the last LED driver device every frame to detect if there are any faults in the daisy chain if the host is not equipped with UART readback capability.

8.5.29 FC27 Register (Offset = 1Bh) [reset = 0000h]

FC27 is shown in Figure 8-60 and described in Table 8-40.

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Figure 8-60. FC27 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	CURR_CHIP_STATUS						
R/W-0h	R-0h						

Table 8-40. FC27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	This bit is reserved and must be 0.
14-7	RESERVED	R/W	0h	These bit are reserved.
6-0	CURR_CHIP_STATUS	R	0h	CURR_CHIP_STATUS [6:0] = {INT, FB_OVF, TSD, LSD, LOD, INC, DEC}

Figure 3-3. TLC696xx-Q1 FC26/27 Register Chip Status

8.5.28 FC26 Register (Offset = 1Ah) [reset = 0000h]

FC26 is shown in Figure 8-59 and described in Table 8-39.

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Figure 8-59. FC26 Register

15	14	13	12	11	10	9	8
RESERVED	PREV_CHIP_STATUS						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
PREV_CHIP_STATUS							
R-0h							

Table 8-39. FC26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	This bit is reserved and must be 0.
14-0	PREV_CHIP_STATUS	R	0h	PREV_CHIP_STATUS {14, 13, 12, 11, 10, [9:0]} = {TSD, LSD, LOD, INC, DEC, chip_idx}

Figure 3-4. FC26 Register and Field Descriptions

TLC69699-Q1 implements the fault interrupt pin to indicate multiple fault types in the system, including the DAISY_CHAIN_FAULT, which indicates one or multiple devices in the daisy chain report LOD, LSD and TSD errors. The host controller can detect the FAULT interrupt status of TLC69699-Q1 and read the FC26/FC27 register of the TLC696xx-Q1 to further locate the chip index and fault type. Mapping the DAISY_CHAIN_FAULT to fault interrupt signal can save additional time for reading FC26/27 every frame, which can help effectively reduce the CCSI frequency.

With the DAISY_CHAIN_FAULT interrupt feature, the time reserved for the fault polling can be removed. So the TCON can reduce the SPI frequency from 8MHz to 5.2MHz in this 43 piece cascaded case. The next section explains the setting of the SPI frequency in detail.

3.3 TXFIFO Configuration

TXFIFO Configuration

The TLC69699-Q1 has both a transmit and a receive FIFO, the transmit FIFO (TXFIFO) is the data that was received by the SPI peripheral and transmitted by the CCSI controller. Both FIFOs are 16-bit-wide first-in-first-out memory buffers. The FIFOs are used to store data words to full-fill the timing requirements while the data is crossing between the SPI clock domain and CCSI clock domain. When the SPI clock domain runs at a higher frequency than the CCSI clock domain, the TXFIFO stores data already received by the SPI peripheral which has not been transmitted yet by the CCSI controller. A counter (TXFFST) keeps track of the number of words currently stored in the TXFIFO, the maximum TXFFST value can be set to 0x1FF. An example where the SPI peripheral runs at a higher clock frequency than the CCSI controller is depicted in Figure 3-5 , set a lower CCSI frequency than the SPI frequency as long as the FIFO overflow is properly prevented.

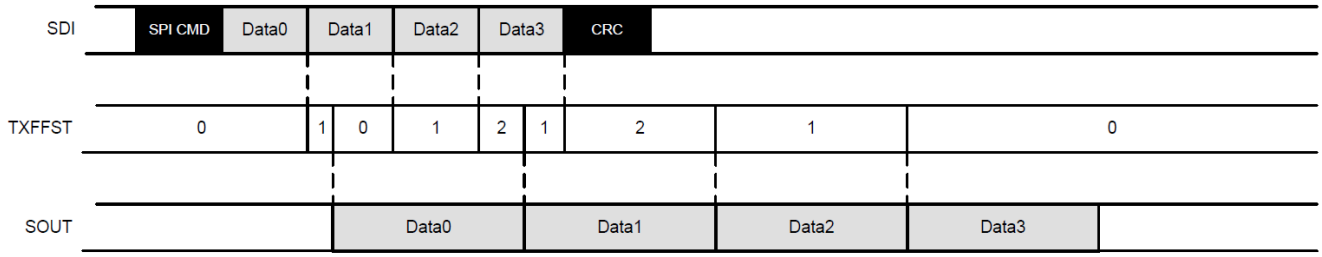

Figure 3-5. Example of SPI Peripheral Running at Higher Frequency than CCSI Controller

TCON can lower the SPI frequency from 8MHz to 5.2MHz now and the TLC69699-Q1 TXFIFO can help further reduce the CCSI frequency to 5MHz or lower, as shown in Figure 3-6 , the bottom waveform is the TCON SPI output at 5.2MHz and the top side is the TLC69699-Q1 CCSI output at 5MHz. A lower CCSI output frequency for TLC69699-Q1 can be set with CCSI_DATA_RATE as long as the FIFO overflow is properly prevented.

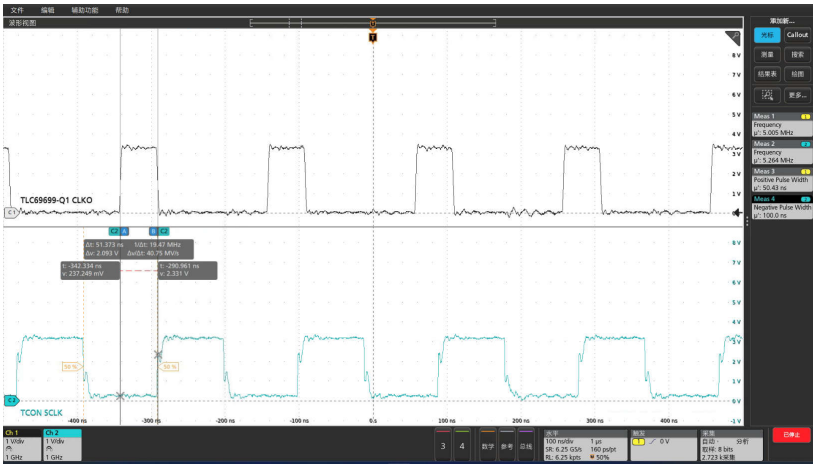

Figure 3-6. TLC69699-Q1 Input and Output Frequency Control with TXFIFO

4 Summary

The TLC696xx-Q1 family has the CLK_O duty cycle increase behavior under 3.3V I/O voltage, so the minimum clock low time limits the maximum cascaded LED drivers. TLC69699-Q1 can help decrease the required CCSI frequency with CCSI duty cycle control, optimized fault-readback scheme, and TXFIFO features, which allows more cascaded TLC696xx-Q1 drivers in a single long daisy chain.

5 References

1. Texas Instruments, *TLC69699-Q1 Automotive SPI-Compatible Connectivity for TLC696xx-Q1 Device Family*, data sheet.
2. Texas Instruments, *TLC696x2/4/8-Q1 16-Channel, 2/4/8 Time-Multiplexing, Automotive Local Dimming Backlight LED Driver*, data sheet.

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