Application Note

Small Form Factor Design for BQ25190

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ABSTRACT

This application note demonstrates the compact power and charging implementation provided by the BQ25190 linear battery charger. The BQ25190 is an excellent choice for wearables, medical devices, smart trackers, and other space-constrained applications. The BQ25190 simplifies complex power tree solution sizes by integrating multiple power rails along with a battery charger, an ADC, a sequencer, and a GPIO expander all in a compact 2.25mm x 2.75mm WCSP package. For applications where PCBA space is a premium, further design accommodations can be made to minimize the total solution size for the BQ25190.

The BQ25190 solution size, including passive components, can be reduced to a 30mm^2 area when optimized for size. This involves component selection, schematic design, layout decisions, and application considerations.

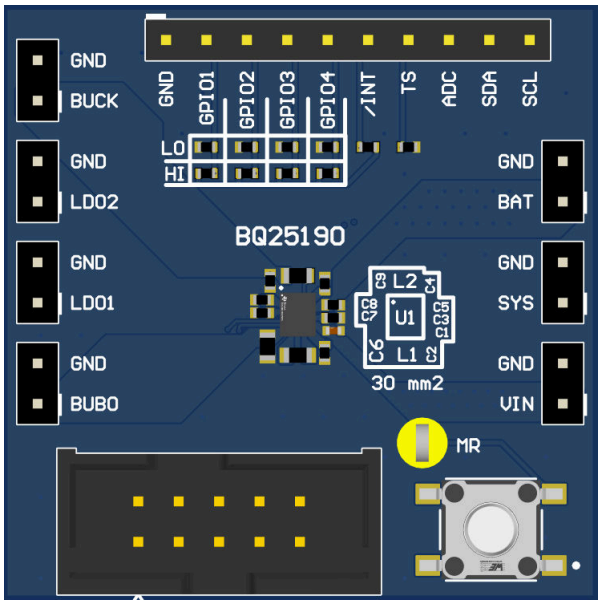

Figure 1-1. BQ25190 Small Form Factor Board

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Trademarks

1 Introduction

The objective of this design is to implement a BQ25190 with as much functionality as possible while minimizing solution size and manufacturing cost. Design with a focus on solution size involves multiple steps including component selection, schematic design, and layout design. For each step, consider application requirements, such as thermal requirements or input voltage range requirements. This reference design is created with a focus for a compact solution that is apt for small, low-powered applications such as smart watches, insulin pumps, and other wearables.

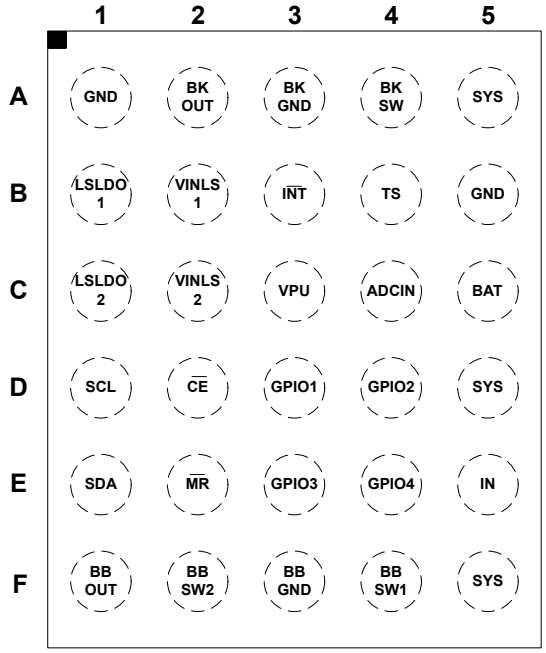

Figure 1-1. BQ25190 Pinout

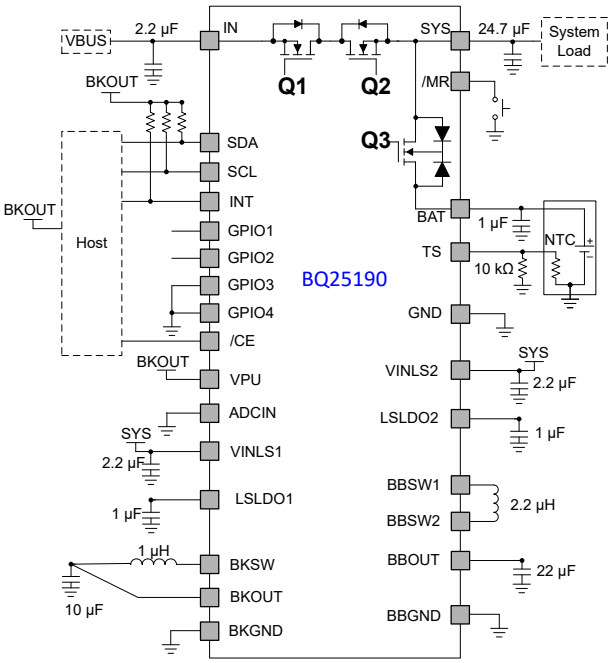

Figure 1-2. BQ25190 Typical Application

The BQ25190 and the critical passive components can be placed in a 30mm^2 area. These design changes are an excellent choice for lower power applications which do not require as much copper and space for heat dissipation as compared to high-current applications. The board uses primarily 6 mil traces and 6 mil vias for digital signals, while maximizing the width of current-carrying traces to reduce trace resistive losses. The board is optimized for charging and critical power functions at the cost of some functionality. Consider the end application functional requirements for any design, which can limit the amount of space saving optimizations that can be made.

Features of the BQ25190

The BQ25190 integrates many features and rails used for robust power and battery management systems.

- I^{2}C interface for configuration and monitoring
- 2µA active battery quiescent current
- 15nA ship mode quiescent current
- Charge current configurable range of 5mA to 1A
- Termination current configurable down to 1mA
- Integrated 12-bit ADC
- Integrated 600mA DVS buck regulator
- Integrated 600mA buck-boost regulator
- 2x Integrated 200mA LDO regulators
- Wide 3V to 18V input voltage range

2 Schematic Design Guide

For the BQ25190, optimizing for space means minimizing component counts, identifying unused pins, alternate connection paths, and selecting the smallest valid components.

The device offers four GPIOs, each with various functions accessible via register programmability. Pins GPIO3 and GPIO4, by default, are used in determining default buck output voltage. The voltage is dependent on GPIO3 and GPIO4 being pulled high, or low, to select one of four default voltages:

	GPIO3 Low	GPIO3 High
GPIO4 Low	1.8V Default V_{buck}	3.3V Default V_{buck}
GPIO4 High	2.5V Default V_{buck}	1.2V Default V_{buck}

For configurability these signals are typically routed out to a pull-up or pull-down resistors. By selecting the best default voltage and directly tying these pins to either GND or SYS, the need for pull-up or pull-down resistors is eliminated.

Component selection can be optimized for space at the cost of some application performance limitations. The table below demonstrates a comparison of component selection between the EVM and the small solution size, as well as a size comparison:

Component	EVM Component	Small Form Factor Component
C_{IN}	10uF | 35V | 0603	22uF | 10V | 0402
$C_{VINLS\ (1\ and\ 2)}$	2.2uF | 6.3V | 0402	None
I_{BB}	2.2uH | 1.7A | 0.14Ω | 0805	2.2uH | 1.05A | 0.25Ω | 0603
I_{BK}	1uH | 2.7A | 0.056Ω | 0805	1uH | 1.6A | 0.114Ω | 0603

These component selections do have impact on performance, but the total solution size is improved. C_{IN} has a reduced capacitance and a reduced rated voltage. This shrinks the operational input voltage range for this application. The changes in inductors (I_{BB} and I_{BK}) have an impact on efficiency due to the changes in DCR. The VINLS capacitors are not needed for this scenario due to the capacitance already on the SYS line and low resistance between VINLS pins and SYS nodes, though this can have an impact on very-fast transient load performance.

Unused pins left as *No Connect* can reduce the routing requirements of the board and make routing out the signals that are needed easily. Less signals with routing out of the IC means that passive components to be pulled in closer. Table 2-1 shows are some signals that can be left open but still allow critical charging and power rail operations:

Table 2-1. No-Connect Signals

Signal	Impact of No-Connect	Mitigation Actions
GPIO1	Loss of GPIO1 functions	
GPIO2	Loss of GPIO2 functions	
/CE	Charge enabled by default	Charge can be disabled via I^2C.
/MR	Push-button-driven hardware reset and Shipmode Entry / Exit functions lost.	HW Reset and Shipmode Entry can be done via I^2C. Shipmode Exit can be done via VIN assertion.
/INT	Loss of /INT reporting to notify of asynchronous event or fault.	Device status and fault registers can be polled for changes in behavior.
ADCIN	Loss of ADCIN channel.	
TS	Loss of TS function. Device detects TS fault by default which prevents charging.	TS_ACTION_EN = 0 can be used to enable charging despite detected TS Fault.

2.1 BQ25190 Schematic

The BQ25190 Small Form Factor schematic are shown in Figure 2-1. The components are the required components for operation and included in the 30mm^2 solution size for the charger.

Components outside of this section are not essential for operation but are included for end user interaction and configuration of the default V_{buck} setting. In a final application, the GPIO resistors can be directly shorted to GND or SYS for configuration without adding to the bill of materials or solution size. Included in this design are also the TS resistor, I^{2}C Pull-ups, a push-button, and a USB2ANY interface. These components are found on other parts of the application, shared with other components, or directly present on a battery pack.

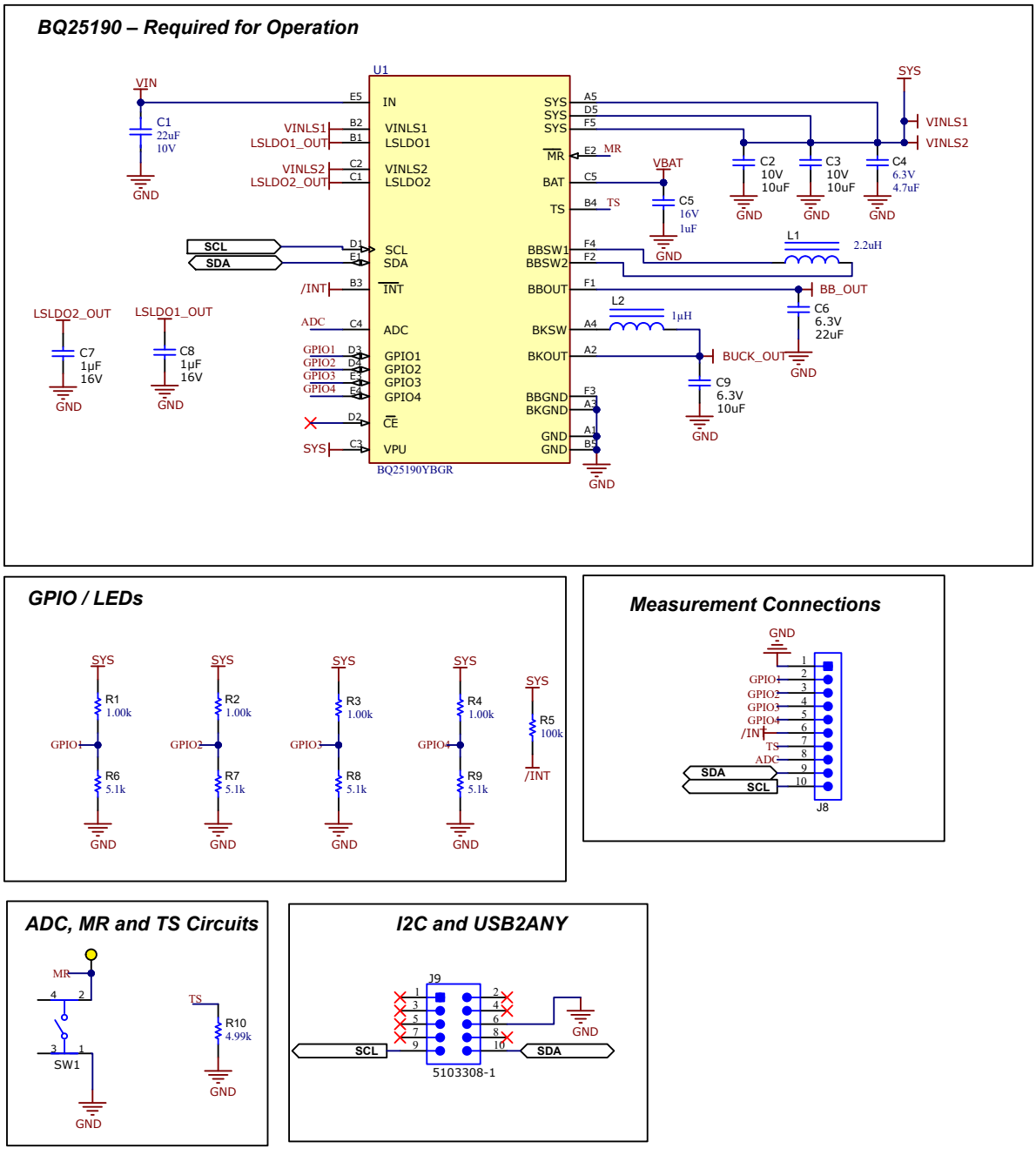

Figure 2-1. BQ25190 Small-Form Factor Schematic

3 Layout Design Guide

One step in improving solution size is pulling external components as close to the integrated circuit as is manufacturable. Current-carrying traces need to be prioritized for least resistance, while digital and control signals can be broken out using smaller traces and deeper layers. Most of the current-carrying pins are directly accessible on the top layer so routing these signals is fairly straightforward. By leaving some pins unused, other signals can be routed on a lower layer that are otherwise blocked by a routing via. For instance, the D2 pin (CE) typically requires a via to be routed out since the pin is blocked in all directions from being routed out in the top layer. Without this via, the GPIO3 and GPIO4 signals can be routed on a lower layer in the space below the D2 pin.

Typically, the VINLS capacitors require pins B2 and C2 to be routed out, which require the LDO capacitors to be pulled further away from the device and increase the solution size. Shorting both to VPU and SYS allows the pins to be routed out on the surface and shorted to SYS. Resistance between the VINLS pins and SYS pin need to be minimized. To minimize noise, TI recommends that the second layer be kept an unbroken GND plane. Figure 3-1 illustrates the signal fan out on this design. Figure 3-2 clarifies the placement of the various passive components. If the ADC pin function is not used, then the SYS rail can be routed diagonally from D5 through C4, to C3, C2, and B1 all on the top layer.

Access to the internal pins, of B3, C3, D3, and E3 reduce the need for blind vias as present in the BQ25190EVM. This also reduces the cost PCB manufacturing.

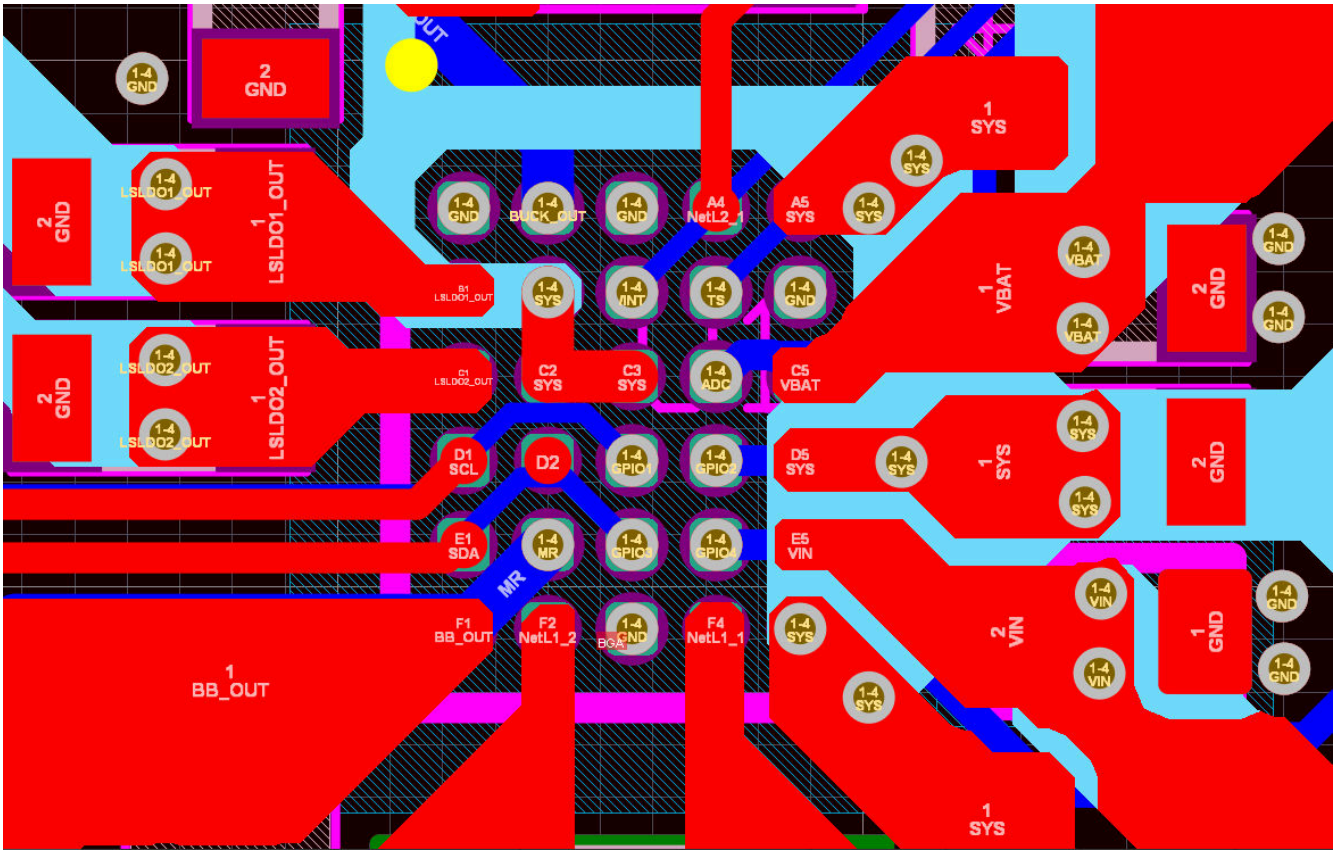

Figure 3-1. BQ25190 Layout with Signal Names

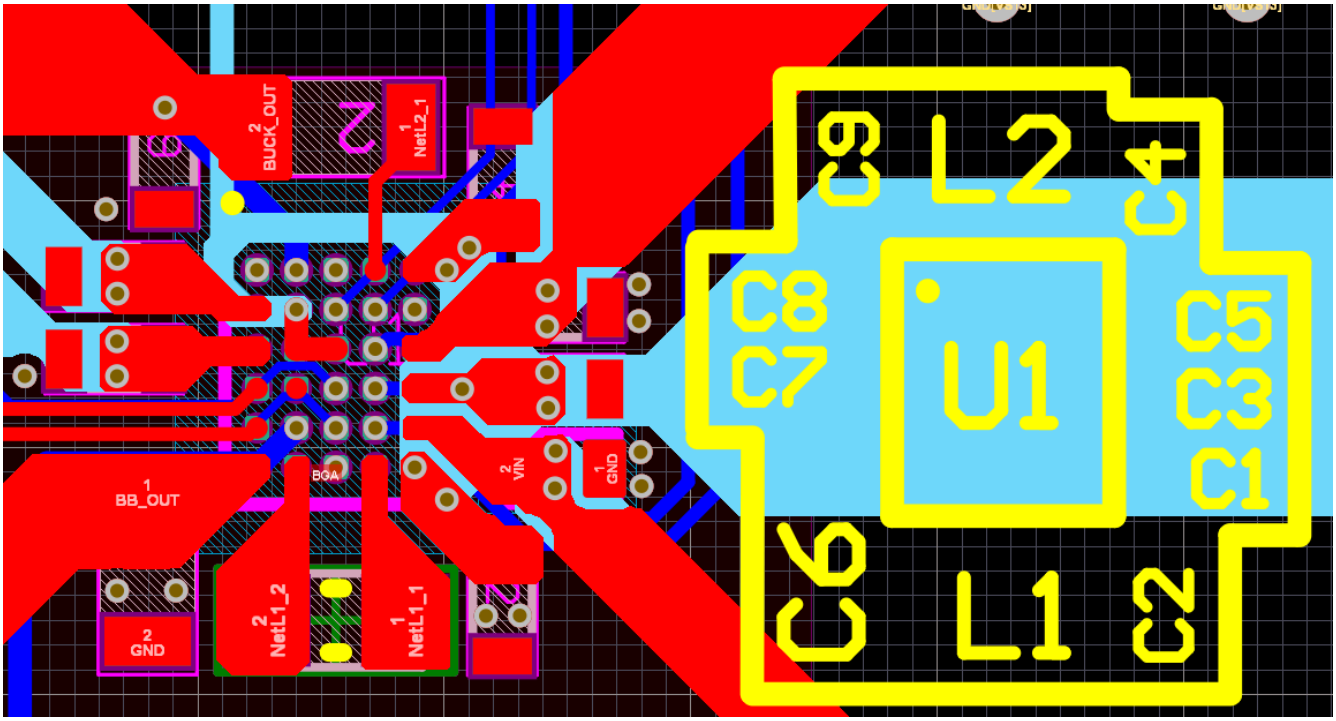

Figure 3-2. BQ25190 Layout with Component Labels

4 PCB Layer Plots

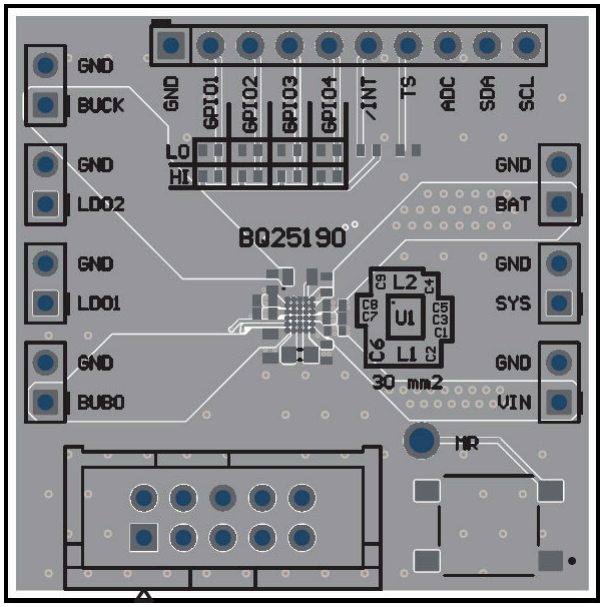

Figure 4-1. Top Layer with Overlay

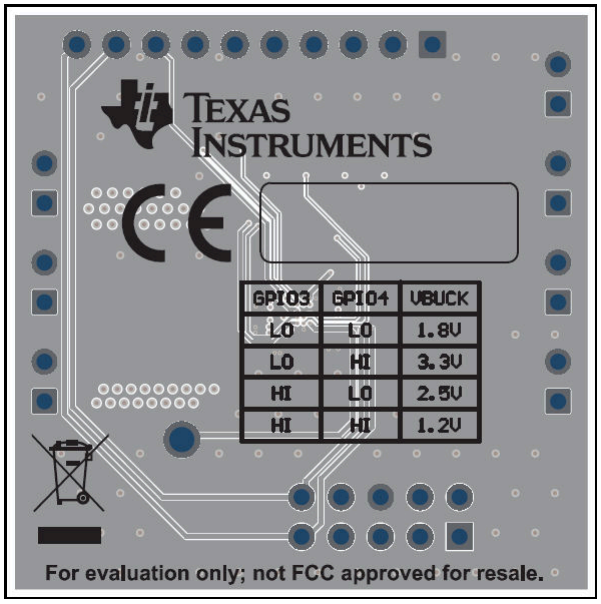

Figure 4-2. Bottom Layer with Overlay

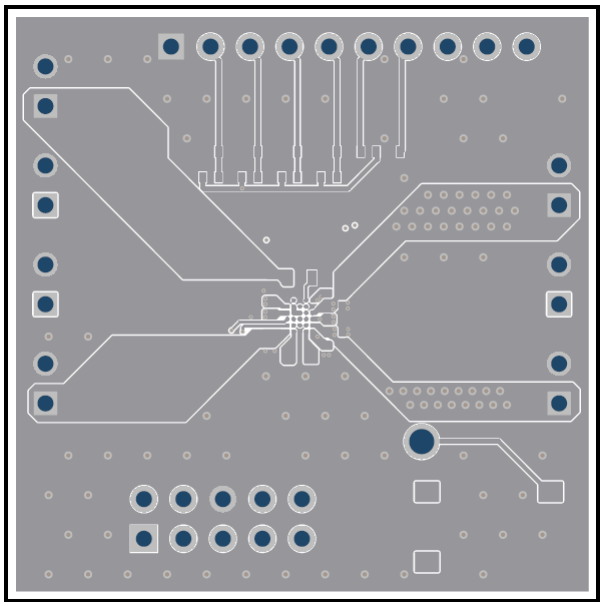

Figure 4-3. Top Layer

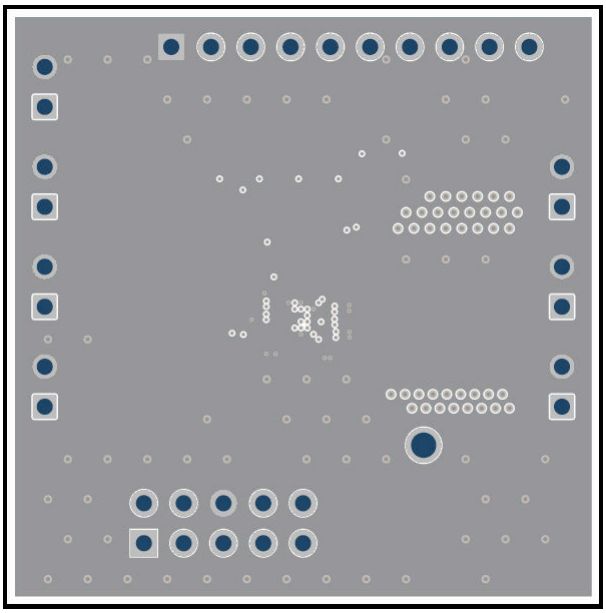

Figure 4-4. Layer 2

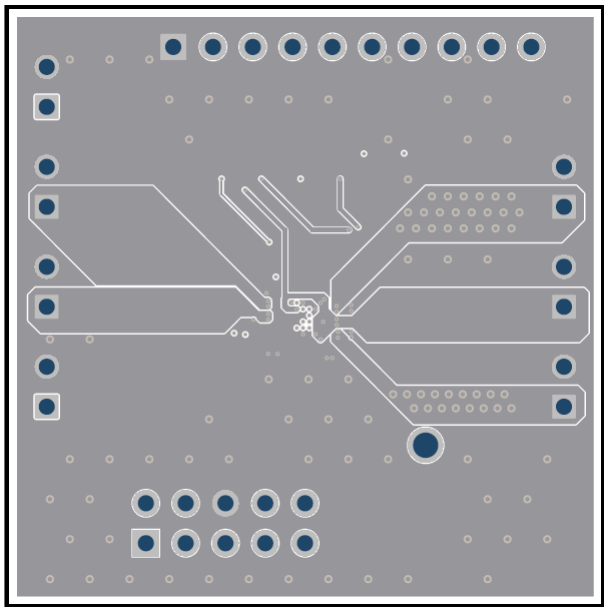

Figure 4-5. Layer 3

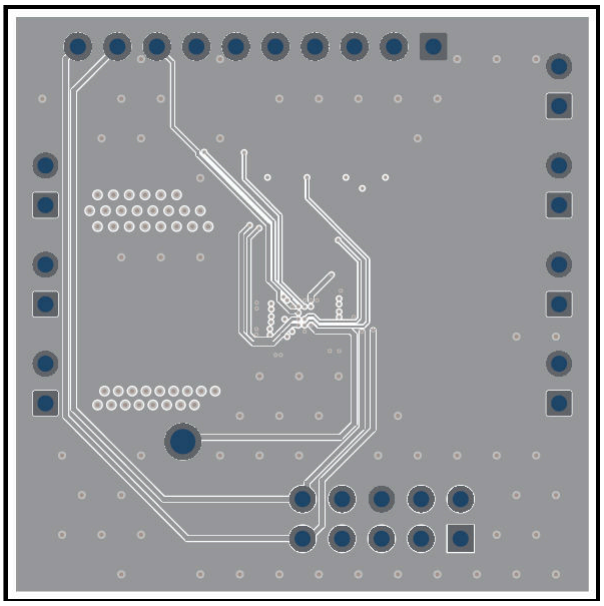

Figure 4-6. Bottom Layer

5 Summary

This document showcases the capabilities of the BQ25190 linear battery charger for space-constrained applications. The highly integrated device combines multiple power rails, battery charging functionality, ADC, sequencer, and GPIO expansion in a single 2.25mm x 2.75mm WCSP package. The BQ25190 provides an excellent power and charging implementation for wearables, medical devices, and smart trackers where board space is limited, with additional design options available to further minimize the overall solution footprint.

6 References

- Texas Instruments, BQ25190 product page
- Texas Instruments, BQ25190 Evaluation Module User's Guide
- Texas Instruments, BQ21061 Two-Layer Small Form Factor Reference Design For Cost-Optimized PCBs, application note
- Texas Instruments, BQ25180 and BQ25181 I2C Controlled Linear Battery Chargers Small Form Factor Design, application note

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