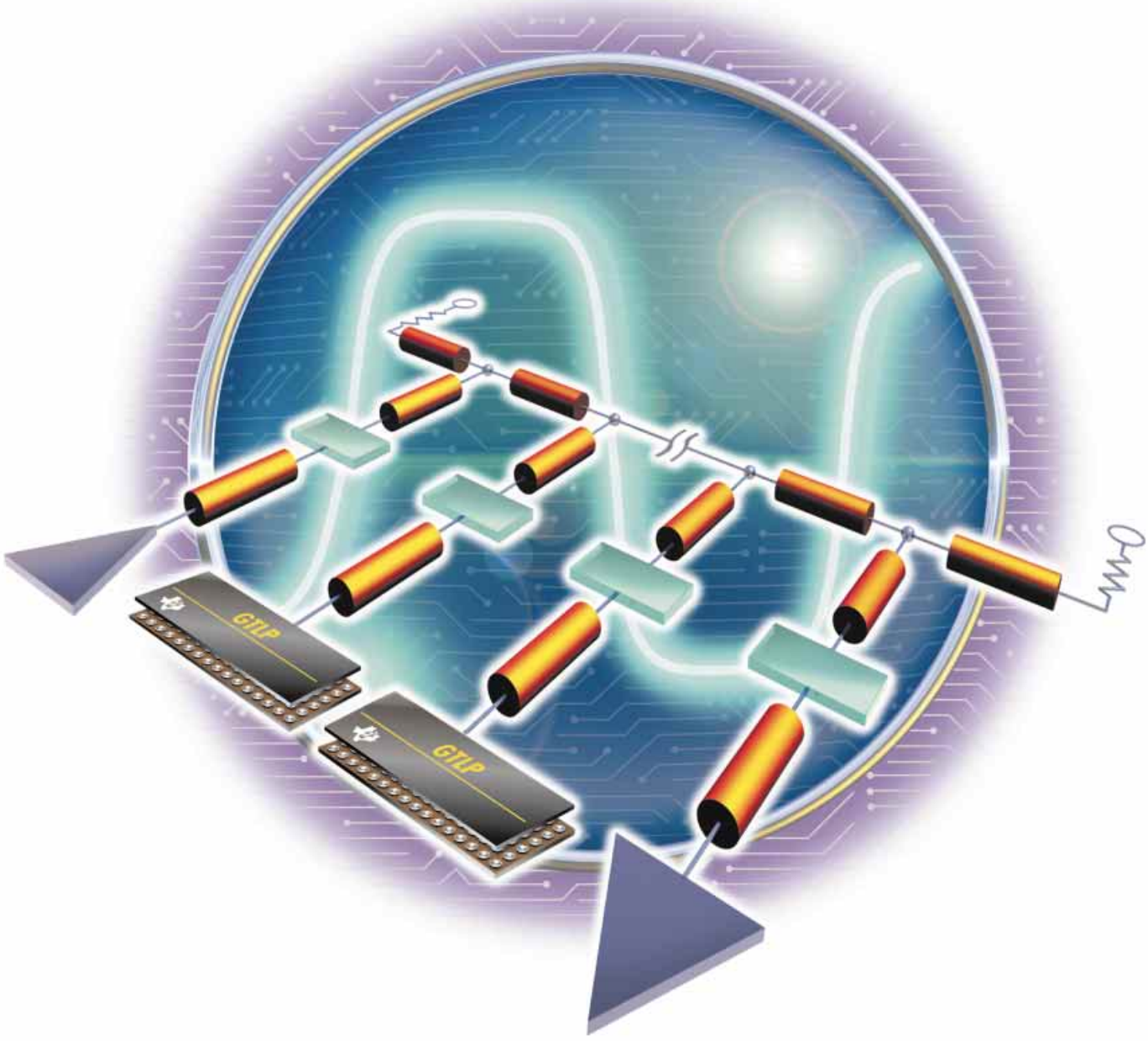
SLL Advanced Bus Interface Logic Products

Selection Guide and Reference



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For more information about Advanced Bus Interface Products, visit www.ti.com/sc/logic

TEXAS INSTRUMENTS

Bus Interface Solutions Overview

Introduction

In today's information-hungry society, transmitting data over several inches between computer memory and display screen is just as critical as sending it halfway around the globe on fiber optics. Texas Instruments (TI) is constantly pushing the capabilities and extending the performance parameters of practically every data transmission standard, including RS-232, RS-423, RS-422, RS-485, Fibre Channel, VME, LVDS (low voltage differential signaling), IEEE 1394 (Firewire), USB (Universal Serial Bus), GeoPort, IrDA (Infrared Data Association), BTL and GTL. Over the past 3 years, TI SLL has combined its expertise in high-speed digital and analog technologies to offer new single-ended backplane optimized transceivers, which provide higher data rates in distributed loads to allow tier 2 uses an alternative to more complex and costly differential solutions.

Within a data transmission system, there are numerous ways of connecting the transmitters, receivers, boards and backplanes. Figure 1 shows how cards are connected in a typical equipment cabinet. In some situations, it is necessary to connect individual cards together with high data throughput point to point connections but most equipment racks include multicard backplanes where control or data signals are shared via backplane board traces. This selection guide features the best single-ended solutions that provide tier 2 users excellent signal integrity across their multicard backplanes.

Data transmission is the catch-all phrase for moving data from one location to another and two parameters are important—the distance between the sending and receiving systems and rate at which data has to be passed to the receiving device. Different transmission standards, such as RS-232, FireWire, LVDS and Gigabit CMOS, provide solutions for various needs in terms of speed and line length for tier 1, 2 and 3 users as shown in Figure 2. Advanced bus solution logic products offer an alternative to tier 2 users over shorter transmission lengths especially with the new GTLP devices.

Every data transmission solution is a translator with one side of the device typically operating at common LVTTL signal levels but the other side optimized for higher data throughput. Shorter voltage swings reduce EMI since the edge rate (slew rate) can be slower and still allow higher transmission rates. Differential complementary signals cancel out common-mode noise that improves signal quality.

For *Differential or Balanced Transmission,* a pair of cables or traces is necessary for each channel. On one line, a "true" signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects basically the difference in inputs and voltage switches the output depending on which input line is more positive than the other one. Due to the common-mode rejection capability of a differential amplifier this noise will be rejected. Additionally, any external noise is coupled onto both lines as a common-mode voltage and is rejected by the receivers.

Single-Ended Transmission is performed on one signal line and the output is interpreted with respect to ground. The advantages of single-ended transmission are simplicity and low cost of implementation. Since a single-ended

Figure 1. Solutions for System Connections

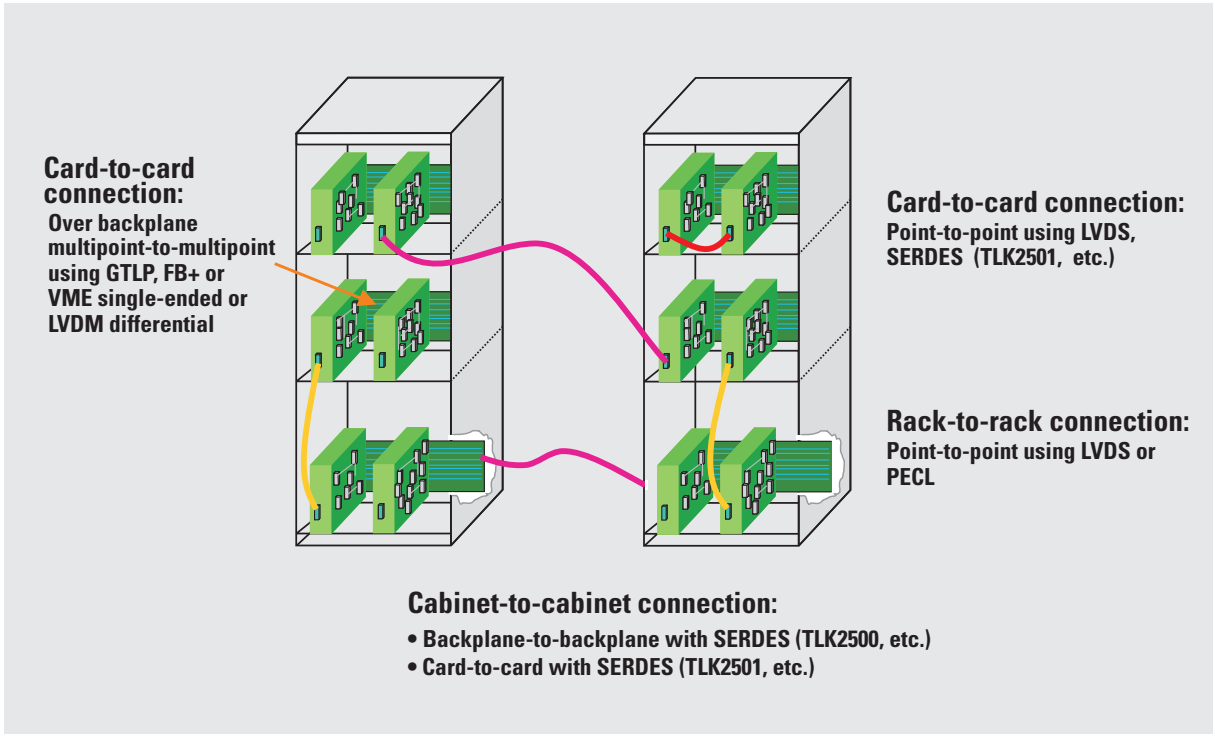
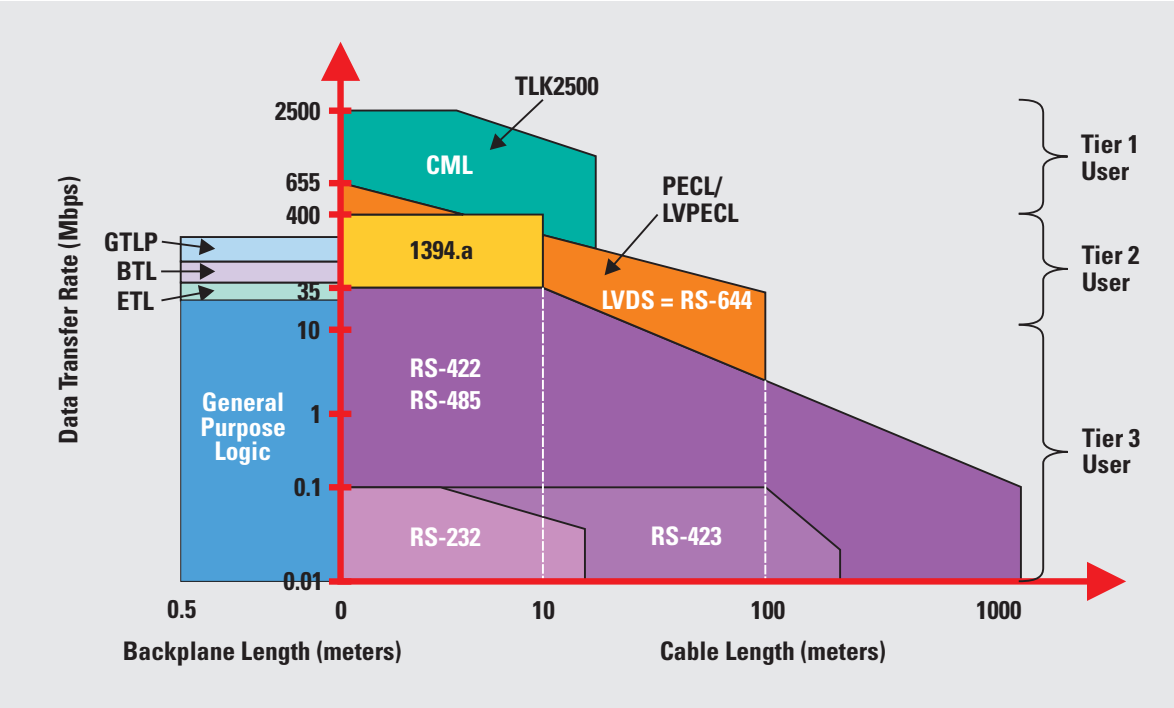


Figure 2. Data Rate vs. Transmission Length



system requires only one line per signal, while differential signals require two, it is ideal for parallel communication where many lines are required, e.g., PC, parallel printer port or serial communication with many handshaking lines, e.g., EIA-232 at tier 3 levels and on VME or proprietary backplanes at tier 2 levels. Finally, single-ended devices transfer data but also offer various logic functions like flip-flops and registers in addition to transceivers that come in small, medium and large bit widths. Most differential devices only send or receive data.

The main disadvantage of the single-ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation. This may lead to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching thresholds of the receiver device, thus increasing its susceptibility to electromagnetic fields. Additionally, the large voltage swings contribute to EMI.

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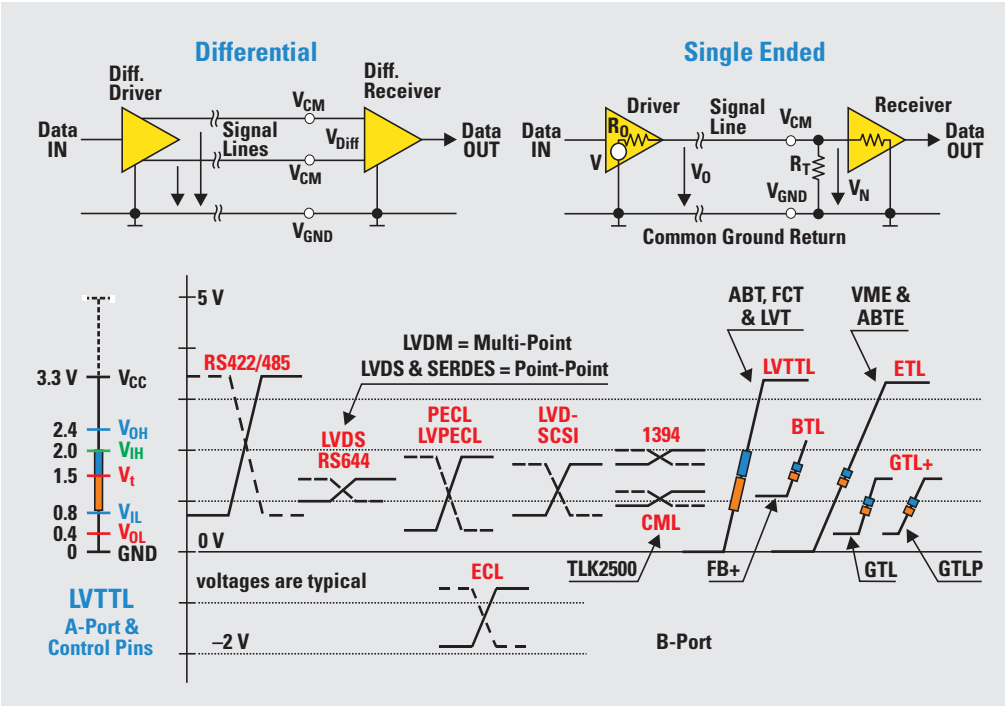
Figure 3. Every Bus Solution Is a Translator



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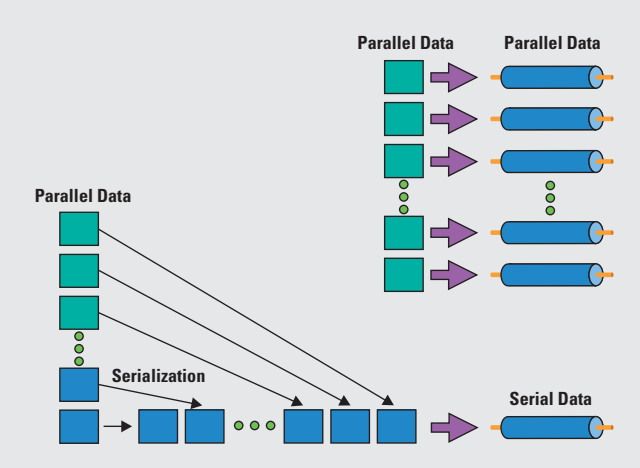
New *Advanced Bus Interface Logic* devices such as GTLP and VME have, however, been optimized to reduce these disadvantages while at the same time offering the simplicity of implementation of previous single-ended devices. GTLP features relatively small voltage swings to reduce EMI and has a reduced threshold differential input that increases the noise margin. Similarly, VME offers a reduced threshold input region to increase the noise margin but has full swing outputs since it is designed to operate into existing TTL backplanes. Both GTLP and VME were designed into models of distributed loads with their performance optimized for the low impedance environment they are going to be operated in. They both have slower edge rates (0.4 to 0.5 V/ns) that reduce ringing and improve signal integrity.

To better understand the principle of parallel and serial transmission, Figure 4 shows the difference between the two. In a purely parallel situation, such as a typical telecom backplane, the driver attached to the bus places n-bits of data in parallel onto the bus and all the information is sent at the same time along the backplane. In the case of serial transmission, the data must first be converted to a serial stream to effectively take advantage of the higher

Figure 4. Parellel vs. Serial Transmission



throughputs available. This is called serialization. The serial data is then transmitted at high speed along the line to the receiver, which then de-serializes the information back into the original parallel data. Serialization is used in SERDES devices that have multiple parallel inputs and one/several serial outputs.

LVDS devices can be used in a parallel implementation providing very high-speed point-to-point transmissions.

Advantages of *parallel transmission* include:

- Very high data rates over a short distance
- Only one trace per channel is required
- Normally, there is no software overhead with parallel standards and one bit could be used as a signal flag
- Very fast system reaction time, since the serial word must first be fully received and decoded
- Many industrial and telecom applications already use parallel backplanes. (Many designers and engineers are familiar with these kinds of systems and have the knowledge and experience to quickly implement such systems.)

The advantages of *serial transmission* include:

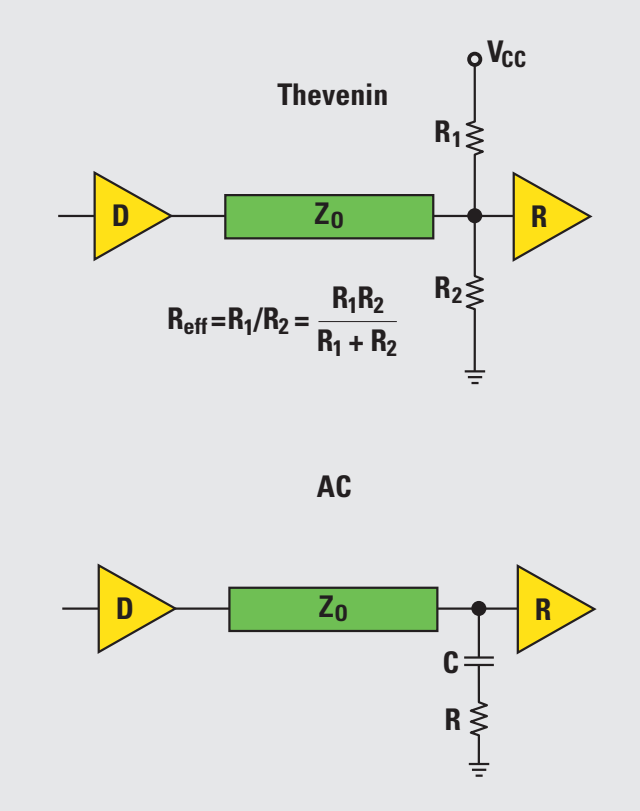
- More flexible approach to data rates allowing longer cable lengths and less expensive cable costs
- Reduction in the number of signal lines and GND lines required to transmit the data from one point to another if SERDES devices are used
- Higher data rate throughput per channel with differential solutions

Advanced Bus Interface Logic

For a long time, TTL busses have been the standard solution for backplane systems. Different logic families are available to fulfill the requirement for backplane busses and the choice for the appropriate logic strongly depended on the physical characteristics of the bus and the required signal integrity. The main factor affecting signal integrity is the number of receiving and transmitting modules connected into that bus. More cards on the backplane with closer spacing will lower the impedance of the bus due to additional capacitive loading (driver and receiver input/output capacitance, printed stub line capacitance and connector capacitance) resulting in the need for a higher drive capability of the logic device.

Mature 5-V TTL and 5-V CMOS as well as 3.3-V CMOS technologies provide a drive capability of 24 mA and can

Figure 5. Typical Termination Models



only handle line impedance down to about 50 ohms. With the introduction of BiCMOS technologies the drive has been enlarged to –32/64 mA (SN74ABTxxx, SN74LVTxxx and SN74ALVTxxx) and with so called incident wave switching drivers (SN74ABT25xxx) it is even possible to drive bus lines with an impedance as low as 25 ohms.

Standard logic devices can be used for either point to point connections or to realize backplane busses, which consists of many drivers and receivers along the bus. Both solutions using standard logic devices are usually set up as parallel busses; up to 36 bits can be switched by one device. The operational frequency can be chosen within a range from a few MHz up to the clock frequency of about 50 MHz, such that the data-throughput per device is in the range of 1 to 2 Gbps. A maximum bus-length is not specified for backplanes; however, in practice, the bus-length of parallel backplanes should not exceed about 50 cm. Typically, Thevenin or AC terminations are used with these types of devices as shown in Figure 5.

Features:

- 4-, 8-, 16- and 32-bit devices enable parallel operation on the backplane/memory bus.
- Boundary scan devices (JTAG - IEEE 1149.1) available in LVT and ABT enable easy testability during design and production. SCOPE™ products are compatible with the IEEE Standard 1149.1-1990 (JTAG) test access port and boundary scan architecture.
- Bus-hold option on data inputs eliminates the need for external pullup resistors.
- 26-ohm series resistor option is included in the output stages to match bus impedance avoiding external resistors and improving signal integrity in point-to-point busses.
- ABT, LVT and ALVT support hot insertion/removal since the power up 3-state outputs prevent bus contention as V_{CC} ramps up or down during insertion or removal.

The slew rate of these devices is about 1.2 to 1.4 V/ns and this higher slew rate causes signal integrity problems in distributed loads like those found in backplanes. This limits their usefulness in many slot multi-point applications and requires reflected wave switching even at lower frequencies. GTLP and VME devices have been optimized for better signal integrity in distributed loads by reducing the slew rate to 0.4 to 0.5 V/ns and designing these devices into a distributed load, not the lumped test load specified in the data sheet. You may think the AC numbers in the GTLP and VME data sheets are non-ideal but this is only because they have to be tested and guaranteed into the typical lumped test load because there is no industry wide distributed test load. However, once these devices are operated in a backplane, they'll prove to be optimized for this environment.

Enhanced Transceiver Logic

Enhanced Transceiver Logic (ETL) features improved noise margins, while maintaining TTL compatible switching levels that enable higher speed in VME backplanes. Typically, Thevenin terminations are used in the standardized 64-bit, 21-slot VME64x backplane of which a typical bit is shown in Figure 6.

VMEbus History

The VMEbus was introduced as backplane bus architecture for industrial and commercial applications in 1981. The data transfer protocols used to define the VMEbus came from the Motorola VERSA bus architecture that owed its heritage to the then, recently introduced, Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data transfer operations: single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous using a master-slave handshake. The master would put address and data onto the bus and wait for an acknowledgment. The selected slave would either read or write data to or from the bus and then provide a data acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbytes/s. Previous to the VMEbus it was not uncommon for backplane busses to require

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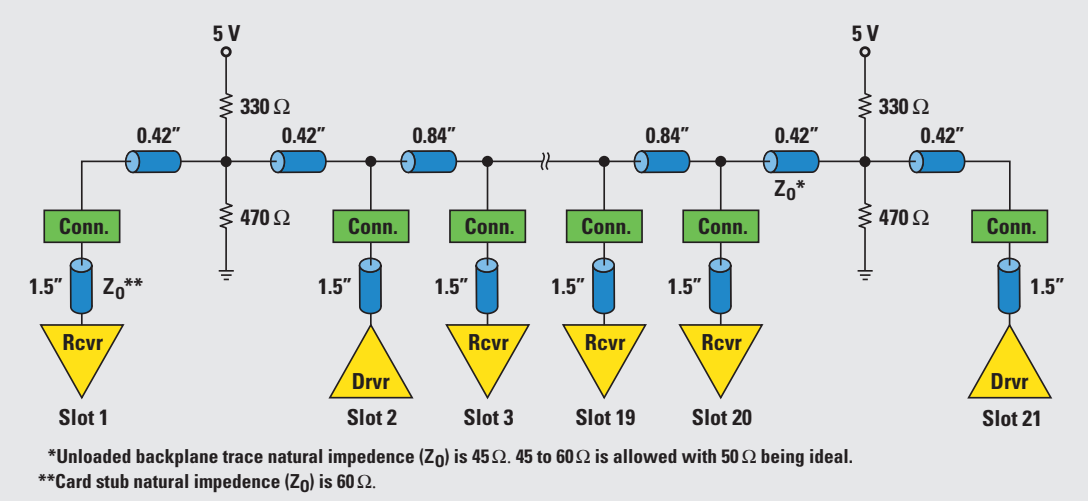
Figure 6. Thevenin Terminations for ETL VME64x Backplane



*Unloaded backplane trace natural impedence (Z_0) is 45 Ω. 45 to 60 Ω is allowed with 50 Ω being ideal.
**Card stub natural impedence (Z_0) is 60 Ω.

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elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems between manufacturers. To make interface design easier and to insure compatibility the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, therefore, doubling the transfer rate as shown in Table 1. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data transfer rates to 320 Mbytes/s or more. The new specification, VITA 1.5 - 199X, double-edge source synchronous transfers (2eSST), is based on the asynchronous 2eVME protocol. It doesn't wait for acknowledgement of the data by the receiver and requires incident wave switching. Sustained data rates of 1 Gbytes/s, more than 10x faster than traditional VME64 backplanes with single-edge signaling are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher frequency operation over the VME64x distributed load backplane. More information on VMEbus can be obtained at **www.vita.com**

Maximum Data Transfer Rates

The SN74VMEH22501 device, which will be released soon, will provide the monotonic incident wave switching needed for the increased data throughput available from the 2eSST protocol. The VME320 backplane approximates a lumped load allowing substantially higher frequency operation over the VMEbus and VME64 distributed load backplanes.

Applicability

The target area for VME backplanes and ETL devices include industrial controls, military, aerospace, transportation, telecommunications, simulations, medical, high energy physics, office automation and instrumentation systems.

Electrical Specifications

ABTE 5-V V_{CC} devices function the same as other TTL devices except for increased noise margin on the ETL (backplane) ports with V_{IH} and V_{IL} ±100 mV around the 1.5-V threshold and the ETL outputs provide –64/+90 mA of drive. The new 3.3-V V_{CC}, 5-V tolerant VME devices will have a V_{IH} and V_{IL} of ±50 mV around the variable $^1/_2$-V_{CC} threshold for better balanced noise margin and ETL outputs of ±48 mA to ensure monotonic incident wave switching.

VME Protocol

The basic single-cycle VMEbus data transfer protocol is very straightforward. The master puts addresses onto the bus, delays a minimum of 35 ns, and then asserts address strobe (AS*). For a write operation, the master puts data onto the bus, delays a minimum of 35 ns, and then asserts one or both of its data strobes (D50* and/or DS1*). All slave cards on the bus monitor the addresses. Each slave is set up to decode a unique address. The assertion of AS* tells the slave that the address is valid. In a write cycle the selected slave must then read data off the bus. The assertion of data strobe tells the slave that data is valid on the bus and can be strobed into memory. The slave then asserts data acknowledge (DTACK*) to signal that the data has been captured.

The 2eVME protocol uses the same asynchronous protocol as the basic single-cycle protocol, but clocks data across the bus on both the rising and falling edges of the data strobes thus gaining a 2x speed up for each cycle. 2eSST on the other hand uses a synchronous protocol that clocks data using DS0* for writes and DTACK* for reads. 2eSST increases the speed of the clocks to speed up the data transfers and requires the use of a backplane that assures monotonic signals, such as provided by the VME320 star backplane.

Features:

- Manufactured using BiCMOS process
- Backplane drive levels necessary for incident wave switching
- Card side data bits feature bus-hold circuitry eliminating the need for external pullup resistors
- Card side data bits feature 26-ohm series output resistors to dampen signal reflections

Table 1. VME Backplane Evolution

Date	Topology	Protocol	Data Bits Per Cycle	Data Transfers Per Clock Cycle	Per System (MBytes/s)	Frequency (MHz)	
						Backplane	Clock
1981	VME bus IEEE-1014	BLT	32	1	40	10	10
1989	VME64	MBLT	64	1	80	10	10
1995	VME64x	2eVME	64	2	160	10	20
1997	VME64x	2eSST	64	2-No Ack	160-320	10-20	20-40
1999	VME320	2eSST	64	2-No Ack	320-1000	20-62.5	40-125

- I_{OFF}, PU/D-3-state, BIAS V_{CC} pin pre-charge and internal pullup resistors on control pins support live insertion/withdrawal
- SN74ABTExxx with the wider noise margin ETL logic levels on the backplane supports the ANSI/VITA 1-1994 specification (VME64) with tight tolerances for transition times and skews
- TI, in conjunction with VITA, is developing the SN74VMEH22501 to support the 2eVME and 2eSST protocol and allow higher data throughput
- Visit **www.ti.com/sc/etl** for information on the ABTE and new VME devices

Backplane Transceiver Logic (SN74FBxxx)

The BTL bus realizes a bus in open collector mode. In this case, the falling edge is actively generated from the driver. Only a low impedance driver can switch the bus with the incident wave in a heavily loaded backplane. The rising edge is generated by the passive pull-up-network. Choosing a pull-up-network with output impedance in the impedance range of the loaded bus-line is the best solution regarding the signal integrity. However, in this case a tremendous low-level-current can be used for one signal-trace. This has been taken into consideration for the backplane transceiver logic circuits. They can handle a current (I_{OL}) up to 100 mA, which equals line impedance of 22 ohms.

Applicability

The target area for BTL devices is the telecom sector, where especially the live insertion capability is mandatory.

Electrical Specifications

The physical layer of the 5-V V_{CC} FutureBus device is called BTL and works with a voltage swing of 1.1 V only using an open collector bus system. The saturation voltage of the pull-down transistor and the forward voltage of the serially connected diode generate the output low level voltage of 1 V. The high level of 2.1 V comes from the termination resistor connected to the termination voltage of 2.1 V. The value of the termination resistor is equal to the impedance of the bus-line and therefore the bus-line is terminated correctly. For safe detection of the logic levels, the inputs are designed with differential amplifiers and a fixed threshold at 1.55 V, exactly in the middle of the voltage swing.

To reduce I_{CC} current spikes, the fall-time is defined to be 2 ns or slower. The rise time is not generated by active electronics, but by the pull-up resistor.

Protocol

FutureBus+ Logical Layer Specification according to the IEEE 896.2 Specification, describing the node management, live insertion and profiles. However, the physical layer may also be used stand-alone without the logical layer.

Features:

- Reduced voltage swing: V_{OL} = 1 V; V_{OH} = 2.1 V generates low switching noise into 11 ohms effective or 22 || 22 ohm line termination resistors
- Matching the pull-up resistor at the line end to the loaded trace impedance avoids line reflections
- Decoupling diode reduces output capacitance to <5 pF increasing line impedance
- Maximum output edge rate 2 ns; trapezoidal waveform reduces system noise
- Supports live insertion/withdrawal with I_{OFF}, PU3S and BIAS V_{CC}

Gunning Transceiver Logic (SN74GTLxxx)

The concept of a Gunning Transceiver Logic (GTL) bus is similar to a BTL system. Because of the missing diode in the open collector/drain outputs (compared to the BTL-solution) the low level is 0.4 V. With a chosen high level of 1.2 V the voltage swing is reduced to only 0.8 V. Again the threshold is set in the middle of the voltage swing at 0.8 V by the external variable input V_{REF} control pin. With GTL output drive capability of up to about 40 mA, the GTL devices are able to drive an effective termination resistor of 0.8 V/40 mA = 20 ohms. If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus is 20 ohms (effectively the driver sees: 40 ohms || 40 ohms = 20 ohms). As a result of the 0.8-V swing and the 40-mA I_{OL} the maximum power dissipation of one output is 16 mW. It is thus possible to integrate these low power drivers into ASICs.

Applicability

The GTL family is designed for a small bus on a board, e.g., between a processor and its memory modules and features a faster edge rate. Because the target application for GTL is not a backplane bus, but a bus on a board, no requirements for hot or live insertion/withdrawal have been included into the specification. GTL1655 is the exception and is a high drive (100 mA), fast edge device that supports live insertion.

Electrical Specifications

The 3.3-V V_{CC}, 5-V tolerant GTL devices support two different logic level specifications: GTL (according to JEDEC Standard JESD8-3) and the GTL+ levels. As already mentioned, GTL V_{TT}/V_{OH} = 1.2 V, V_{IH}/V_{IL} = ±50 mV around the variable V_{REF} threshold that is normally set at 0.8 V. V_{OL} is dependant on the device, trace and effective termination resistance but is normally 0.4 V or below.

Features:

- Differential amplifier guarantees stable threshold voltage of the receiver
- Low voltage swing generates low switching noise and reduces EMI
- High drive capable GTL1655 enables incident wave switching as low as 11 ohms effective or 22 || 22 ohms line termination resistance
- Matching the pull-up resistor at the line end to the loaded trace impedance avoids line reflections
- GTL1655 edge rate control selection input pin (held at V_{CC} or GND) changes the GTL slew rate from a fast to an even faster edge rate to compensate for changes in loading

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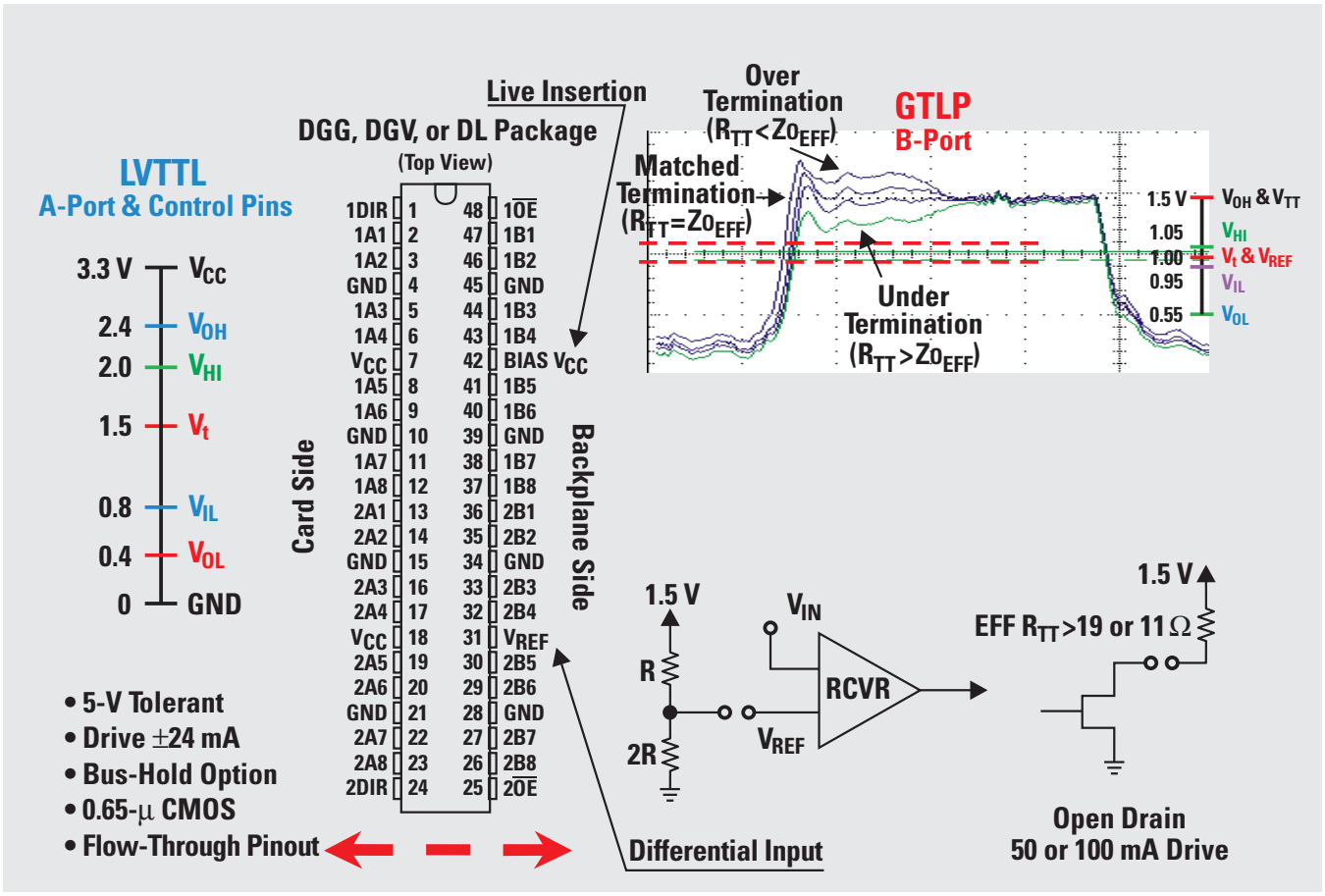
Figure 7. High-Performance Backplane Translator



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Gunning Transceiver Logic Plus (SN74GTLPxxx)

Gunning Transceiver Logic Plus (GTLP) devices are high-speed, high-performance backplane transceivers that operate like the GTL family except for two major differences, they have been optimized with slower edge rates for the distributed loads found in multi-slot backplanes and they support live insertion applications. The GTLP reduced output swing (<1 V), reduced input threshold levels and slower edge rates allow higher backplane frequencies. GTLP devices are functionally and footprint equivalent to common ABT, FCT, LVT, ALVT and FB+ devices but provided an alternative to more complex serial technologies in high data throughput applications.

The GTLP ’16245 type bus transceiver is shown in Figure 7. The key to GTLP’s success in backplane applications is that:

- GTLP outputs are designed into a backplane load, not the typical lumped load, with slower, more controlled edge rates
- Controlled edge rates and reduced voltage swing minimize EMI
- Incident wave switching is guaranteed at any frequency if R_{TT} is close to or less than the effective trace impedance

The differential V_{REF} input and R/2R resistor divider network ensure that the noise margin is not lost if V_{TT} fluctuates during switching operations and provides the designer flexibility in adjusting the switching threshold for unusual situations. Simply change the resistor values to adjust V_{REF} higher or lower.

GTLP offers two different drives, 50- or 100-mA, to allow the designer flexibility in matching the device to backplane length, slot spacing and termination resistor. The medium drive device can drive lines down to 19 ohms (lowest termination resistor that can be driven by the driver in the middle of a bus is 38 ohms—effectively the driver’s load is 38 ohms || 38 ohms = 19 ohms). The high drive devices can drive loads down to 11 ohms (minimum termination resistor for bus configuration will be 22 ohms). It is important to pick a termination resistor that matches the loaded backplane trace impedance for best signal integrity/incident wave switching but that is within the capacity of the driver. High drive devices can be used in place of medium drive devices even with larger termination resistor values (e.g., 75 Ω) without concern although since the medium drive devices are less costly the best drive match for the application would provide the optimum solution.

Table 2. Measured Range of Characteristics for the GTLP EVM

Unloaded (Natural) Trace			Trace and 20 Empty Connectors at 0.94″		Fully Loaded With 20 Cards at .094″		Card C_t (pF)
Z_O (Ω)	T_{PD} (ps/in)	C_O (pF/in)	Z_O (Ω)	t_{PD} (ps/in)	Z_O (Ω)	t_{PD} (ps/in)	
47	164	3.49	39	197	21	371	11.6
94	211	2.24	72	274	34	585	12.1

Loaded trace impedance is a function of natural trace impedance (Z_O), stub length, connector impedance, device impedance and card spacing. The GTLP EVM is constructed like a typical open drain telecom backplane that would look like the double-ended pull-up terminated trace as shown in Figure 8.

The bus is pulled high to the termination voltage (V_{TT} =1.5 V) through the termination resistance (R_{TT} = 22 Ω) when the GTLP open drain device is off and pulled low when GTLP open drain device is on. The advantage of the open drain backplane is that there is no bus contention, it is simple to implement and there is less power consumption than in Thevenin terminated backplanes.

Actual range of measurements from the GTLP EVM is shown in Table 2. It clearly shows that in a heavily loaded backplane the termination resistance should easily go as low as 21 Ω, but is limited to 22 Ω by the GTLP high drive maximum I_{OL} recommendations. Increasing the natural trace impedance can change the termination resistor to a value that is within the capacity of the high-drive devices and better approximate what the medium-drive devices can handle. The down side is that the backplane time of flight will now be about 58% slower. Typical card capacitance will be between 10 and 18 pF depending on device C_{IO} and stub length (stub length being most critical and should always be less than 1 inch).

Applicability

GTLP is used where the major concerns are higher data throughput, live insertion capability, better signal integrity or lower power consumption in parallel backplane architectures.

Electrical Specifications

The GTLP device is optimized at GTLP signal level specifications, but also operates at GTL (according to JEDEC Standard JESD8-3). The GTLP voltage swing is from 1.5 V to 0.55 V with ±50 mV around the variable V_{REF} threshold of 1.0 V, which is the same as GTL+ but is normally referred to as GTLP in these backplane optimized devices. The bus system is identical to the GTL bus with the exception that the edge rate is much slower and the devices have been designed into a distributed load.

Features:

- 3.3-V operation with 5-V tolerant LVTTL inputs/outputs, which allow the devices to act as 5-V TTL-to-GTLP as well as 3.3-V LVTTL-to-GTLP translators.
- Significantly improved Output Edge Control (OEC™) circuitry on the rising and falling edge of the GTLP outputs reduces line reflections, electromagnetic interference (EMI) and improves overall signal integrity allowing clock frequencies in excess of 120 MHz.
- Maximum data frequency is about 60 MHz in system clock and 135 MHz in source synchronous clock mode.
- Fully supports live insertion with I_{OFF}, PU3S and BIAS V_{CC} circuitry.
- Edge Rate Control (ERC) circuitry on high-drive devices allows a slow and a slightly faster edge rate. The slightly faster edge rate will reduce the propagation delay and increase the maximum possible frequency in optimally terminated backplanes.

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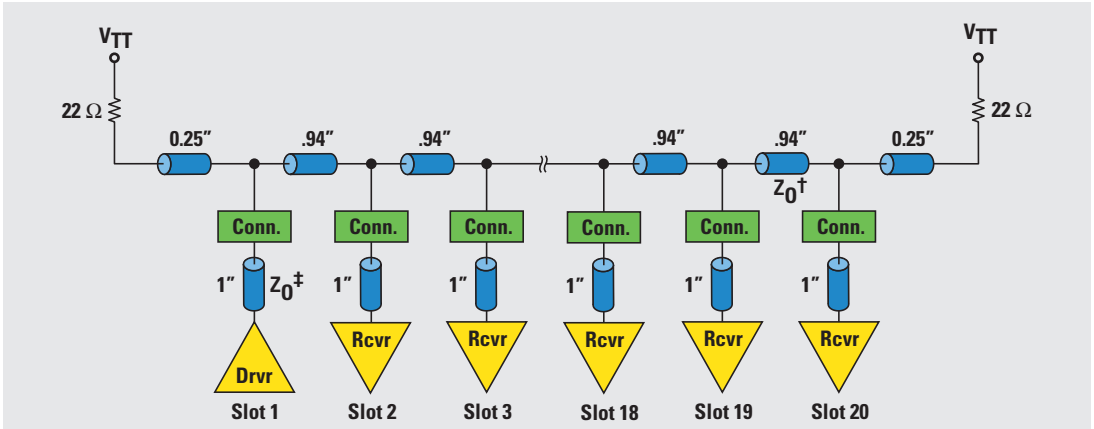
Figure 8. Typical GTLP Backplane



† Unloaded backplane trace natural impedance (Z_O) is 45 Ω. 45 to 60 Ω is allowed with 50 Ω being ideal.
‡ Card stub natural impedance (Z_O) is 60 Ω.

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- CMOS construction for $^1/_3$ the static power consumption of BiCMOS logic devices.
- LVTTL side balanced drive of ±24 mA with optional Bus-hold circuitry.

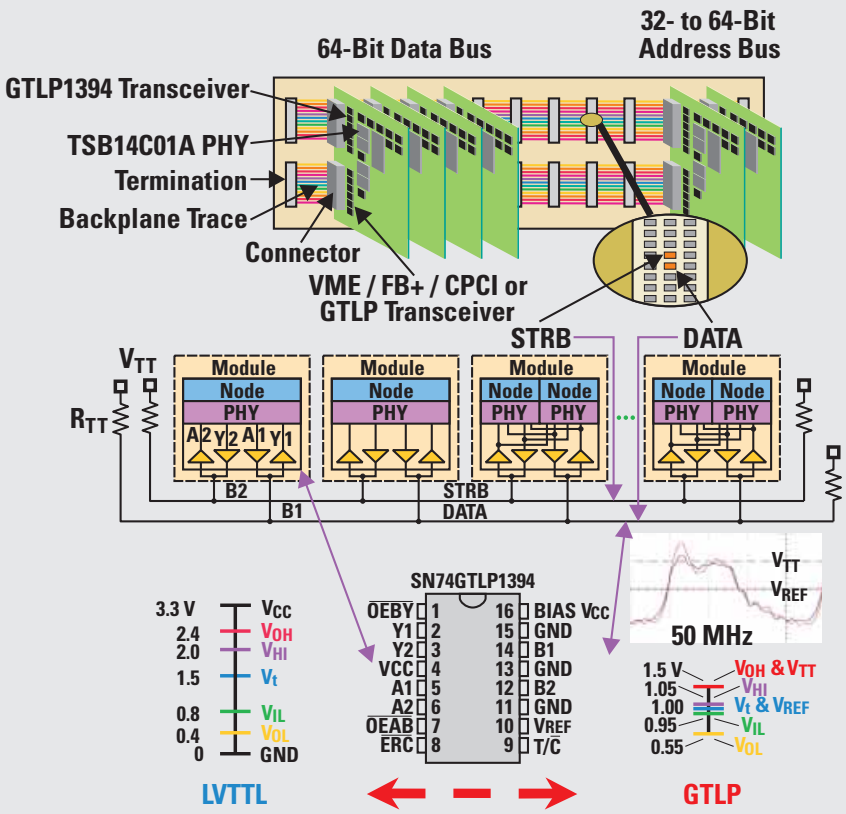
Combined Applications

With many TI devices at their disposal, design engineers can solve data transmission concerns and balance performance with cost, availability and board space constraints.

TI SLL Advanced Bus Interface Logic provide reliable tier 2 performance at a reasonable cost and are available in various packaging options including SOIC, SSOP, TSSOP, TVSOP, VFBGA and LFBGA.

The TSB14C01 1394 backplane PHY and the SN74GTLP1394 shown in Figure 9 are a prime example of how the best of both worlds can be combined in one application. They are used to provide robust 1394 link layer controller signals to each telecom card via a simple and cost effective open drain GTLP bus transceiver. The 1394 backplane PHY in conjunction with the 1394 link layer and microprocessor provides absolute control over each card and is able to monitor and shutdown any card that locks up the system allowing a safe restart and continued operation. Many optical routers are using these devices in this type of implementation. The SN74GTLP1394 provides the means to send the serial data signal and strobe across increasingly wider backplanes with excellent signal integrity even at S100 (50 MHz) speeds. The SN74GTLP1394 is a versatile part that is also being used as a GTLP clock driver and as a precision differential input/LVTTL level translator from a TTL clock via a resistor divider network.

Figure 9. SN74GTLP1394 Backplane Application



- The 1394 backplane serial bus plays a supportive role in backplane systems providing a means for diagnostics, system enhancement and peripheral monitoring.
- Data transfer rates of 50 Mbps (S50) and 100 Mbps (S100) supported by GTLP at 25- or 50-MHz frequencies.
- Edge rates are optimized for high-performance multi-slot parallel backplane applications.
- More cost effective and easier to implement than more complex LVDS solutions.
- Better signal integrity and more cost effective than existing FB+ solutions.

SN74GTLP1394 main features include:

- LVTTL-to-GTLP bi-directional translator
- High GTLP drive (100 mA)
- TI-OPC™ overshoot protection circuitry
- BIAS V_{CC} supports true live insertion
- 3.3-V V_{CC} with 5-V tolerance
- 16-pin SOIC (D&DR), TSSOP (PWR) and TVSOP (DGVR) packages

Product Selection Guide

ABT

Device	No. Pins	Description	Availability							
			MIL	PDIP	QFP	SOIC	SSOP	TQFP	TSSOP	TVSOP
SN74ABT125	14	Quad Bus Buffers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT126	14	Quad Bus Buffers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT240A	20	Octal Buffers/Drivers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT241	20	Octal Buffers/Drivers with 3-State Outputs	✓							
SN74ABT241A	20	Octal Buffers/Drivers with 3-State Outputs		✓		✓	✓		✓	
SN54ABT244	20	Octal Buffers and Line Drivers with 3-State Outputs	✓							
SN74ABT244A	20	Octal Buffers and Line Drivers with 3-State Outputs		✓		✓	✓		✓	✓
SN74ABT245A	20	Octal Bus Transceivers with 3-State Outputs	✓							
SN74ABT245B	20	Octal Bus Transceivers with 3-State Outputs		✓		✓	✓		✓	✓
SN74ABTH245	20	Octal Bus Transceivers with 3-State Outputs	✓	✓		✓	✓		✓	✓
SN74ABT273	20	Octal D-Type Flip-Flops with Clear	✓	✓		✓	✓		✓	✓
SN74ABT373	20	Octal Transparent D-Type Latches with 3-State Outputs	✓	✓		✓	✓		✓	
SN54ABT374	20	Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs	✓							
SN74ABT374A	20	Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs		✓		✓	✓		✓	
SN74ABT377	20	Octal D-Type Flip-Flops with Enable	✓							
SN74ABT377A	20	Octal D-Type Flip-Flops with Enable	✓	✓		✓	✓		✓	
SN74ABT533	20	Octal Inverting Transparent Latches with 3-State Outputs	✓							
SN74ABT533A	20	Octal Inverting Transparent Latches with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT534	20	Octal D-Type Inverting Flip-Flops with 3-State Outputs	✓							
SN74ABT534A	20	Octal D-Type Inverting Flip-Flops with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT540	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs		✓		✓	✓		✓	
SN54ABT541	20	Octal Buffers and Line Drivers with 3-State Outputs	✓							
SN74ABT541B	20	Octal Buffers and Line Drivers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT543	24	Octal Registered Transceivers with 3-State Outputs	✓							
SN74ABT543A	24	Octal Registered Transceivers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT573	20	Octal Transparent D-Type Latches with 3-State Outputs	✓							
SN74ABT573A	20	Octal Transparent D-Type Latches with 3-State Outputs	✓	✓		✓	✓		✓	
SN54ABT574	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓							
SN74ABT574A	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT620	20	Octal Bus Transceivers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT623	20	Octal Bus Transceivers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT640	20	Octal Bus Transceivers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT646A	24	Octal Registered Bus Transceivers with 3-State Outputs	✓	✓		✓	✓		✓	✓
SN74ABT651	24	Octal Bus Transceivers and Registers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT652A	24	Octal Bus Transceivers and Registers with 3-State Outputs	✓	✓		✓	✓		✓	✓
SN74ABT657A	24	Octal Bus Transceivers with Parity Generators/Checkers and 3-State Outputs		✓		✓	✓		✓	
SN54ABT821	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs	✓							
SN74ABT821A	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT823	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT827	24	10-Bit Buffers/Drivers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT833	24	8-Bit to 9-Bit Parity Bus Transceivers	✓	✓		✓	✓		✓	
SN74ABT841	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs	✓							
SN74ABT841A	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs		✓		✓	✓		✓	
SN74ABT843	24	9-Bit Bus-Interface D-Type Latches with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT853	24	8-Bit to 9-Bit Parity Bus Transceivers	✓	✓		✓	✓		✓	
SN74ABT861	24	10-Bit Transceivers with 3-State Outputs		✓		✓				
SN74ABT863	24	9-Bit Bus Transceivers with 3-State Outputs		✓		✓	✓		✓	
SN74ABT2240A	20	Octal Buffers and Line/MOS Drivers with Series Damping Resistors and 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT2241	20	Octal Buffers and Line/MOS Drivers with Series Damping Resistors and 3-State Outputs		✓		✓	✓		✓	
SN74ABT2244A	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT2245	20	Octal Transceivers and Line MOS Drivers with Series Damping Resistors and 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABTR2245	20	Octal Transceivers and Line MOS Drivers with Series Damping Resistors and 3-State Outputs		✓		✓	✓		✓	✓

✓ = Now + = Planned

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ABT *(continued from previous page)*

Device	No. Pins	Description	Availability							
			MIL	PDIP	QFP	SOIC	SSOP	TQFP	TSSOP	TVSOP
SN74ABT2827	24	10-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs		✓		✓	✓		✓	
SN74ABT2952A	24	Octal Bus Transceivers and Registers with 3-State Outputs	✓	✓		✓	✓		✓	
SN74ABT5400A	28	11-Bit Line/Memory Drivers with 3-State Outputs				✓				
SN74ABT5401	28	11-Bit Line/Memory Drivers with 3-State Outputs				✓				
SN74ABT5402A	28	12-Bit Line/Memory Drivers with 3-State Outputs				✓				
SN74ABT5403	28	12-Bit Line/Memory Drivers with 3-State Outputs				✓				
SN54ABT16240	48	16-Bit Buffers/Drivers with 3-State Outputs	✓							
SN74ABT16240A	48	16-Bit Buffers/Drivers with 3-State Outputs	✓				✓		✓	✓
SN74ABT16241A	48	16-Bit Buffers/Drivers with 3-State Outputs	✓				✓		✓	✓
SN74ABT16244A	48	16-Bit Buffers/Drivers with 3-State Outputs					✓		✓	✓
SN74ABTH16244	48	16-Bit Buffers/Drivers with 3-State Outputs	✓				✓		✓	✓
SN74ABT16245A	48	16-Bit Bus Transceivers with 3-State Outputs					✓		✓	✓
SN74ABTH16245	48	16-Bit Bus Transceivers with 3-State Outputs	✓				✓		✓	✓
SN74ABTH16260	56	12-Bit to 24-Bit Multiplexed D-Type Latches with 3-State Outputs	✓				✓			
SN74ABT16373A	48	16-Bit Transparent D-Type Latches with 3-State Outputs	✓				✓		✓	✓
SN74ABT16374A	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓				✓		✓	✓
SN74ABTH16460	56	4-to-1 Multiplexed/Demultiplexed Transceivers with 3-State Outputs					✓		✓	
SN74ABT16470	56	16-Bit Registered Transceivers with 3-State Outputs					✓		✓	
SN74ABT16500B	56	18-Bit Universal Bus Transceivers with 3-State Outputs					✓		✓	
SN74ABT16501	56	18-Bit Universal Bus Transceivers with 3-State Outputs					✓		✓	
SN74ABT16540A	48	16-Bit Buffers/Drivers with 3-State Outputs					✓		✓	✓
SN74ABT16541A	48	16-Bit Buffers/Drivers with 3-State Outputs					✓		✓	✓
SN74ABT16543	56	16-Bit Registered Transceivers with 3-State Outputs	✓				✓		✓	✓
SN74ABTH16543	56	16-Bit Registered Transceivers with 3-State Outputs					✓		✓	✓
SN74ABT16600	56	18-Bit Universal Bus Transceivers with 3-State Outputs					✓		✓	
SN74ABT16601	56	18-Bit Universal Bus Transceivers with 3-State Outputs	✓				✓		✓	
SN74ABT16623	48	16-Bit Bus Transceivers with 3-State Outputs					✓		✓	
SN74ABT16640	48	16-Bit Bus Transceivers with 3-State Outputs	✓				✓		✓	
SN74ABT16646	56	16-Bit Bus Transceivers and Registers with 3-State Outputs	✓				✓		✓	
SN74ABT16652	56	16-Bit Bus Transceivers and Registers with 3-State Outputs	✓				✓			
SN74ABT16657	56	16-Bit Transceivers with Parity Generators/Checkers and 3-State Outputs					✓		✓	✓
SN74ABT16821	56	20-Bit D-Type Flip-Flops with 3-State Outputs					✓		✓	
SN74ABT16823	56	18-Bit D-Type Flip-Flops with 3-State Outputs	✓				✓		✓	✓
SN74ABTH16823	56	18-Bit D-Type Flip-Flops with 3-State Outputs					✓		✓	
SN74ABT16825	56	18-Bit Buffers/Drivers with 3-State Outputs					✓			
SN74ABT16833	56	Dual 8-Bit to 9-Bit Parity Bus Transceivers					✓		✓	✓
SN74ABT16841	56	20-Bit Bus-Interface D-Type Latches with 3-State Outputs	✓				✓			
SN74ABT16843	56	18-Bit Bus-Interface D-Type Latches with 3-State Outputs					✓		✓	
SN74ABT16853	56	Dual 8-Bit to 9-Bit Parity Bus Transceivers					✓		✓	
SN74ABT16863	56	18-Bit Bus-Interface Transceivers with 3-State Outputs					✓			
SN74ABT16952	56	16-Bit Registered Transceivers with 3-State Outputs	✓				✓		✓	✓
SN74ABTH25245	24	25-Ohm Octal Bus Transceivers with 3-State Outputs		✓		✓				
SN74ABTH32245	100	32-Bit Bus Transceivers with 3-State Outputs						✓		
SN74ABTH32316	80	16-Bit Tri-Port Universal Bus Exchangers	✓		✓					
SN74ABTH32318	80	18-Bit Tri-Port Universal Bus Exchangers			✓					
SN74ABTH32501	100	32-Bit Universal Bus Transceivers with 3-State Outputs						✓		
SN74ABTH32543	100	32-Bit Registered Bus Transceivers with 3-State Outputs						✓		
SN74ABT162244	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs	✓				✓		✓	✓
SN74ABT162245	48	16-Bit Bus Transceivers with Series Damping Resistors and 3-State Outputs	✓				✓		✓	✓
SN74ABTH162245	48	16-Bit Bus Transceivers with Series Damping Resistors and 3-State Outputs					✓		✓	✓
SN74ABTH162260	56	12-Bit to 24-Bit Multiplexed D-Type Latches with Series Damping Resistors and 3-State Outputs					✓			

✓ = Now + = Planned

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Device	No. Pins	Description	Availability							
			MIL	PDIP	QFP	SOIC	SSOP	TQFP	TSSOP	TVSOP
SN74ABTH162460	56	4-to-1 Multiplexed/Demultiplexed Registered Transceivers with 3-State Outputs					✓		✓	✓
SN74ABT162500	56	18-Bit Universal Bus Transceivers with 3-State Outputs					✓			
SN74ABT162501	56	18-Bit Universal Bus Transceivers with 3-State Outputs					✓		✓	
SN74ABT162601	56	18-Bit Universal Bus Transceivers with 3-State Outputs	✓				✓		✓	
SN74ABT162823A	56	18-Bit Bus-Interface Flip-Flops with 3-State Outputs					✓		✓	
SN74ABT162825	56	18-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs					✓			
SN74ABT162827A	56	20-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs					✓		✓	✓
SN74ABT162841	56	20-Bit Bus-Interface D-Type Latches with 3-State Outputs					✓		✓	

ABTE/ETL

Device	No. Pins	Description	Availability		
			MIL	SSOP	TSSOP
SN74ABTE16245	48	16-Bit Incident-Wave-Switching Bus Transceivers with 3-State Outputs	✓	✓	✓
SN74ABTE16246	48	11-Bit Incident-Wave-Switching Bus Transceivers with 3-State and Open-Collector Outputs		✓	✓

ALVT

Device	No. Pins	Description	Availability			
			LFBGA	SSOP	TSSOP	TVSOP
SN74ALVTH16240	48	16-Bit Buffers/Drivers with 3-State Outputs		✓	✓	✓
SN74ALVTH16244	48	16-Bit Buffers/Drivers with 3-State Outputs		✓	✓	✓
SN74ALVTH16245	48	16-Bit Bus Transceivers with 3-State Outputs		+	+	+
SN74ALVTHR16245	48	16-Bit Bus Transceivers with I/O Series Damping Resistors and 3-State Outputs		+	+	+
SN74ALVTH16260	56	12-Bit to 24-Bit Multiplexed D-Type Latches with 3-State Outputs		+	+	+
SN74ALVTH16373	48	16-Bit Transparent D-Type Latches with 3-State Outputs		✓	✓	✓
SN74ALVTH16374	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs		✓	✓	✓
SN74ALVTH16500	56	18-Bit Universal Bus Transceivers with 3-State Outputs		+	+	+
SN74ALVTH16501	56	18-Bit Universal Bus Transceivers with 3-State Outputs		+	+	+
SN74ALVTH16543	56	16-Bit Registered Transceivers with 3-State Outputs		+	+	+
SN74ALVTH16601	56	18-Bit Universal Bus Transceivers with 3-State Outputs		✓	✓	✓
SN74ALVTH16646	56	16-Bit Bus Transceivers and Registers with 3-State Outputs		+	+	+
SN74ALVTH16652	56	16-Bit Bus Transceivers and Registers with 3-State Outputs		+	+	+
SN74ALVTH16721	56	20-Bit D-Type Flip-Flops with 3-State Outputs		+	+	+
SN74ALVTH16821	56	20-Bit D-Type Flip-Flops with 3-State Outputs		✓	✓	✓
SN74ALVTH16827	56	20-Bit Buffers/Drivers with 3-State Outputs		✓	✓	✓
SN74ALVTH16841	56	20-Bit Bus Interface D-Type Latches with 3-State Outputs		+	+	+
SN74ALVTH32244	96	32-Bit Buffers/Drivers with 3-State Outputs	✓			
SN74ALVTH32373	96	32-Bit Transparent D-Type Latches with 3-State Outputs	✓			
SN74ALVTH32374	96	32-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓			
SN74ALVTH162244	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs		✓	✓	✓
SN74ALVTH162245	48	16-Bit Bus Transceivers with Series Damping Resistors and 3-State Outputs		+	+	+
SN74ALVTH162827	56	20-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs		✓	✓	✓

FB+/BTL

Device	No. Pins	Description	Availability		
			MIL	QFP	TQFP
SN74FB1650	100	18-Bit TTL/BTL Universal Storage Transceivers			✓
SN74FB1651	100	17-Bit TTL/BTL Universal Storage Transceivers with Buffered Clock Lines			✓
SN74FB1653	100	17-Bit LVTTL/BTL Universal Storage Transceivers with Buffered Clock Lines			✓
SN74FB2031	52	9-Bit TTL/BTL Address/Data Transceivers	✓	✓	
SN74FB2032	52	9-Bit TTL/BTL Competition Transceivers		✓	
SN74FB2033A	52	8-Bit TTL/BTL Registered Transceivers	✓	✓	
SN74FB2033K	52	8-Bit TTL/BTL Registered Transceivers		✓	
SN74FB2040	52	8-Bit TTL/BTL Transceivers	✓	✓	
SN74FB2041A	52	7-Bit TTL/BTL Transceivers		✓	

✓ = Now + = Planned

FCT

Device	No. Pins	Description	Availability				
			MIL	PDIP	SOIC	SSOP	TSSOP
CY29FCT52CT	24	Octal Registered Transceivers with 3-State Outputs			✓	✓	
CY74FCT138AT	16	1-of-8 Decoders			✓	✓	
CY74FCT138CT	16	1-of-8 Decoders	✓		✓	✓	
CY74FCT138T	16	1-of-8 Decoders				✓	
CY74FCT157AT	16	Quad 2-Input Multiplexers			✓	✓	
CY74FCT157CT	16	Quad 2-Input Multiplexers			✓	✓	
CY74FCT163CT	16	Synchronous 4-Bit Binary Counters			✓	✓	
CY74FCT163T	16	Synchronous 4-Bit Binary Counters	✓				
CY74FCT191AT	16	Presettable Synchronous 4-Bit Up/Down Binary Counters			✓		
CY74FCT191CT	16	Presettable Synchronous 4-Bit Up/Down Binary Counters			✓	✓	
CD74FCT240	20	Octal Buffers/Drivers with 3-State Outputs		✓	✓		
CY74FCT240AT	20	Octal Buffers/Drivers with 3-State Outputs	✓		✓	✓	
CY74FCT240CT	20	Octal Buffers/Drivers with 3-State Outputs			✓	✓	
CY74FCT240T	20	Octal Buffers/Drivers with 3-State Outputs			✓	✓	
CD74FCT244	20	Octal Buffers and Line Drivers with 3-State Outputs		✓	✓		
CD74FCT244AT	20	Octal Buffers and Line Drivers with 3-State Outputs		✓			
CY74FCT244AT	20	Octal Buffers and Line Drivers with 3-State Outputs	✓	✓	✓		
CY74FCT244CT	20	Octal Buffers and Line Drivers with 3-State Outputs	✓		✓	✓	
CY74FCT244DT	20	Octal Buffers and Line Drivers with 3-State Outputs			✓	✓	
CY74FCT244T	20	Octal Buffers and Line Drivers with 3-State Outputs	✓		✓	✓	
CD74FCT245	20	Octal Bus Transceivers with 3-State Outputs		✓	✓		
CY74FCT245AT	20	Octal Bus Transceivers with 3-State Outputs	✓	✓	✓	✓	
CY74FCT245CT	20	Octal Bus Transceivers with 3-State Outputs	✓		✓	✓	
CY74FCT245DT	20	Octal Bus Transceivers with 3-State Outputs				✓	
CY74FCT245T	20	Octal Bus Transceivers with 3-State Outputs	✓		✓	✓	
CY74FCT257AT	16	Quad 1-of-2 Data Selectors/Multiplexers with 3-State Outputs				✓	
CY74FCT257CT	16	Quad 1-of-2 Data Selectors/Multiplexers with 3-State Outputs			✓	✓	
CY74FCT257T	16	Quad 1-of-2 Data Selectors/Multiplexers with 3-State Outputs				✓	
CD74FCT273	20	Octal D-Type Flip-Flops with Clear		✓	✓		
CY74FCT273AT	20	Octal D-Type Flip-Flops with Clear	✓		✓	✓	
CY74FCT273CT	20	Octal D-Type Flip-Flops with Clear			✓	✓	
CY74FCT273T	20	Octal D-Type Flip-Flops with Clear			✓	✓	
CD74FCT373	20	Octal Transparent D-Type Latches with 3-State Outputs		✓	✓		
CY74FCT373AT	20	Octal Transparent D-Type Latches with 3-State Outputs	✓		✓	✓	
CY74FCT373CT	20	Octal Transparent D-Type Latches with 3-State Outputs			✓	✓	
CY74FCT373T	20	Octal Transparent D-Type Latches with 3-State Outputs			✓		
CD74FCT374	20	Octal Transparent D-Type Latches with 3-State Outputs		✓	✓		
CY74FCT374AT	20	Octal Transparent D-Type Latches with 3-State Outputs	✓	✓	✓	✓	
CY74FCT374CT	20	Octal Transparent D-Type Latches with 3-State Outputs	✓		✓	✓	
CY74FCT374T	20	Octal Transparent D-Type Latches with 3-State Outputs	✓		✓	✓	
CY74FCT377AT	20	Octal D-Type Flip-Flops with Enable			✓	✓	
CY74FCT377CT	20	Octal D-Type Flip-Flops with Enable	✓		✓	✓	
CY74FCT377T	20	Octal D-Type Flip-Flops with Enable				✓	
CY74FCT399AT	16	Quad 2-Input Multiplexers with Storage			✓		
CY74FCT399CT	16	Quad 2-Input Multiplexers with Storage			✓		
CY74FCT480AT	24	Dual 8-Bit Parity Generators/Checkers		✓		✓	
CY74FCT480BT	24	Dual 8-Bit Parity Generators/Checkers	✓	✓	✓	✓	
CY29FCT520AT	24	8-Bit Multi-Level Pipeline Registers		✓	✓		
CY29FCT520BT	24	8-Bit Multi-Level Pipeline Registers			✓		
CY29FCT520CT	24	8-Bit Multi-Level Pipeline Registers			✓		
CD74FCT540	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs		✓	✓		
CY74FCT540CT	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs				✓	
CD74FCT541	20	Octal Buffers and Line Drivers with 3-State Outputs		✓	✓		
CY74FCT541AT	20	Octal Buffers and Line Drivers with 3-State Outputs		✓	✓	✓	
CY74FCT541CT	20	Octal Buffers and Line Drivers with 3-State Outputs			✓	✓	
CY74FCT541T	20	Octal Buffers and Line Drivers with 3-State Outputs			✓		
CD74FCT543	24	Octal Registered Transceivers with 3-State Outputs		✓	✓		
CY74FCT543AT	24	Octal Registered Transceivers with 3-State Outputs			✓	✓	
CY74FCT543CT	24	Octal Registered Transceivers with 3-State Outputs			✓	✓	

✓ = Now + = Planned

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Device	No. Pins	Description	Availability				
			MIL	PDIP	SOIC	SSOP	TSSOP
CY74FCT543T	24	Octal Registered Transceivers with 3-State Outputs	✓		✓	✓	
CD74FCT564	20	Octal Inverting D-Type Flip-Flops with 3-State Outputs		✓	✓		
CD74FCT573	20	Octal Transparent D-Type Latches with 3-State Outputs		✓	✓	✓	
CD74FCT573AT	20	Octal Transparent D-Type Latches with 3-State Outputs		✓			
CY74FCT573AT	20	Octal Transparent D-Type Latches with 3-State Outputs		✓	✓	✓	
CY74FCT573CT	20	Octal Transparent D-Type Latches with 3-State Outputs			✓	✓	
CY74FCT573T	20	Octal Transparent D-Type Latches with 3-State Outputs			✓	✓	
CD74FCT574	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs		✓	✓		
CY74FCT574AT	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓		✓	✓	
CY74FCT574CT	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs			✓	✓	
CY74FCT574T	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs			✓	✓	
CD74FCT623	20	Octal Bus Transceivers with 3-State Outputs			✓		
CY74FCT646AT	24	Octal Registered Bus Transceivers with 3-State Outputs			✓	✓	
CY74FCT646CT	24	Octal Registered Bus Transceivers with 3-State Outputs	✓		✓	✓	
CY74FCT646T	24	Octal Registered Bus Transceivers with 3-State Outputs			✓	✓	
CY74FCT652AT	24	Octal Bus Transceivers and Registers with 3-State Outputs			✓	✓	
CY74FCT652CT	24	Octal Bus Transceivers and Registers with 3-State Outputs			✓	✓	
CY74FCT652T	24	Octal Bus Transceivers and Registers with 3-State Outputs				✓	
CY29FCT818AT	24	Diagnostic Scan Registers	✓				
CY29FCT818CT	24	Diagnostic Scan Registers		✓	✓	✓	
CD74FCT821A	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓	✓		
CY74FCT821AT	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs			✓	✓	
CY74FCT821BT	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓	✓		
CY74FCT821CT	24	10-Bit Bus-Interface Flip-Flops with 3-State Outputs			✓	✓	
CD74FCT822A	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓			
CD74FCT823A	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓			
CY74FCT823AT	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓	✓	✓	
CY74FCT823BT	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓			
CY74FCT823CT	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs			✓	✓	
CD74FCT824A	24	9-Bit Bus-Interface Flip-Flops with 3-State Outputs		✓			
CY74FCT825CT	24	8-Bit Bus-Interface Flip-Flops with 3-State Outputs				✓	
CY74FCT827AT	24	10-Bit Buffers/Drivers with 3-State Outputs			✓	✓	
CY74FCT827CT	24	10-Bit Buffers/Drivers with 3-State Outputs			✓	✓	
CD74FCT841A	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs		✓	✓		
CY74FCT841AT	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs	✓		✓		
CY74FCT841BT	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs		✓			
CY74FCT841CT	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs			✓	✓	
CD74FCT842A	24	10-Bit Bus-Interface D-Type Latches with 3-State Outputs			✓		
CD74FCT843A	24	9-Bit Bus-Interface D-Type Latches with 3-State Outputs			✓		
CD74FCT844A	24	9-Bit Transparent Latches with 3-State Outputs		✓			
CY74FCT2240AT	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2240CT	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2240T	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs			✓		
CY74FCT2244AT	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2244CT	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2244T	20	Octal Buffers/Line Drivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2245AT	20	Octal Bus Transceivers with Series Damping Resistors and 3-State Outputs		✓	✓	✓	
CY74FCT2245CT	20	Octal Bus Transceivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2245T	20	Octal Bus Transceivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2257AT	16	Quad 1-of-2 Data Selectors/Multiplexers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2257CT	16	Quad 1-of-2 Data Selectors/Multiplexers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2373AT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2373CT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2373T	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2374AT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2374CT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2374T	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓		

✓ = Now + = Planned

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Device	No. Pins	Description	Availability				
			MIL	PDIP	SOIC	SSOP	TSSOP
CY74FCT2541AT	20	Octal Line Drivers/MOS Drivers with 3-State Outputs			✓	✓	
CY74FCT2541CT	20	Octal Line Drivers/MOS Drivers with 3-State Outputs			✓	✓	
CY74FCT2541T	20	Octal Line Drivers/MOS Drivers with 3-State Outputs			✓	✓	
CY74FCT2543AT	24	Octal Registered Transceivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2543CT	24	Octal Registered Transceivers with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2543T	24	Octal Registered Transceivers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2573AT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2573CT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2573T	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓		
CY74FCT2574AT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2574CT	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓	✓	
CY74FCT2574T	20	Octal Transparent D-Type Latches with Series Damping Resistors and 3-State Outputs			✓		
CY74FCT2646AT	24	Octal Registered Bus Transceivers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2646CT	24	Octal Registered Bus Transceivers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2652AT	24	Octal Bus Transceivers and Registers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2652CT	24	Octal Bus Transceivers and Registers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2827AT	24	10-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				✓	
CY74FCT2827CT	24	10-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				✓	
CD74FCT2952A	24	Octal Bus Transceivers and Registers with 3-State Outputs			✓		
CY74FCT16240AT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT16240ET	48	16-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT16244AT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16244CT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16244ET	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16244T	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16245AT	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT16245CT	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT16245ET	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT16245T	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT16373AT	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT16373CT	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT16373ET	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT16374AT	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT16374CT	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT16374ET	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT16374T	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	
CY74FCT16500CT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT16501AT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	
CY74FCT16501ET	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT16543AT	56	16-Bit Registered Transceivers with 3-State Outputs					+
CY74FCT16543CT	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT16543ET	56	16-Bit Registered Transceivers with 3-State Outputs				+	+
CY74FCT16543T	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT16646AT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16646CT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16646ET	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16646T	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16652AT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16652CT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT16652ET	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT16823AT	56	18-Bit D-Type Flip-Flops with 3-State Outputs					+
CY74FCT16823CT	56	18-Bit D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT16823ET	56	18-Bit D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT16827AT	56	20-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT16827CT	56	20-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16827ET	56	20-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT16841AT	56	20-Bit Bus-Interface D-Type Latches with 3-State Outputs				+	

✓ = Now + = Planned

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Device	No. Pins	Description	Availability				
			MIL	PDIP	SOIC	SSOP	TSSOP
CY74FCT16841CT	56	20-Bit Bus-Interface D-Type Latches with 3-State Outputs				+	
CY74FCT16952AT	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT16952CT	56	16-Bit Registered Transceivers with 3-State Outputs					+
CY74FCT16952ET	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT162240CT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162240ET	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162244AT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162244CT	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162244ET	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162244T	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162H244AT	48	16-Bit Buffers/Drivers with Bus Hold and 3-State Outputs					+
CY74FCT162H244CT	48	16-Bit Buffers/Drivers with Bus Hold and 3-State Outputs				+	
CY74FCT162H244ET	48	16-Bit Buffers/Drivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162245AT	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT162245CT	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT162245ET	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT162245T	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT162H245AT	48	16-Bit Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162H245CT	48	16-Bit Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162H245ET	48	16-Bit Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162373AT	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT162373CT	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT162373ET	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT162374AT	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT162374CT	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT162374ET	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT162374T	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	
CY74FCT162500AT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	
CY74FCT162500CT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	
CY74FCT162501AT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT162501CT	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT162501ET	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT162H501CT	56	18-Bit Universal Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162H501ET	56	18-Bit Universal Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT162543AT	56	16-Bit Registered Transceivers with 3-State Outputs					+
CY74FCT162543CT	56	16-Bit Registered Transceivers with 3-State Outputs				+	+
CY74FCT162543ET	56	16-Bit Registered Transceivers with 3-State Outputs				+	+
CY74FCT162543T	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT162H543CT	56	16-Bit Registered Transceivers with Bus Hold and 3-State Outputs					+
CY74FCT162646AT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT162646CT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT162646ET	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT162652AT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	
CY74FCT162652CT	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT162652ET	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT162823AT	56	18-Bit D-Type Flip-Flops with 3-State Outputs					+
CY74FCT162823CT	56	18-Bit D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT162823ET	56	18-Bit D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT162827AT	56	20-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT162827BT	56	20-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT162827CT	56	20-Bit Buffers/Drivers with 3-State Outputs					+
CY74FCT162827ET	56	20-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT162841CT	56	20-Bit Bus-Interface D-Type Latches with 3-State Outputs				+	+
CY74FCT162952AT	56	16-Bit Registered Transceivers with 3-State Outputs					+
CY74FCT162952BT	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT162952ET	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT162H952AT	56	16-Bit Registered Transceivers with Bus Hold and 3-State Outputs					+
CY74FCT162H952CT	56	16-Bit Registered Transceivers with Bus Hold and 3-State Outputs				+	
CY74FCT162H952ET	56	16-Bit Registered Transceivers with Bus Hold and 3-State Outputs					+
CY74FCT163244A	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+
CY74FCT163244C	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+

✓ = Now + = Planned

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Device	No. Pins	Description	Availability				
			MIL	PDIP	SOIC	SSOP	TSSOP
CY74FCT163H244C	48	16-Bit Buffers/Drivers with Bus Hold and 3-State Outputs				+	+
CY74FCT163245A	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT163245C	48	16-Bit Bus Transceivers with 3-State Outputs				+	+
CY74FCT163H245A	48	16-Bit Bus Transceivers with Bus Hold and 3-State Outputs				+	
CY74FCT163H245C	48	16-Bit Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT163373C	48	16-Bit Transparent D-Type Latches with 3-State Outputs				+	+
CY74FCT163374A	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs					+
CY74FCT163374C	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs				+	+
CY74FCT163H374C	48	16-Bit Edge-Triggered D-Type Flip-Flops with Bus Hold and 3-State Outputs				+	+
CY74FCT163500A	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	
CY74FCT163500C	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT163501C	56	18-Bit Universal Bus Transceivers with 3-State Outputs				+	+
CY74FCT163H501C	56	18-Bit Universal Bus Transceivers with Bus Hold and 3-State Outputs				+	+
CY74FCT163543A	56	16-Bit Registered Transceivers with 3-State Outputs				+	
CY74FCT163543C	56	16-Bit Registered Transceivers with 3-State Outputs				+	+
CY74FCT163646C	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT163652A	56	16-Bit Bus Transceivers and Registers with 3-State Outputs					+
CY74FCT163652C	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				+	+
CY74FCT163827A	56	20-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT163827C	56	20-Bit Buffers/Drivers with 3-State Outputs				+	
CY74FCT163952C	56	16-Bit Registered Transceivers with 3-State Outputs				+	+
CY74FCT163H952C	56	16-Bit Registered Transceivers with Bus Hold and 3-State Outputs				+	+

GTL

Device	No. Pins	Description	Availability		
			MIL	SSOP	TSSOP
SN74GTL1655	64	16-Bit LVTTL-to-GTL/GTLP Universal Bus Transceivers with Live Insertion			✓
SN54GTL16612	56	18-Bit LVTTL-to-GTL/GTLP Universal Bus Transceivers	✓		
SN74GTL16616	56	17-Bit LVTTL-to-GTL/GTLP Universal Bus Transceivers with Buffered Clock Outputs		✓	✓
SN74GTL16622A	64	18-Bit LVTTL-to-GTL/GTLP Registered Bus Transceivers			✓
SN74GTL16923	64	18-Bit LVTTL-to-GTL/GTLP Registered Bus Transceivers			✓

GTLP

Device	No. Pins	Description	Availability				
			LFBGA	SOIC	SSOP	TSSOP	TVSOP
SN74GTLPH306	24	8-Bit LVTTL-to-GTLP Bus Transceivers		+		+	+
SN74GTLP817	24	GTLP-to-LVTTL 1-to-6 Fanout Drivers		+		+	+
SN74GTLP1394	16	2-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Bus Transceivers with Selectable Parity		+		+	+
SN74GTLPH1612	64	18-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Universal Bus Transceivers				+	
SN74GTLPH1616	64	17-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Universal Bus Transceivers with Buffered Clock				+	
SN74GTLPH1645	56	16-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Bus Transceivers				+	+
SN74GTLPH1655	64	16-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Universal Bus Transceivers				+	
SN74GTLPH3245	114	32-Bit LVTTL-to-GTLP Adjustable-Edge-Rate Bus Transceivers	+				
SN74GTLPH16612	56	18-Bit LVTTL-to-GTLP Universal Bus Transceivers			✓	✓	
SN74GTLPH16912	56	18-Bit LVTTL-to-GTLP Universal Bus Transceivers				+	+
SN74GTLPH16916	56	17-Bit LVTTL-to-GTLP Universal Bus Transceivers with Buffered Clock				+	+
SN74GTLPH16945	48	16-Bit LVTTL-to-GTLP Bus Transceivers				+	+
SN74GTLPH32945	96	32-Bit LVTTL-to-GTLP Bus Transceivers	+				

LVT

Device	No. Pins	Description	Availability					
			MIL	LFBGA	SOIC	SSOP	TSSOP	TVSOP
LVT Octals (SN74LVTxxx, SN74LVTHxxx)								
SN74LVTH125	14	Quad Bus Buffers with 3-State Outputs			✓	✓	✓	✓
SN74LVTH126	14	Quad Bus Buffers with 3-State Outputs			+	+	+	+
SN74LVT240A	20	Octal Buffers/Drivers with 3-State Outputs			✓	✓	✓	
SN74LVTH240	20	Octal Buffers/Drivers with 3-State Outputs			✓	✓	✓	
SN74LVTH241	20	Octal Buffers/Drivers with 3-State Outputs			✓	✓	✓	
SN74LVT244B	20	Octal Buffers and Line Drivers with 3-State Outputs			✓	✓	✓	✓

✓ = Now + = Planned

(continued on next page)

LVT *(continued from previous page)*

Device	No. Pins	Description	Availability					
			MIL	LFBGA	SOIC	SSOP	TSSOP	TVSOP
LVT Octals (SN74LVTxxx, SN74LVTHxxx) *(continued from previous page)*								
SN74LVTH244A	20	Octal Buffers and Line Drivers with 3-State Outputs	✓		✓	✓	✓	✓
SN74LVT245B	20	Octal Bus Transceivers with 3-State Outputs			✓	✓	✓	✓
SN74LVTH245A	20	Octal Bus Transceivers with 3-State Outputs	✓		✓	✓	✓	✓
SN74LVTH273	20	Octal D-Type Flip-Flops with Clear			✓	✓	✓	
SN74LVTH373	20	Octal Transparent D-Type Latches with 3-State Outputs	✓		✓	✓	✓	
SN74LVTH374	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓		✓	✓	✓	
SN74LVTH540	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs			✓	✓	✓	✓
SN74LVTH541	20	Octal Buffers and Line Drivers with 3-State Outputs			✓	✓	✓	✓
SN74LVTH543	24	Octal Registered Transceivers with 3-State Outputs			✓	✓	✓	✓
SN74LVTH573	20	Octal Transparent D-Type Latches with 3-State Outputs	✓		✓	✓	✓	✓
SN74LVTH574	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓		✓	✓	✓	✓
SN74LVTH646	24	Octal Registered Bus Transceivers with 3-State Outputs	✓		✓	✓	✓	✓
SN74LVTH652	24	Octal Bus Transceivers and Registers with 3-State Outputs			✓	✓	✓	✓
LVT Widebus™ (SN74LVTH16xxx)								
SN74LVT16240	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+	+
SN74LVTH16240	48	16-Bit Buffers/Drivers with 3-State Outputs				✓	✓	✓
SN74LVTH16241	48	16-Bit Buffers/Drivers with 3-State Outputs				✓	✓	
SN74LVT16244B	48	16-Bit Buffers/Drivers with 3-State Outputs				+	+	+
SN74LVTH16244A	48	16-Bit Buffers/Drivers with 3-State Outputs	✓			✓	✓	✓
SN74LVT16245B	48	16-Bit Bus Transceivers with 3-State Outputs				✓	✓	+
SN74LVTH16245A	48	16-Bit Bus Transceivers with 3-State Outputs	✓			✓	✓	✓
SN74LVTH16373	48	16-Bit Transparent D-Type Latches with 3-State Outputs	✓			✓	✓	
SN74LVTH16374	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Output	✓			✓	✓	
SN74LVTH16500	56	18-Bit Universal Bus Transceivers with 3-State Outputs				✓	✓	✓
SN74LVTH16501	56	18-Bit Universal Bus Transceivers with 3-State Outputs	✓			✓	✓	✓
SN74LVTH16541	48	16-Bit Buffers/Drivers with 3-State Outputs				✓	✓	
SN74LVTH16543	56	16-Bit Registered Transceivers with 3-State Outputs				✓	✓	✓
SN74LVTH16646	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				✓	✓	✓
SN74LVTH16652	56	16-Bit Bus Transceivers and Registers with 3-State Outputs				✓	✓	✓
SN74LVTH16835	56	18-Bit Universal Bus Drivers with 3-State Outputs				✓	✓	✓
SN74LVTH16952	56	16-Bit Registered Transceivers with 3-State Outputs	✓			✓	✓	✓
LVT Widebus+™ (SN74LVTH32xxx)								
SN74LVT32244	96	32-Bit Buffers/Drivers with 3-State Outputs		+				
SN74LVTH32244	96	32-Bit Buffers/Drivers with 3-State Outputs		+				
SN74LVT32245	96	32-Bit Bus Transceivers with 3-State Outputs		+				
SN74LVTH32245	96	32-Bit Bus Transceivers with 3-State Outputs		+				
SN74LVTH32373	96	32-Bit Transparent D-Type Latches with 3-State Outputs		+				
SN74LVTH32374	96	32-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs		+				
SN74LVTH32501	114	32-Bit Universal Bus Transceivers with 3-State Outputs		+				
LVT Octals/Widebus With Series Damping Resistors (SN74LVTH2xxx, SN74LVTH162xxx)								
SN74LVTH2245	20	Octal Bus Transceivers with Series Damping Resistors and 3-State Outputs			✓	✓	✓	✓
SN74LVTH2952	24	Octal Bus Transceivers and Registers with 3-State Outputs			✓	✓	✓	✓
SN74LVT162240	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				+	+	+
SN74LVTH162240	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				✓	✓	✓
SN74LVTH162241	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				✓	✓	
SN74LVT162244A	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs				+	+	+
SN74LVTH162244	48	16-Bit Buffers/Drivers with Series Damping Resistors and 3-State Outputs	✓			✓	✓	
SN74LVT162245A	48	16-Bit Bus Transceivers with Series Damping Resistors and 3-State Outputs				✓	✓	+
SN74LVTH162245	48	16-Bit Bus Transceivers with Series Damping Resistors and 3-State Outputs	✓			✓	✓	
SN74LVTH162373	48	16-Bit Transparent D-Type Latches with 3-State Outputs	✓			✓	✓	
SN74LVTH162374	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✓			✓	✓	
SN74LVTH162541	48	16-Bit Buffers/Drivers with 3-State Outputs				✓	✓	

✓ = Now + = Planned

Appendix A

For More Information

GTLP Overview: New Devices Offer Higher Speed With Better Signal Integrity and Lower Power Consumption Than Traditional Backplane Logic

DALLAS (Jan. 18, 2000)—As the world leader in logic, TI continues to drive the market by introducing its new family of Gunning Transceiver Logic Plus (GTLP) devices, which enable designers to increase backplane data throughput by 100 to 300 percent over traditional logic, such as ABT, FCT, LVT, ALVT, LVC and FutureBus+. These devices are specifically designed for multi-slot medium- and heavily-loaded backplanes and fully support live insertion, a capability that is imperative in high-availability communications and networking applications. In addition, some devices are footprint compatible with logic currently used in parallel backplanes to further ease the designer's task of integrating GTLP into next-generation systems.

www.ti.com/sc/gtlp

Application Reports Summary

Basic Design Considerations for Backplanes (SZZA016)

This application report describes the design issues relevant to backplane design. Designing a high-performance backplane can be extremely complex, where issues such as distributed capacitance, stub lengths, signal integrity, noise margin, rise time, flight time, and propagation delay need to be defined and optimized to achieve good signal integrity on the backplane board. This application report is based on a GTLP backplane driver used to study the effects of these issues. Guidelines that should be followed by backplane designers for optimal board design are detailed. The information in this application report should enable the design engineer to successfully design a high-performance backplane using GTLP.

www.ti.com/sc/docs/psheets/abstract/apps/szza016a.htm

Fast GTLP Backplanes With the GTL1655 (SCBA015)

This application report describes the physical principles of fast bus systems and the problems that can arise in their development. Transmission-line theory is the basis for comparing various specifications of TTL, BTL, GTL and GTLP integrated circuits.

The SN74GTL1655 universal bus transceiver (UBT) is presented as an optimum solution for the design of backplanes for future high-speed bus systems. Comprehensive measurement results of tests on the SN74GTL1655 are included.

www.ti.com/sc/docs/psheets/abstract/apps/scba015.htm

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic (SCEA003)

GTL and BTL transceivers provide high-performance, excellent signal integrity and cost-effectiveness in high-speed backplane and point-to-point applications. This document discusses the GTL and BTL devices I/O structure, power consumption, simultaneous switching, slew rate, and signal integrity. Design considerations for using these devices are provided.

www.ti.com/sc/docs/psheets/abstract/apps/scea003a.htm

Thin, Very Small-Outline Package (TVSOP) Application Brief (SCBA009)

Development of portable, lightweight, high-performance electronics products is driving the semiconductor industry toward smaller, thinner, and higher-density packages. Pricing pressures are encouraging strong efforts toward cost reduction. TI always has been a leader in IC packaging and is now introducing a new family of thin, very small-outline packages (TVSOP) to support the component miniaturization requirements of the industry. The new TVSOP family, in 14-, 16-, 20-, 24-, 48-, 56-, 80-, and 100-pin types, features a lead pitch of 0.40 mm (16 mil) and a device height meeting the 1.2-mm Personal Computer Memory Card International Association (PCMCIA) requirement. The TVSOP have received Joint Electronics Device Engineering Council (JEDEC) registration under semiconductor package standard MO-194. This application report presents an overview of the TVSOP family characteristics, including thermal, electrical, reliability, and moisture-sensitivity performance. Assembly and mounting guidelines for devices with 0.40-mm lead pitch are included.

www.ti.com/sc/docs/psheets/abstract/apps/scba009c.htm

32-Bit Logic Families in LFBGA Packages: 96- and 114-Ball Low-Profile, Fine-Pitch BGA Packages (SCEA014)

Collectively Integrated Device Technology, Philips Semiconductors and TI evaluated many customer inputs and identified a Low-Profile, Fine-Pitch Ball-Grid Array (LFBGA) package solution that would best serve customers' needs at 64 and higher ball counts. Studies have shown that the LFBGA is an optimal solution for reducing the inductance, improving thermal performance and minimizing board real estate in support of integrated bus functions. Together, our objective is to provide multisource products in a package that enables significant electrical improvements when compared to existing packages, as well as cost savings to the OEM manufacturing process.

www-s.ti.com/sc/techlit/scea014

MicroStar Junior™ Design Summary (SCET004)

Collectively Philips Semiconductors and TI evaluated many customer inputs and identified a VFBGA package solution that would best serve customers' needs at 56 and below ball count. Studies have shown that the VFBGA is an optimal solution for reducing the inductance, improving thermal performance and minimizing board real estate in support of integrated bus functions. Together, our objective is to provide multi-source products in a package that enables significant electrical improvements when compared to existing packages, as well as cost savings to the OEM manufacturing process.

www-s.ti.com/sc/psheets/scet004/scet004.pdf

Comparison of Electrical and Thermal Parameters of Widebus SMD and LFBGA Packages (SCYA007)

The trend toward 16- and 32-bit-wide bus systems, in conjunction with continuing advances in surface-mount technology during the 1980s and 1990s, led to the development of ever-smaller packages combined with increased integrated-circuit performance. The improvement in the electrical characteristics of the packages also made possible development of smaller-footprint packages for Widebus circuits. In the mid-1980s, TI produced Widebus devices with improved electrical characteristics and expanded data width, supporting up to 20 bits in a single package. Now, TI is launching the low-profile, fine-pitch, ball-grid array (LFBGA). The LFBGA is the first BGA package for logic components, featuring improved signal characteristics, as well as increased integration. With new designs that support up to 36 bits in a single package, doubling component density on the printed circuit board using Widebus packages has been achieved. The purpose of this report is to familiarize designers with the advantages of this package option by comparing the mechanical data, electrical characteristics, and thermal parameters of four packages: 48-pin SSOP (Shrink Small-Outline Package), 48-pin TSSOP (Thin Shrink Small-Outline Package), 48-pin TVSOP (Thin, Very Small-Outline Package), and 96-pin LFBGA (Low-profile Fine-pitch Ball-Grid Array), using the 244-function (unidirectional) buffer/driver of the LVC logic family.

www.ti.com/sc/docs/psheets/abstract/apps/scya007.htm

Semiconductor Packing Methodology (SZZA021A)

The TI Semiconductor Group uses three packing methodologies to prepare semiconductor devices for shipment to end-users. The methods employed are linked to the device level for shipping configuration keys. End users of the devices often need to peruse many TI and industry publications to understand the shipping configurations. This application report documents TI's three main shipping methods and typical dimensions for end users to review.

www.ti.com/sc/docs/psheets/abstract/apps/szza021a.htm

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