Application Report
SCYA049A–April 2010–Revised July 2016

How to Select Little Logic

Samuel Lin

Standard Linear and Logic

ABSTRACT

TI Little Logic devices are logic-gate devices assembled in a small single-, dual-, or triple- gate package. Little Logic devices are widely used in portable equipment, such as mobile phones, MP3 players, and notebook computers. Little Logic devices are also used in desktop computers and telecommunications. Little Logic gates are common components for easy PC board routing, schematic design, and bug fixes that add without taking up significant space.

Little Logic devices are offered in several product categories that meet specific requirements of low and ultra-low voltage, and low power. This application report discusses critical characteristics, features, and applications of TI's newest Little Logic family and package offerings.

Contents

List of Figures

List of Tables

1 Introduction

System designers occasionally are faced with choosing the right product from several Little Logic families. AND, OR, XOR, and NAND device functions, as well as other multiplexer functions are important in enhancing system reliability and fixing timing problems in circuit design. Parameters and features of I_{off}, C_{on}, input tolerance, and speed are important when selecting the right devices for critical timing design.

This application report lists some of the key product family features, parameters, and advantages for selecting the right device for a specific design.

Figure 1 shows Little Logic families by operating voltage range at optimized supply-voltage nodes.

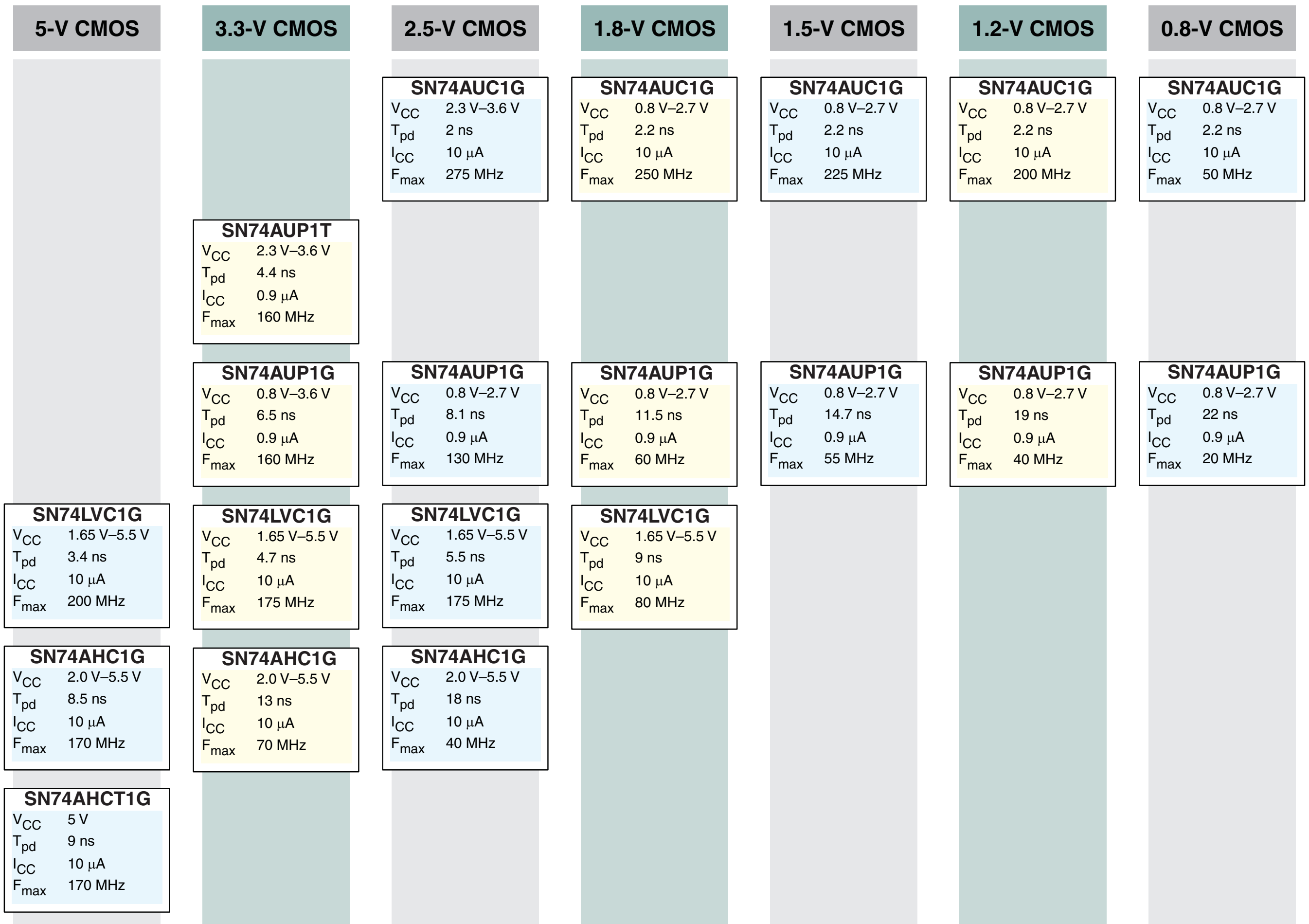


Figure 1. Little Logic Migration to Low Voltage/Low Power

Little Logic gate usage is increasing because it represents a major advantage over multiple-gate devices, which require the routing of multiple etches from distinct partitions on a printed circuit board (PCB) through one logic device. Little Logic devices are housed in a single, dual, or triple gate, limiting the IC pinout to 4-, 5-, 6-, and 8-pin packages.

Figure 2 shows the benefits of using Little Logic devices when designing the PC board layout.

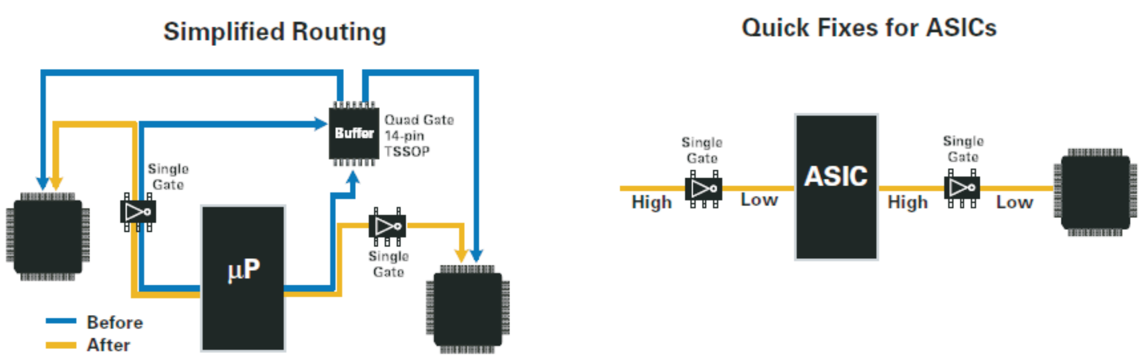


Figure 2. PC Board Layout and Better Overall Performance

2 Little Logic Product Families

Little Logic gates can be used in any digital circuit, PC, portable equipment, or telecommunication device, with the advantages of easy board layout and design.

Portable equipment requires a very small package to fit in its compact slim casing, and a low-voltage function to meet the requirements CPUs and MCUs, as well as low power consumption to extend battery life.

The technologies used are based on the CMOS manufacturing process. CMOS input stages are controlled exclusively by application voltage, so there is no current flowing at the input stage. Therefore, the input impedance of CMOS devices is in the mega-Ω range. Negative voltage spikes are limited by a protection diode. The output stage of most CMOS logic depends on the applied supply voltage with proper switching output level, except specific output structures, such as open drain, output 3-state, or overshoot or undershoot protection.

TI offers not only different logic-gate functions, but also digital switch and analog switch product functions in Little Logic families:

- SN74AHC1G, SN74AHCT1G
- SN74LVC1G/2G/3G
- SN74CBT/CBTLV1G/CBT3T1G
- SN74AUP1G/2G/3G
- SN74AUC1G/2G
- SN74AUP1T (level shifter)

2.1 *SN74AHC1G and SN74AHCT1G Little Logic Devices*

Advanced high-speed CMOS technology (AHC and AHCT) has two products prefixes (SN74AHCT1G and SN74AHC1G) with different logic input levels. The SN74AHCT1Gxx is powered by 5 V and the SN74AHC1Gxx is powered by a wider voltage range (2 V to 5 V) and can be used either in 3.3-V or 5-V environments.

In the current market, some Little Logic uses HCMOS technology with names including 74HC/HCT1G, TC7S, TC7SET, NC7S, and NC7ST. In general, SN74AHC1G and SN74AHCT1G can replace them.TI offers advanced HCMOS Little Logic by adding optimized features for 3.3 V and 5 V.

AHC1G and AHCT1G optimized features versus HCMOS:

- Low noise – The AHC1G family allows designers to maintain the same low-noise characteristics of HCMOS without the overshoot and undershoot typical of higher-drive devices usually required to achieve speeds.
- Speed – The AHC1G offers three times the speed of HCMOS (see Figure 3).
- Low power – The AHC1G family uses CMOS technology and has low power consumption, and 10-µA maximum static current.
- Drive – Output-drive current is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- 5-V input tolerant at 3.3 V – With the input diode to V_{CC} removed, it is specified for both 5-V and 3.3-V operation and down translation (HCMOS does not support this).

Table 1. AHC1G and AHCT1G Versus HCMOS

		AHCT1G	AHC1G	HCMOS	
V_{CC}		5 V	3.3 V	5 V	2 V
Drive		±8 mA	±8 mA	8 mA or less	20 µA
Speed (maximum)		5.5 ns	7.9 ns	17 ns	54 ns or slower
Power dissipation capacitance		9.5 pF			
Level conversion option	Input	3.3 V	5 V	3.3 V	
	Output	5 V	3.3 V	5 V	

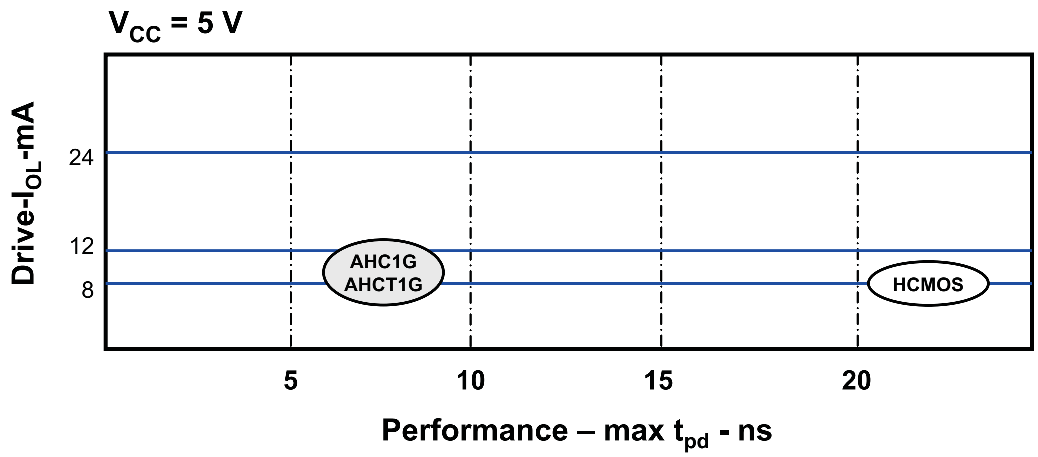


Figure 3. AHC vs HC Performance Comparison

2.1.1 AHC and AHCT Translation Features

Level matching between parts of circuits is very important in the design process to make a system reliable and stable. Most processor I/O switching levels use TTL levels or low-voltage CMOS, which refers to supply V_{CC} changing the logic level.

The AHCT1G is a designed LVTTL/TTL input (2 V/0.8 V), which can also accept 5-V CMOS (4.44 V/0.5 V). The output is fixed 5-V CMOS (4.44 V/0.5 V). In fact, the AHCT1G operates as a translation gate from 3.3-V input to 5-V CMOS powered by a 5-V node.

Figure 4 shows a typical example of the SN74AHCT1G application converting LVTTL to 5-V CMOS.

The SN74AHC1G is designed to achieve LVTTL-/TTL-level matching at 3.3-V V_{CC} operating with levels of (V_{IH} = 2 V and V_{IL} = 0.8 V). With 5-V input tolerance, it can be used in a down-translation application and the output level relies on the supply V_{CC}.

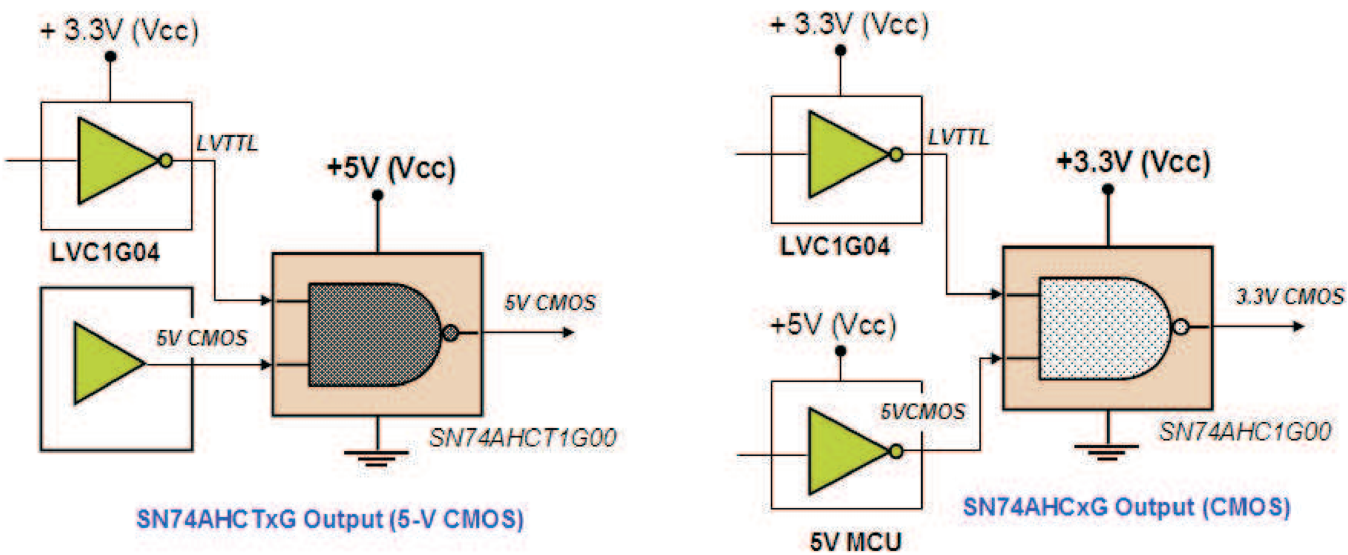


Figure 4. SN74AHCT1G00 and SN74AHC1G00 Output Structures

In summary, the SN74AHCT1G is powered by 5 V to accept LVTTL/TTL levels and the SN74AHC1G can be powered by 3.3 V to accept LVTTL/TTL levels.

2.2 *SN74LVCxG Little Logic Devices*

SN74LVC1G, SN74LVC2G, and SN74LVC3G Little Logic components are designed with no clamp diodes to V_{CC} on either inputs or outputs, making the interface voltage higher than applied V_{CC}. This design allows the down translation from 5 V to a desired lower switch level, which refers to supply V_{CC} of the chip. As its operating voltage is from 1.65 V to 5 V, it allows a mixed mode where the designer can use 1.8 V, 2.5 V, or 3.3 V.

The SN74LVCxG logic family input structure is 3.3-V CMOS DC; V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V meet LVTTL, meaning that the threshold voltage of 1.5 V is typically where the transition from a recognized low input to a recognized high input occurs.

The output is a pure CMOS output structure and it is mainly related to applied supply voltage, with minor influence from I_{OH}/I_{OL} driving current and loading.

SN74LVCxG Little Logic is faster in CMOS speed compared to SN74AHCxG to meet critical timing requirements in memory application, I/O switching, and control signals. It is optimized in 3.3-V digital circuits and has become a mainstream Little Logic family.

The SN74LVCxG can be selected for direct replacement of the SN74AHCxG when faster speed and higher driving capability are required.

2.2.1 LVC Partial Power Down (I_{OFF})

SN74LVC1G, SN74LVC2G, and SN74LVC3G have partial power-down mode, which allows isolating the power of the chip for power saving and signal isolation.

The I_{OFF} protection circuit ensures that no excessive current is drawn to/from an input, output, or combined I/O that is biased to a specified voltage while the device is powered down (V_{CC} = 0 V), and supports a partial power-down mode of system operation. In the case of a wireless LAN module where some logic is required yet the supply voltage is isolated, the selected gate device must have the I_{OFF} feature to prevent current leakage.

SN74LVC1G, SN74LVC2G, and SN74LVC3Gxx with I_{OFF} allows a maximum of approximately 10 µA to flow under these conditions. This condition is helpful to a designer not considering isolating the signal during the power-off mode.

2.3 *SN74AUPxG Little Logic Devices*

Today's processors and microcontrollers are moving to lower voltage operation for power saving and. the I/Os will need to run at higher frequencies with less noise.

Advanced ultra-low power (AUP) CMOS Little Logic is optimized at 3.3 V and lowers voltage down to 1 V with optimized driving capability. AUP devices consume 50% less power than the current mainstream LVC or LCX single gates and are ideal for portable equipment, such as mobile phones, PDAs, digital cameras, and video cameras, as well as digital photo frames where an extended battery life is required.

The SN74AUPxG Little Logic gate has similar I/O structure (CMOS I/O) to the SN74LVCxG for easy replacement under 3.3 V or lower conditions.

The SN74AUPxG device with single-gate CMOS low power dissipation (I_{CC} = 0.5 µA maximum at 25°C) is considered the lowest power consumption logic gate when compared to other existing single-gate products.

The I/O structure provides design protection even when input voltages of up to 3.6 V are applied, regardless of the supply voltage. This enables the products to interface 3-V circuits to 1.2-V environments and vice versa.

The SN74AUP1G logic family includes single-, dual-, and triple-gate functions packaged in 4-, 5-, 6-, and 8-pin packages for specific design requirements.

Table 2 shows differences between the SN74LVC1G00 and SN74AUP1G00 devices. The SN74AUP1G00 has enhancements in lower power and lower voltage design that the SN74LVC1G00 does not provide, such as 1.4 V and 1.1 V and lower power consumption (I_{CC}: AUP1G = 0.5 µA and LVC1G = 10 µA).

Table 2. SN74AUP1G00 and SN74LVC1G00 Comparison

		SN74AUP1G00	SN74LVC1G00
Supply voltage		0.8 to 3.6 V	1.65 V to 5.5 V
Input tolerant		3.6 V	5.5 V
I_{OFF}		±0.2 µA	±10 µA
I_{CC}		0.5 µA	10 µA
I_{OH}/I_{OL}	1.1 V	1.1 mA	–
	1.4 V	1.7 mA	–
	1.65 V	1.9 mA	1.9 mA
	2.3 V	3.1 mA	3.1 mA
	3 V	4 mA	4 mA
V_{OH}	1.1 V	0.75 x V_{CC}	no
	1.4 V	1.11 V	no
	1.65 V	1.32 V	0.65 x V_{CC}
	2.3 V	1.9 V	1.7 V
	3 V	2.6 V	2 V
	5 V	–	0.7 x V_{CC}
V_{OL}	1.1 V	0.3 x V_{CC}	–
	1.4 V	0.31 V	–
	1.65 V		0.35 x V_{CC}
	2.3 V	0.44 V	0.7 V
	3 V		0.8 V
	5 V	–	0.3 x V_{CC}

2.3.1 SN74AUPxG Little Logic Power Consumption

As cellular phones and other portable electronics become more complex, more power is consumed by systems in both active and standby mode. Consequently, selecting low-power devices for portable electronics imposes new challenges in the areas of core voltage, energy management, and battery lifetime.

Increasing microprocessor complexity increases power consumption and, by selecting the Little Logic product family, migration to low-power CMOS logic achieves the lowest power consumption in both dynamic- and static-mode situations.

Figure 5 shows power-usage differences between LVC and AUP. Both dynamic-power consumption and static-power consumption are significantly lower with LVC Little Logic.

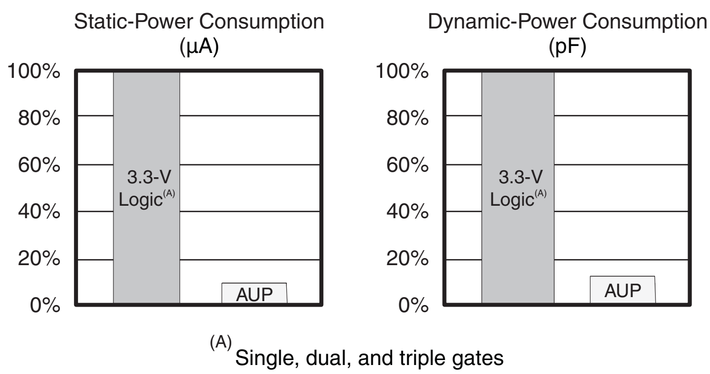


Figure 5. LVC/AUP Power Consumption Comparison

2.4 SN74AUCxG Little Logic Devices

Advanced ultra-low-voltage CMOS (SN74AUC1G) devices are optimized at 1.8-V V_{CC} with wider operation from 0.8 V to 2.7 V and a 3.6-V tolerance. This sub-1-V family operates at low power and high speed, while maintaining overall system signal integrity for use in telecommunications equipment, high-performance workstations, and portable consumer electronics.

SN74AUC1G logic devices are designed for high-speed applications with optimum signal integrity. With a unique output structure (see Figure 6), AUC devices switch fast and maintain very low transition noise.

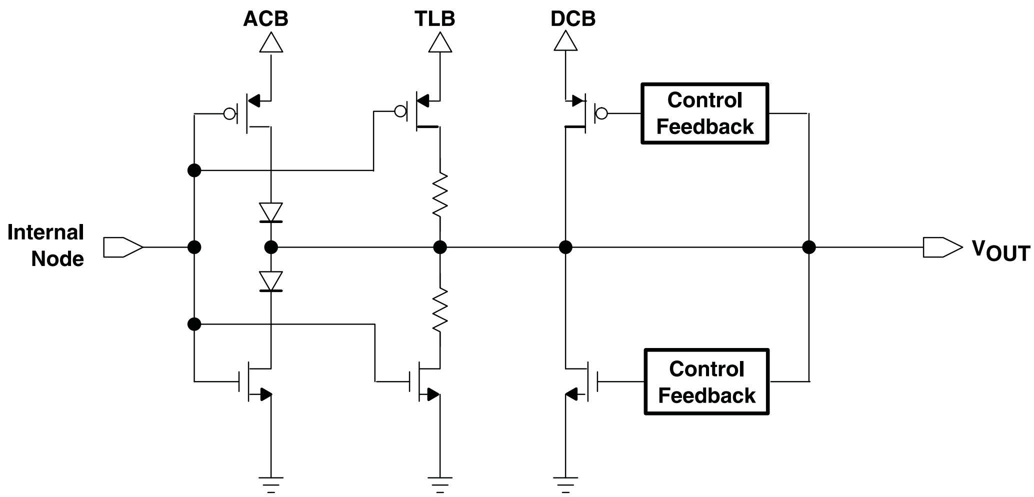


Figure 6. AUC Output Structure

The SN74AUC1G is used for faster timing requirements in 1.8-V operated memory bus controllers.

2.4.1 SN74AUCxG Little Logic Signal Integrity and Faster Speed

System designers continually pursue lower-power high-speed solutions. The increase in system speed may conflict with the low-power requirements. For a push-pull-type CMOS output buffer, higher speed calls for higher drive strength, resulting in the increase of power dissipation, overshoot, and undershoot. At low V_{CC}, the signal swing is smaller, resulting in lower transition time. But the low signal swing requires better signal integrity as the noise margin gets smaller with lower V_{CC}. SN74AUC1G logic addresses the challenge of higher structure. In addition to better signal integrity and faster speed requirements, system designers, especially for portable applications, require a solution that uses no external termination, that is, damping resistors, clamping diodes, pullup resistors, and so forth.

Because AUC is the next generation of sub-3.3-V design, TI not only offers the Little Logic family, but also multichannel and 16-/32-bit Widebus™ products for 1.8-V high-speed design requirements.

2.5 SN74AUP1T Gate Logic Translator Little Logic Devices

SN74AUP1T is modified from SN74AUP1G to meet the lower threshold for lower voltage input switching levels of 1.8 V and 2.5 V. The output refers to supply V_{CC} and can be achieved by connecting either 2.5-V CMOS or 3.3-V CMOS outputs.

The SN74AUP1T output is comparable to a standard SN74AUP1G CMOS output supply voltage (V_{CC}) except for the input level.

The major difference between SN74AUP1G and SN74AUP1T is the different logic input switching level. The SN74AUP1G input refers to supply V_{CC} and the SN74AUP1T input is designed to accept a lower threshold level. For example, SN74AUP1G (3.3 V) is an LVTTL input and SN74AUP1T (3.3 V) accepts a 1.8-V to 2.5-V logic level for high or low.

The SN74AUP1T gate only requires a single voltage to achieve the level shifter function:

- 1.8 V to 3.3 V (at V_{CC} = 3.3 V)
- 2.5 V to 3.3 V (at V_{CC} = 3.3 V)

- 1.8 V to 2.5 V (at V_{CC} = 2.5 V)
- 3.3 V to 2.5 V (at V_{CC}= 2.5 V)

Figure 7 shows the potential application requirements in mixed-mode environments.

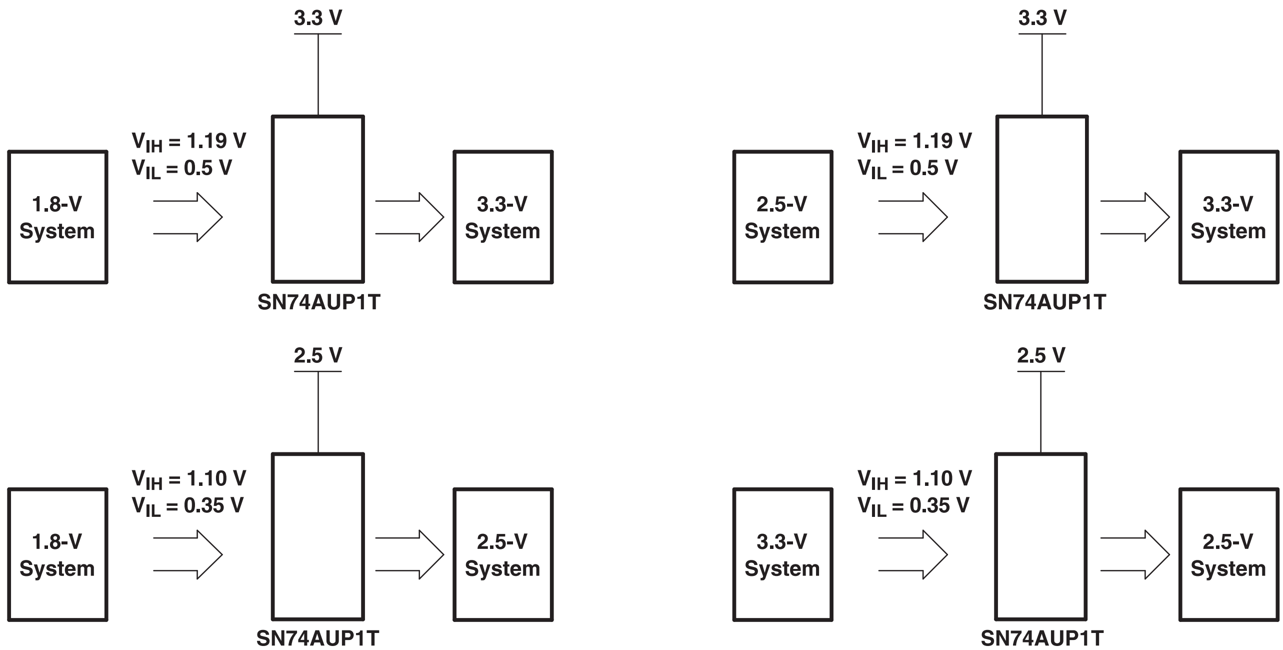


Figure 7. Potential Level Translator Applications

2.6 *SN74CBTxG, SN74CBTDxG, SN74CB3T1G, and SN74CBTLVxG Digital Switch Devices*

TI offers a wide variety of digital switches in standard multiple channels. In the Little Logic family, TI offers a single channel in the product groups of CBT, CBTLV, CB3T, and CBTD. These devices are designed for connecting high-speed digital buses. Characterized by sub-nanosecond propagation delay and fast switching, these devices are ideally suited for voltage translation, hot swapping, hot plug, bus or capacitance isolation, and many other applications.

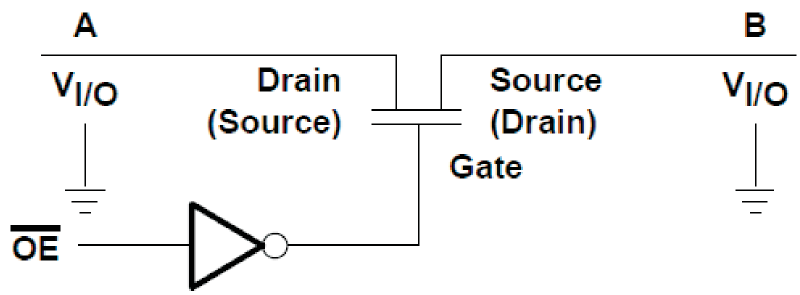
SN74CBT1G125, SN74CBT1G384, SN74CB3T1G125, SN74CBTD1G125, and SN74CBTD1G384 are N-Channel FETs controlled by CMOS logic levels with different powered devices. The switch is bidirectional; the source and drain are interchangeable (while operating, the side with the lowest V_{IO} is the source). Figure 8 shows the N-channel FET switch simplified structure.

An input signal applied to the left I/O pin results in an identical output signal at the right I/O pin. The NMOS switch can pass signals only up to a threshold voltage below V_{CC}. If powered by 5 V when connecting the SN74CBTxG, its output is up to 4 V as the threshold voltage drop is 1 V (see to Figure 7). The NMOS switch can be used in a up-translation application with pullup resistors, and Figure 8 shows the clock input or signal input where the output is limited by external pullup resistors for a desired maximum V_{CC} level. The clock out signal still meets the 5-V TTL/LVTTL level, 2.4-V minimum output. The enable pin is required to pull up to 5 V to ensure the $\overline{EN}$ slew rate.

As previously mentioned, the SN74CBT1G125 output is 4 V maximum and powered by 5 V. The SN74CBTD1G125 gets a maximum 3.3-V LVTTL/5-V TTL output level by adding the diode on the path of the V_{CC} power pin. The internal diode would drop 0.7 V and NMOS would drop 1 V then the output is 3.3 V maximum (see Figure 9). In fact, all SN74CBTDxG are used as 5-V to 3.3-V down translators with bidirectional switches without adding any pullup resistor like the SN74CBT1G125.

The SN74CB3T1G125 is powered by 2.5 V and 3.3 V with 5-V input tolerance. It can be used in translation to desired output maximum level, which is equal to supply voltage range. The data input allows 0 V to 5 V with output-level limitation up to V_{CC}.

The SN74CB3T1G125 can be used in down-translation applications to achieve desired output by connecting the desired supply V_{CC}. Figure 10 shows the typical I/O structure. When the input is below V_{CC} level, the output is almost the same. When the input is higher than V_{CC}, the output is limited to the maximum V_{CC} DC level and protects the circuit where they are higher input voltage are not tolerated.



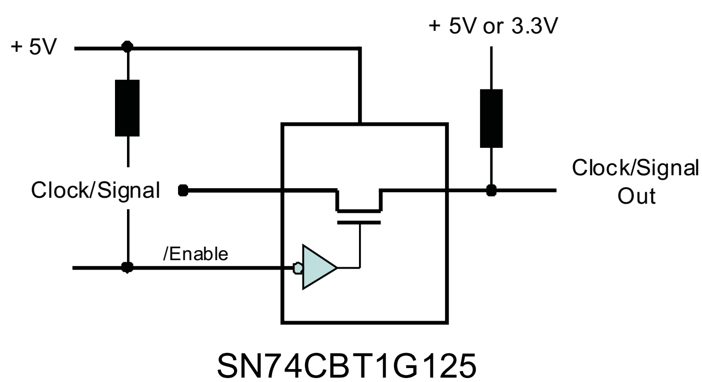


Figure 8. N-Channel FET Switch (SN74CBTxG)

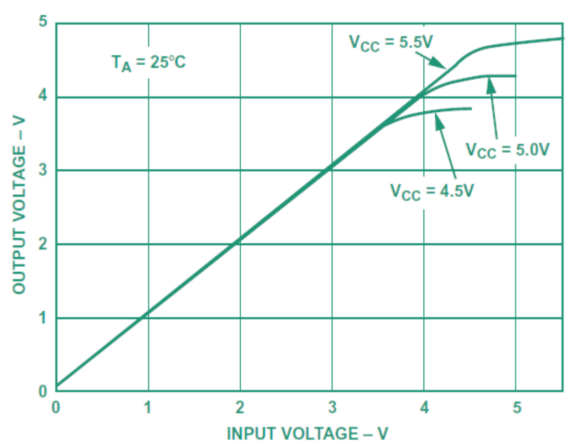
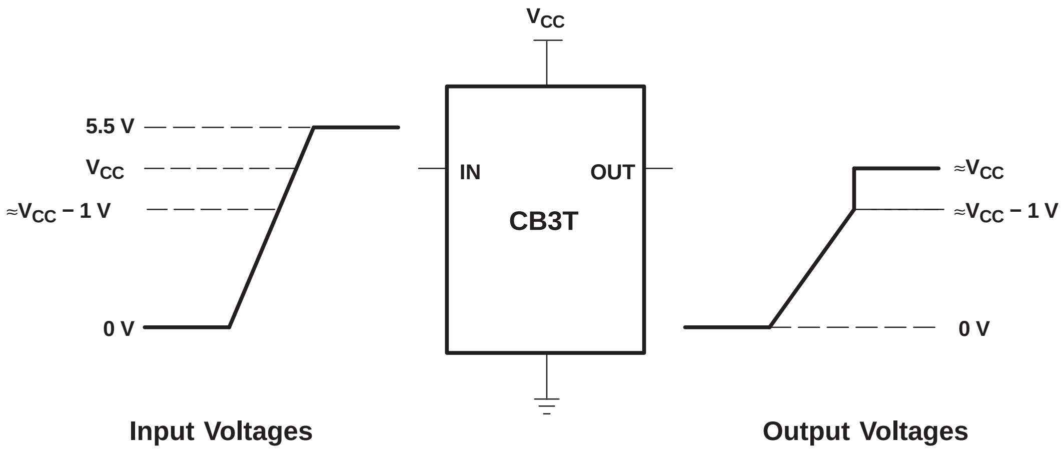


Figure 9. V_{OUT} vs V_{IN} for CBT1G384 and CBT1G125



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} – 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 10. Typical DC Voltage Translation Characteristics

The SN74CBTLV1G125 is a low-voltage single N-channel transistor in parallel with a single P-Channel transistor (see Figure 10) and is optimized in low-side supply voltage range from 2.3 V to 3.6 V and V_O is up to the V_{CC} level. Featuring low r_{ON} and flat r_{ON} values, the device can be used in digital control signals and analog video and audio signals with less distortion.

Since V_I = V_O, it can switch any level of low-voltage signal regardless of supply voltage.

In summary, both the SN74CBTxG and SN74CBTLVxG are digital switches that can bypass any signals within allowed V_{IO} range and defined V_O level.

In addition to digital switches, TI offers CMOS analog switches in the Little Logic family.

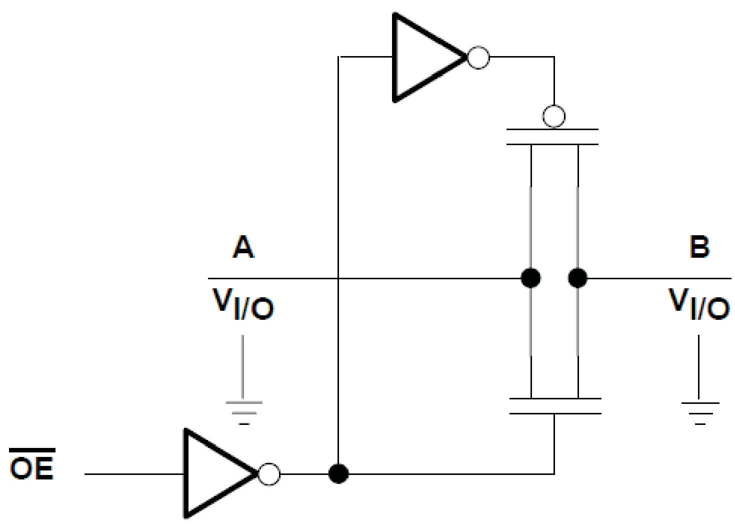


Figure 11. N-Channel FET Switch

2.6.1 Typical Application Using SN74CBTxG/SN74CBTLVxG/SN74CBTDxG

The SN74CBT1G125 and SN74CBT1G384 are 5-V supply digital switches; they have similar functions with different pin assignments (see Figure 12) and are used to switch both analog and digital signal.

A common requirement of bus architectures is low capacitance loading of the bus. Such a system requires bus-bridging devices that allow a number of loads. Ideally, any load on a bus that is not in use should be disconnected to reduce overall capacitive loading and avoid exceeding bus capacitance.

The I²C bus limits the bus up to 400 pF, where the digital switch can be used to isolate unused parts and USB signals for power saving and external overload protection.

The digital switch can be also used in traditional video analog types of S-video, composite, and component video signals, and PC VGA R, G, and B signal isolation and protection.

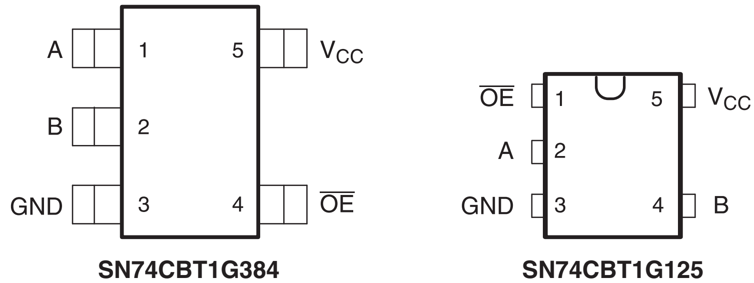


Figure 12. Pin Assignments (SN74CBT1G384 vs SN74CBT1G125)

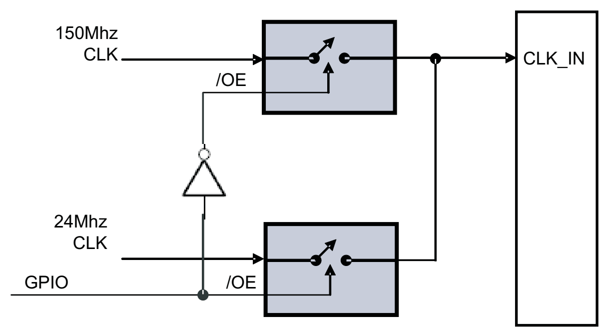
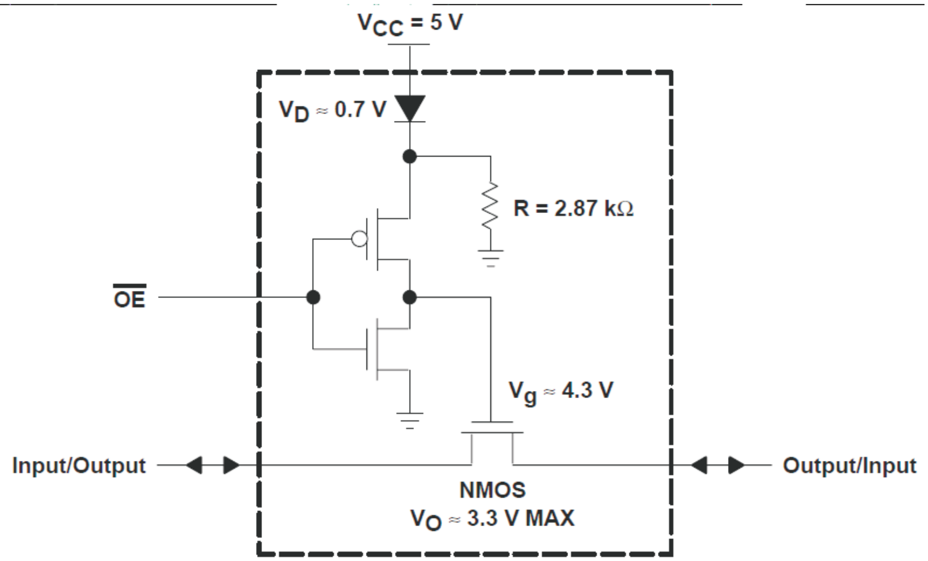


Figure 13. Using Digital Switch as Clock Source Select

The SN74CBTD1G125 and SN74CBTD1G384 use the same pinouts and footprints as the SN74CBT1G125 and SN74CBT1G384, respectively, with the internal diode to V_{CC} getting the exact 3.3-V maximum output level (see Figure 14).



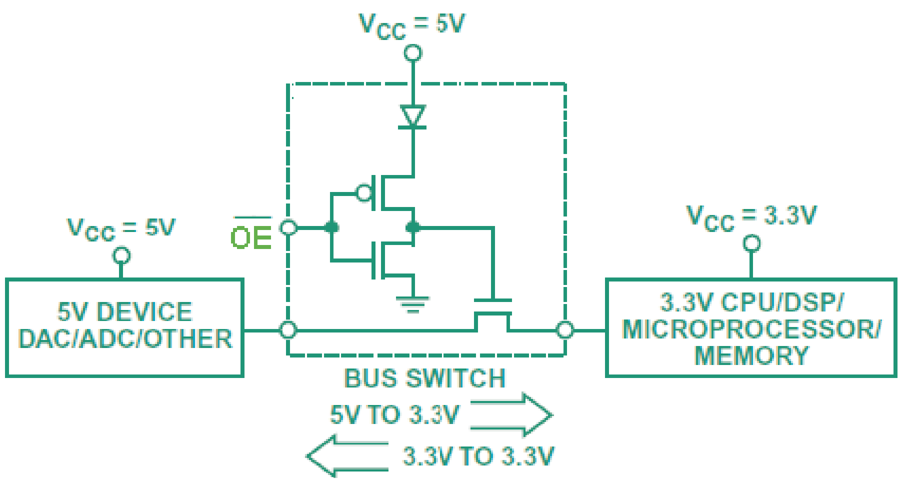


Figure 14. Using SN74CBTD1G384 and SN74CBTD1G125 in Level Translation/Isolation

2.7 *CMOS Analog Switch*

TI also offers a low-voltage CMOS analog switch as 3.3 V optimized (SN74LVC1G66, SN74LVC2G66, SN74LVC1G3157, and SN74LVC2G53) or 1.8 V optimized (SN74AUC1G66, SN74AUC2G66, and SN74AUC2G53).

The CMOS analog switch uses N-/P-channel technology that generates lower r_{ON} and flat r_{ON} to optimize audio and video signal switching with less distortion (see Figure 15).

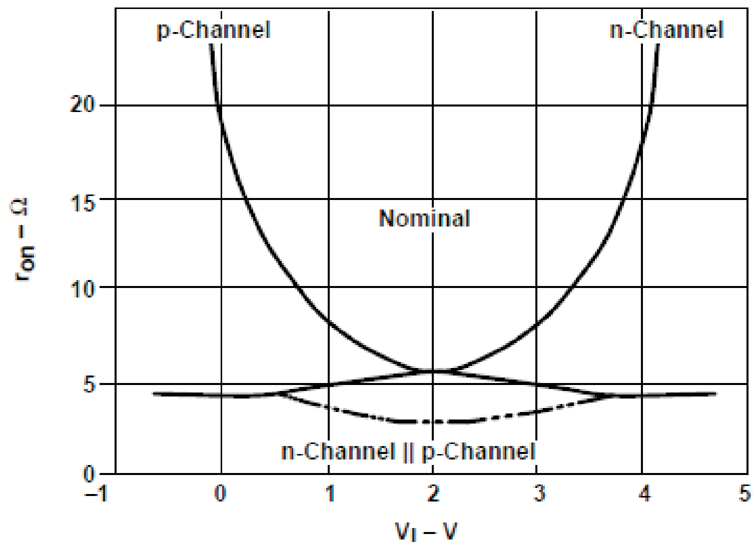


Figure 15. On-State Resistance (r_{ON}) vs Input Voltage for Parallel N-Channel and P-Channel FET Switch

2.7.1 Typical Applications Using CMOS Analog Switch

The SN74LVC1G66 and dual SN74LVC2G66 are high-speed 300-MHz single-pole single-throw (SPST) devices with normally open switches and targeted for general-purpose applications, including audio, video, digital/analog signals, and I^2C open-drain bus isolation and selection.

Figure 17 shows a typical application of a mobile cellular phone connecting the MIC input and audio output isolation during headphone connection. Another typical application is of an amplifier front side selecting the voltage level.

A CMOS analog switch is similar to a digital bus switch (SN74CBT1G125), but CMOS analog switches are easier to use as the N-channel MOSFET in parallel with a P-channel MOSFET allows signals to pass in either direction with equal ease. The two MOSFETs are switched on and off by internal inverting and noninverting amplifiers. Taking the P- and N-channel on resistance (r_{ON}) in parallel for each level of V_{IN} yields composite on-resistance characteristics for the parallel structure (see Figure 15). This plot of r_{ON} versus V_{IN} can be described as linear. The less r_{ON} variation within analog input voltage aids sensitive audio and video signals.

The CMOS analog switch behaves similar to a digital bus but is optimized in applications for A/V analog signals with lower r_{ON} variation. Disadvantages include not having overvoltage tolerance.

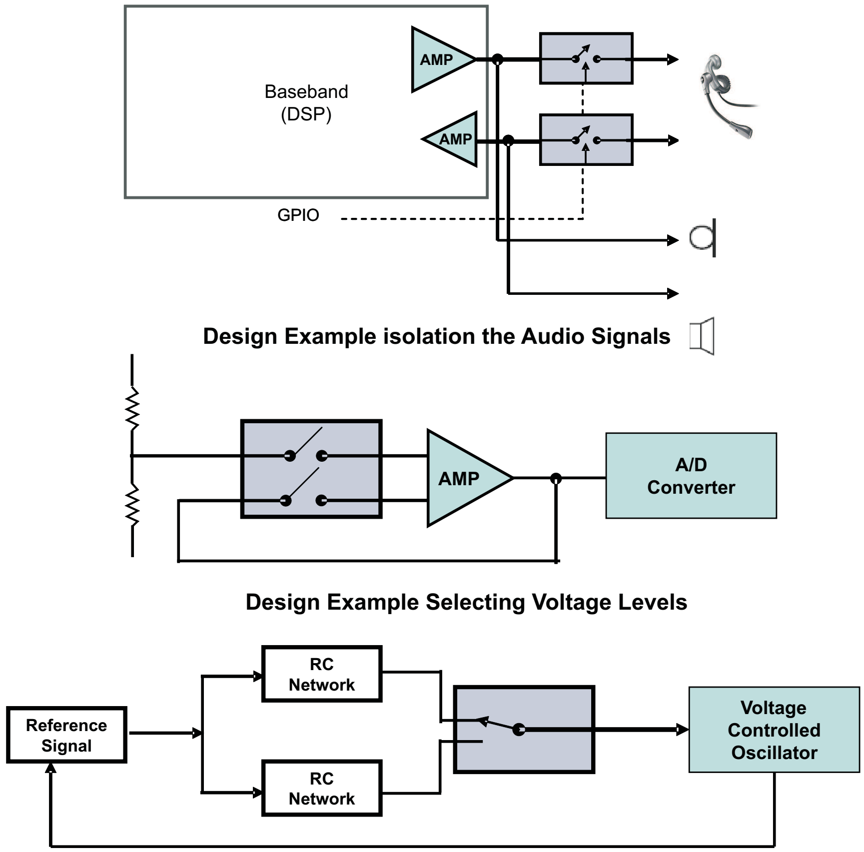


Figure 16. SPST CMOS Analog Switch Applications

3 Key Concerns in Little Logic Selection

Logic gate circuits are designed to input and output with only two types of signals - high (1) and low (0) - as represented by a variable voltage (full power supply voltage for a high state and zero voltage for a low state). In reality, logic signal voltage levels rarely attain full power-supply voltage level due to stray voltage drops in the transistor circuitry.

TTL/LVTTL levels are designed to accept 0 V to 0.8 V for low signal input and 2 V to 5 V for high signal input. CMOS logic (CMOS gate circuit) has input and output signal specifications that are quite different from TTL/LVTTL acceptable logic signal voltage levels. But in CMOS logic, the logic input signal level is almost-compatible TTL, i.e., LVTTL, at 3.3-V power-supply voltage. Logic output signal voltage levels are designed differently for TTL and CMOS. Figure 17 shows the comparison of different logic input and output signal voltage levels. Due to the different logic levels and other functions, such as input tolerance, output tolerance, high-speed, and power-down features, TI offers several logic families.

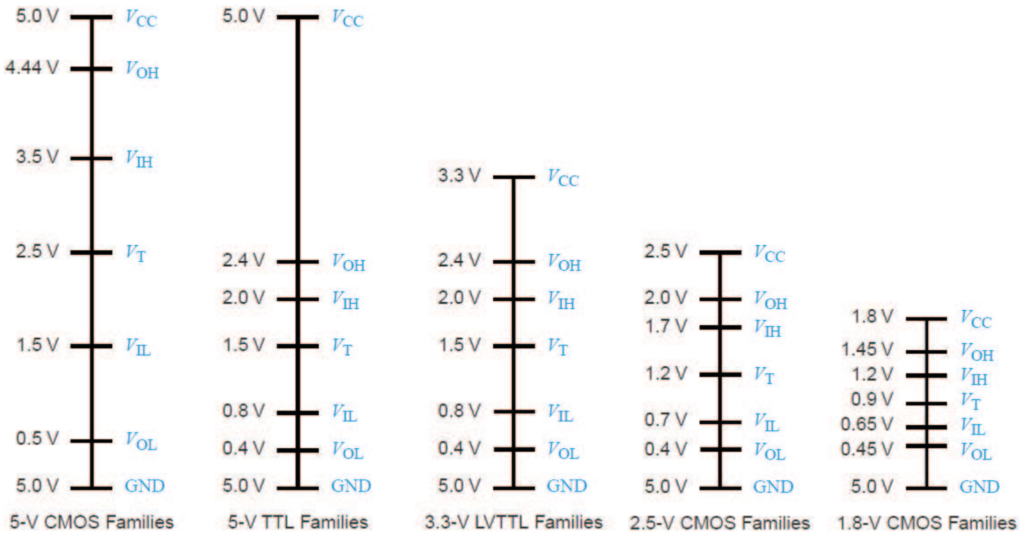


Figure 17. Logic Switching Levels (Inputs/Outputs)

The key to understanding standard Little Logic is in the area of I/O structure to match the connected I/Os, control inputs, outputs, and supply voltage levels.

The following section introduces related key parameters and how they are applied to different designs.

3.1 High- and Low-Level Logic Input (V_{IH}/V_{IL})

In low-voltage logic families, there a many switching levels for CMOS, TTL, mixed CMOS/TTL, ETL, BTL, and GTL.

TI Little Logic families are mainly TTL/CMOS families powered by 3.3 V, 2.5 V, 1.8 V, or even lower voltage. TTL input switching levels are mainly fixed at 2 V minimum for high-state input and 0.8 V maximum for low-state input. This means the logic device can accept the high input from 2 V to V_{CC} level and low input from 0.8 V to 0 V at any supply V_{CC}.

The SN74AHCT1Gxx has TTL input at 5-V supply-voltage operation and all SN74AHC1G, SN74LVC1G, and SN74AUP1G families have an LVTLL input at 3.3-V supply-voltage operation.

Table 3 shows each different Little Logic family input switching level for easy understanding and selection of the right logic with the correct required logic input level.

Table 3. V_{IH}/V_{IL} Comparison for Little Logic

LOGIC INPUTS		AHCT1G	AHC1G	LVC1G	AUP1G	AUC1G
High-level input voltage (V_{IH})	5 V	2 V	3.85 V	0.7 x V_{CC}		
	3.3 V		>2.1 V	2 V	2 V	
	3 V		2.1 V	2 V	2 V	
	2.5 V		>1.5 V	1.7 V	1.6 V	1.7 V
	2 V		1.5 V			
	1.8 V			0.65 x V_{CC}	0.65 x V_{CC}	0.65 x V_{CC}
	1.5 V				0.65 x V_{CC}	0.65 x V_{CC}
	1.1 V				0.65 x V_{CC}	0.65 x V_{CC}

Table 3. V_{IH}/V_{IL} Comparison for Little Logic (continued)

LOGIC INPUTS		AHCT1G	AHC1G	LVC1G	AUP1G	AUC1G
Low-level input voltage (V_{IL})	5 V	0.8 V	1.65 V	0.3 x V_{CC}		
	3.3 V		<0.9 V	0.8 V	0.9 V	
	3 V		0.9 V	0.8 V	0.9 V	
	2.5 V		<0.5 V	0.7 V	0.7 V	0.7 V
	2 V		0.5 V			
	1.8 V			0.3 x V_{CC}	0.35 x V_{CC}	0.35 x V_{CC}
	1.5 V				0.35 x V_{CC}	0.35 x V_{CC}
	1.1 V				0.35 x V_{CC}	0.35 x V_{CC}

Almost all Little Logic is designed to achieve TTL input levels at 3.3-V supply voltage to meet standard LVTTL, and all the switching voltage input levels rely on the supply V_{CC} lower than 3.3 V except the specific designed threshold control.

3.1.1 Input Voltage Range (V_I)

Most logic data sheets provide the maximum input voltage (V_I) range to allow system designers to consider the input signal connection with the absolute maximum rating and recommended operating condition for optimal to worst-case scenarios.

From parameter V_I, it can be determined whether the device has input tolerance at any supply operating voltage range, that is, if $V_I = V_{CC}$, the input signal does not exceed the V_{CC} level, and if V_I = 5 V, the input signal is allowed to maximum 5 V.

Table 4. Input Voltage Range, V_I

		AHCT1G	AHC1G	LVC1G	AUP1G	AUC1G
V_I	Maximum rating	7 V	7 V	6.5 V	4.6 V	3.6 V
	Recommended operating	5.5 V	5.5 V	5.5 V	3.6 V	3.6 V

System engineers should understand the controller logic output maximum levels and use Table 4 to select the right product for maximum voltage-level tolerance, even if the logic V_{IH}/V_{IL} matches the other output connections.

Figure 18 shows that by providing a standard 5-V CMOS output high of 4.7 V, it must select 5-V input tolerance and set the right supply V_{CC} connecting to the logic device V_{CC} to accept the input levels for high and low state.

Table 5. Input Voltage Range

	5-V CMOS OUTPUT	LVTTL OUTPUT	LVC1G00 (V_{IH}/V_{IL})
High	4.7 V to 5 V	2 V to 4.7 V	≥2 V
Low	0 V to 0.2 V	0 V to 0.4 V	≤0.8 V

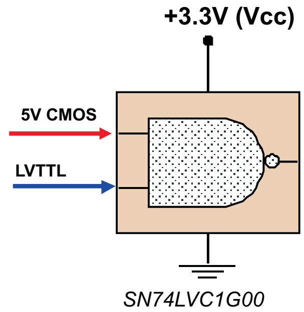


Figure 18. Input Voltage Range

3.2 High- and Low-Level Logic Output (V_{OH}/V_{OL})

The load at the output determines the output voltage. Respectively, as DC current increases and decreases it will cause output voltages to vary. Most logic data sheets provide various signal output-voltage levels by listing *test conditions* for proper system design application. In general, tables show maximum to minimum load by specifying high-level output voltage (V_{OH}) and low-level output voltage (V_{OL}).

Table 6 compares output signal voltage for different CMOS families.

Table 6. V_{OH}/V_{OL} Comparison for Little Logic

LOGIC INPUTS			AHC1G	LVC1G	AUP1G	AUC1G
High-level output voltage (V_{OH})	5 V	–8 mA	3.94 V			
		–32 mA		3.8 V		
	3 V	–4 mA	2.58 V		2.6 V	
		–24 mA		2.3 V		
	2.3 V	–8 mA		1.9 V		
		–3.1 mA			1.9 V	
	1.65 V	–4 mA		1.2 V		
		–1.9 mA			1.32 V	
	1.4 V	–5 mA				1 V
	1.1 V	–3 mA				0.8 V
Low-level output voltage (V_{OL})	5 V	8 mA	0.36 V			
		32 mA		0.55 V		
	3 V	4 mA	0.36 V		0.44 V	
		24 mA		0.55 V		
	2.3 V	8 mA		0.3 V		0.6 V
		3.1 mA			0.44 V	
	1.65 V	4 mA		0.45 V		
		1.9 mA			0.31 V	
	1.4 V	5 mA				0.4 V
	1.1 V	3 mA				0.3 V

For a 3-V supply V_{CC} condition, V_{OH}/V_{OL} is within acceptable TTL/LVTTL output signal voltage range. Therefore, designers use CMOS logic gates driving the TTL/LVTTL signal in a 3.3-V digital circuit.

3.3 Schmitt-Trigger Input Structure (V_{T+}, $V_{T–}$)

V_{T+} is a positive-going input threshold level and $V_{T–}$ is a negative-going input threshold level, that is, V_{T+} maximum is V_{IH} minimum and $V_{T–}$ minimum is V_{IL} maximum to ensure input signal recognition.

The Schmitt trigger is used in many applications in numerous analog and digital circuits. However, the versatility of a TTL Schmitt trigger is hampered by its narrow supply range, limited interface capability, low input impedance, and unbalanced output characteristics.

Figure 19 shows the Schmitt-trigger input (known as hysteresis input) application that receives different amplitudes and uses the hysteresis input circuit to generate the digital output.

V_{T+} and V_{T-} are similar to V_{IH} and V_{IL} to accept a high or low; Figure 20 shows the hysteresis input.

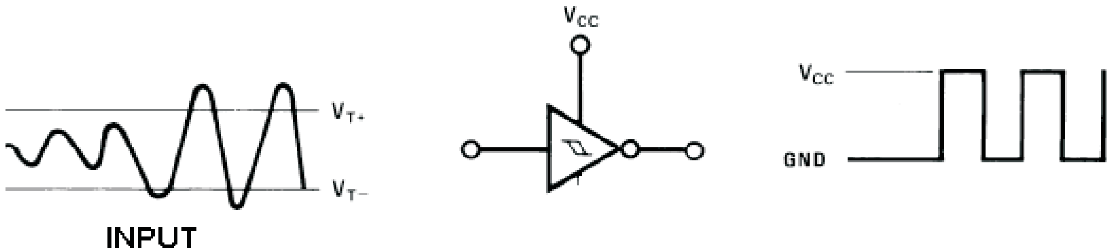
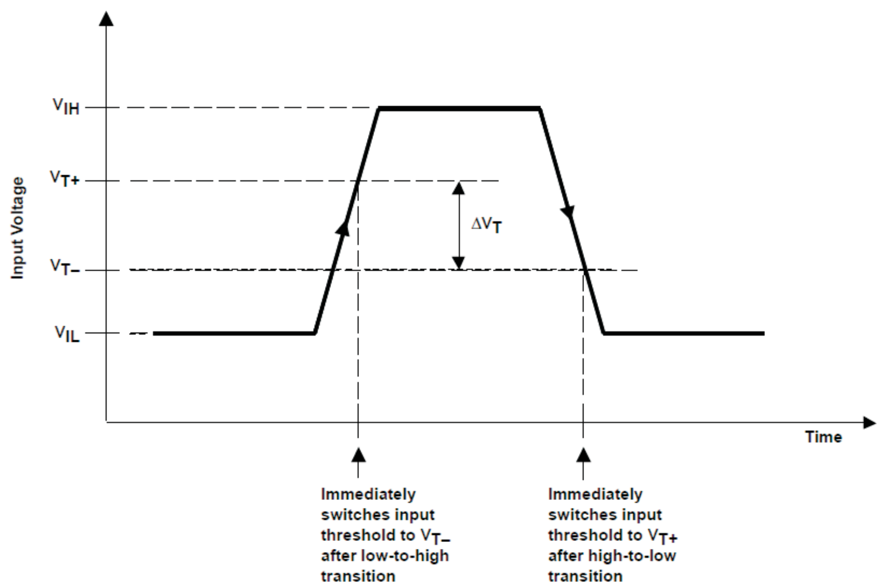


Figure 19. Linear Input With Output Using Schmitt-Trigger Input Gate



The input signal must go higher than V_{IH} or V_{t+} max and lower than V_{IL} or V_{t-} min to guarantee a switch.

Figure 20. Hysteresis - Input Voltage vs Time

The benefit of a device that has built-in dc hysteresis is that, depending on the amount of hysteresis and the amount of noise present, the input is immune to such noise. This digital form of filtering out unwanted noise can be beneficial in a system where noise caused by electromagnetic interference (EMI) or crosstalk cannot be reduced.

3.4 I_{OFF} Partial Power Down and V_{CC} Isolation

During the system design, I_{OFF} is one of the important features to use for power saving. In a power-saving circuit, it can be selected by either choosing lower power consumption devices or isolating the power when the system is sleeping. However, selecting a Little Logic device with the I_{OFF} feature is suggested, otherwise, it causes excess current leakage.

The I_{OFF} feature is also considered one of the protection circuits in an external Interface by connecting the cable to another system that is in power-on mode and the system is in power-down mode.

The I_{OFF} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down, and is said to support partial-power-down mode of system operation. This condition can occur when subsections of a system are powered down (partial power down) to reduce power consumption.

Figure 21 shows an output with I_{OFF} structure and a blocking diode to prevent excess current leakage.

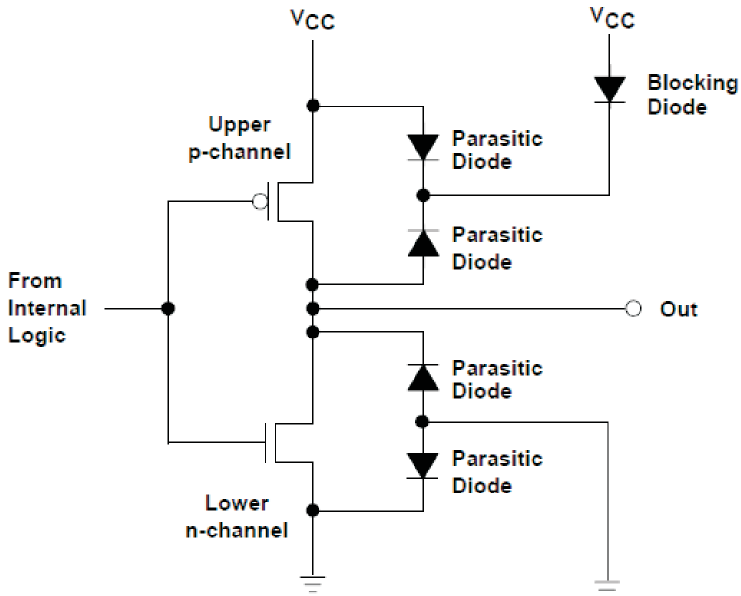


Figure 21. Typical CMOS Totem-Pole Output With I_{OFF}

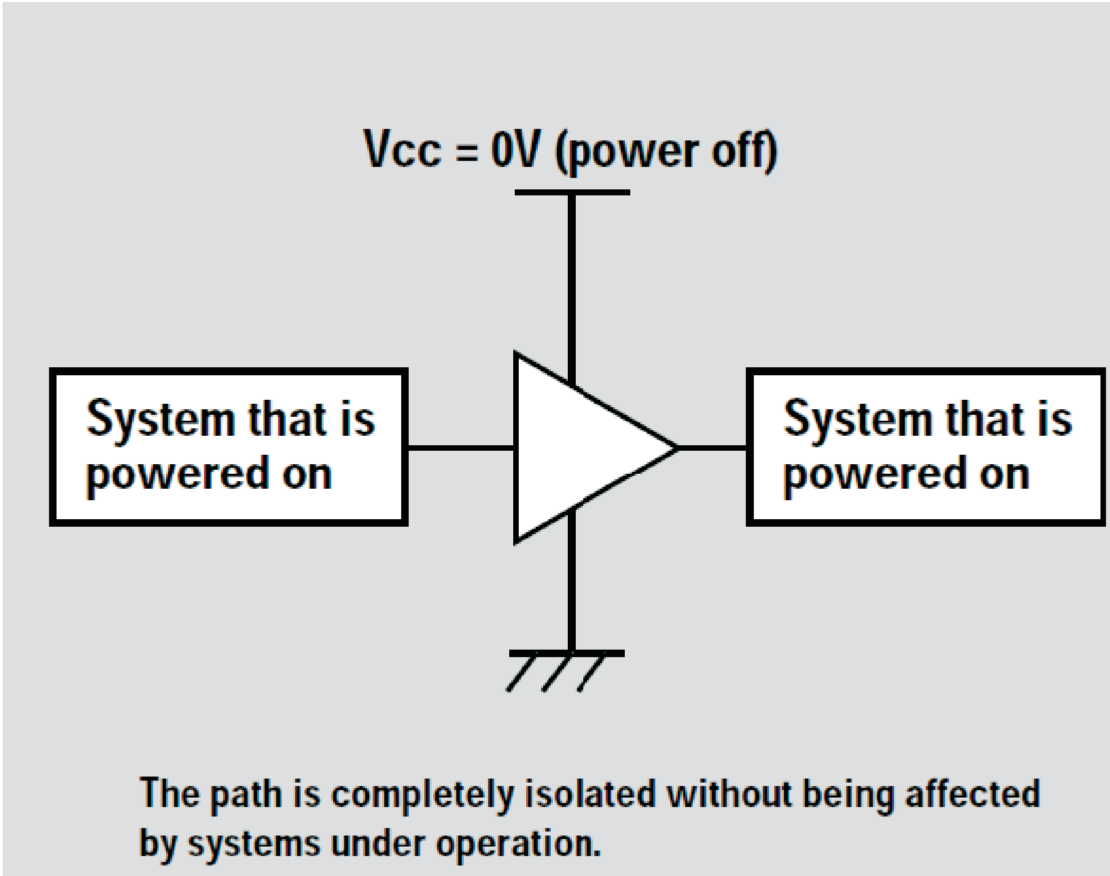


Figure 22. Typical Application With I_{OFF} Protection

3.5 Logic Compatibility

Logic compatibility has become more prevalent since the first 3.3-V logic devices were introduced into the market, thus creating an evolutionary trend in logic ICs. This trend demands that lower power-supply-voltage devices have the capability to communicate with older 5-V devices or lower 1.8-V devices. In time, power-supply nodes have decreased even further mainly due to power-consumption reduction. This reduction in supply nodes, coupled with the fact that 5-V systems are not only still in use, but thriving, has forced logic manufacturers to provide logic devices that are compatible with technologies from several different output-voltage levels.

If the output dc steady-state logic-high and logic-low voltage levels (V_{OH} and V_{OL}) are outside of the minimum V_{IH} and maximum V_{OL} range of an input port, in general, one can consider these ports compatible (see Figure 23).

If so, the SN74AUP1T translator gate is using a hysteresis circuit to set V_{IH} and V_{IL} at lower levels to get the 1.8-V, 2.5-V, and 3.3-V dc input logic level.

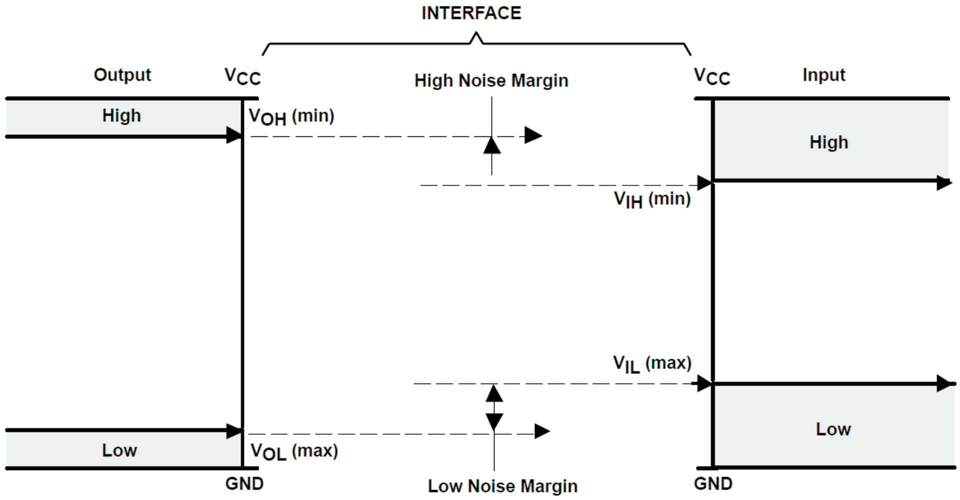


Figure 23. Logic Compatibility Between I/Os

3.5.1 Control Pin on Little Logic

For the most part, control signals on Little Logic devices are the enable (EN) pin and direction-control (DIR) pin. The enable pin is used enable or disable all outputs and the direction-control pin controls the direction of the bidirectional bus-transceiver function.

All control signals must be referenced to supply V_{CC} and the input signal is almost the same as input levels of V_{IH} and V_{IL}. Most of the control pins are connected to the processor GPIO. Faulty design would lead to an excess supply-current draw.

As shown in Figure 24, the control block is built using CMOS logic circuitry and, therefore, is susceptible to this same current consumption issue if the control input voltage is not at the rails (V_{CC} or GND). In battery-operated applications, any extra current consumption is not tolerated, so this issue must be understood and addressed from the start of system design.

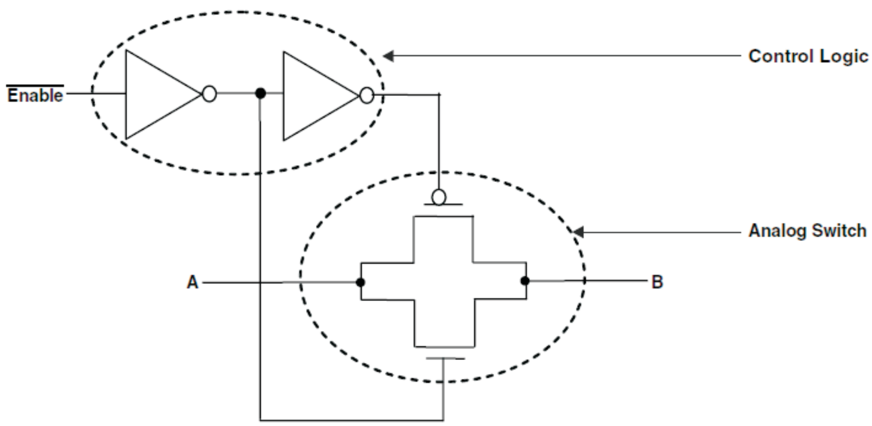


Figure 24. Typical Analog Switch Internal Struction

System designers will occasionally add pullup resistors on control pins to set the defalt level. The pullup resistor should be tied to V_{CC} and should not exceed the input tolerance.

Do not use a pullup resistor to connect the V_{CC} level that is lower than the V_{CC} level of the device; it causes excess current consumption.

4 System Applications of Little Logic Gates

Little Logic consists not only of standard gate buffer devices, but includes analog and digital switches. The gate functions can be grouped as:

Gates
- Two Inputs
- Three Inputs

Buffers/Inverters
- Schmitt-Trigger Inputs
- 3-State Buffer/Inverters
- Open-Drain Outputs

Level Shifters
- Dual-Power Rails
- Gate Translation
- Configurable Gate Translation

Signal Switches
- Digital Switches
- SPST Analog Switches
- SPDT Analog Switches

Miscellaneous Functions
- Buffer Multiplexers
- Decoders
- Latches/Flip Flops

4.1 Gates

The main gate functions are NAND (00), NOR (02), AND (08), OR (32), and XOR (86) and they can be two or three inputs. The single 2-input gates are general purpose and common devices in a system.

Table 7 shows 2- and 3-input gate selections for several product families.

Table 7. 2-Input/3-Input Gate Selection

	SN74AHCT1G	SN74AHC1G	SN74LVC1G	SN74AUP1G	SN74AUC1G
Single 2-Input NAND Gate (00)	√	√	√	√	√
Single 2 Input NOR Gate (02)	√	√	√	√	√
Single 2-Input AND Gate (08)	√	√	√	√	√
Single 2-Input OR Gate (32)	√	√	√	√	√
Single 2-Input NAND Gate w/Open-Drain Output (38)			√		
Single 2-Input Exclusive OR Gate (86)	√	√	√		√
	SN74LVC2G	SN74AUP2G	SN74AUC2G		
Single 2-Input NAND Gate (00)	√	√	√		
Single 2-Input NOR Gate (02)	√	√	√		
Single 2-Input AND Gate (08)	√	√	√		
Single 2-Input OR Gate (32)	√	√	√		
Single 2-Input NAND Gate w/Open-Drain Output (38)	√				
Single 2-Input Exclusive OR Gate (86)	√		√		
	SN74LVC1G	SN74AUP1G			
Single 3-Input NAND Gate (10)	√	√			
Single 3-Input AND Gate(11)	√				
Single 3-Input NOR Gate (27)	√				
Single 3-Input OR Gate (332)	√	√			
Single 3-Input Exclusive-OR Gate (386)	√				
Single 3-Input Positive AND-OR Gate (0832)	√				

Table 7. 2-Input/3-Input Gate Selection (continued)

	SN74AHCT1G	SN74AHC1G	SN74LVC1G	SN74AUP1G	SN74AUC1G
Single 3-Input Positive OR-AND Gate (3208)	√				

4.2 Signal Switches

TI offers different technology for signal switching in different signal applications. Table 8 can be used to select the appropriate products for an application.

Table 8. Signal-Switch Selection

DEVICE	V_{CC} NODES	TYPE	I/O INPUT TOLERANT	DATA I/O	RECOMMENDED APPLICATION
SN74CBT1G125 SN74CBT1G384	5 V	SPST	5 V	0 V to 4 V	High-speed signals, video signals of VGA type, S-video, components, etc.
SN74CBTD1G125 SN74CBTD1G384	5 V	SPST	5 V	0 V to 3.3 V	Signal translation from 5 V to 3.3 V maximum
SN74CB3T1G125	2.5 V 3.3 V	SPST	5 V	0 V to V_{CC}	Signal translation to V_{CC} maximum level
SN74CBTLV1G125	2.5 V 3.3 V	SPST	V_{CC}	0 V to V_{CC}	Audio signal, digital signal by using lower r_{ON} and $r_{ON\ flat}$
SN74LVC1G66 SN74LVC2G66	1.65 V ≈ 5 V	SPST	V_{CC}	0 V to V_{CC}	Audio signal, digital signal within 0 to V_{CC} range
SN74AUC1G66 SN74AUC2G66	0.8 V ≈ 2.7 V	SPST	V_{CC}	0 V to V_{CC}	Optimized in 1.8-V signal range and low dc signal and audio
SN74LVC1G3157	1.65 V ≈ 5 V	SPDT	V_{CC}	0 V to V_{CC}	Audio signal, digital signal within 0 to V_{CC} range
SN74AUC2G53	0.8 V ≈ 2.7 V	SPDT	V_{CC}	0 to V_{CC}	Optimized in 1.8-V signal range and low dc signal and audio

4.3 Buffers and Inverters

Logic buffers have many uses in digital electronic circuit design as they can be used to isolate other gates from each other, or they can be used to drive high current loads because their output drive capability is higher than their input signal. In other words, they have a high fanout capability and drive more than a single node.

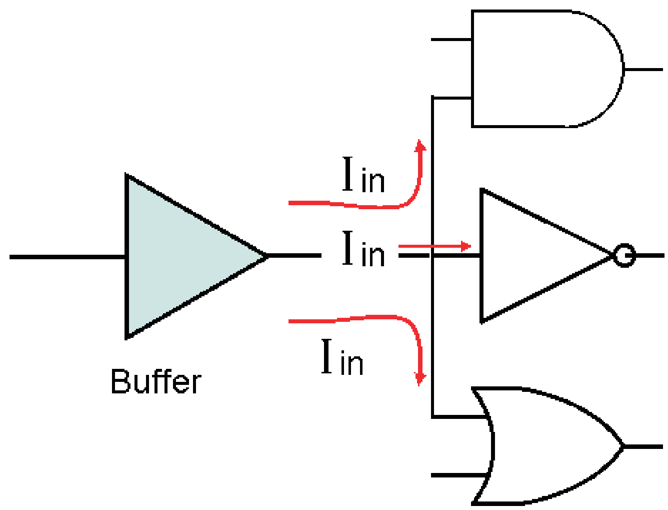


Figure 25. Logic Buffer Driving 3-Gate Inputs

The 3-state buffer is another type of logic buffer whose output can be disconnected or set to high impedance. This type of buffer is known as a 3-state output buffer.

There are two different types of 3-state output buffers - one whose output is controlled by an active high and the other is controlled by active-low control signals.

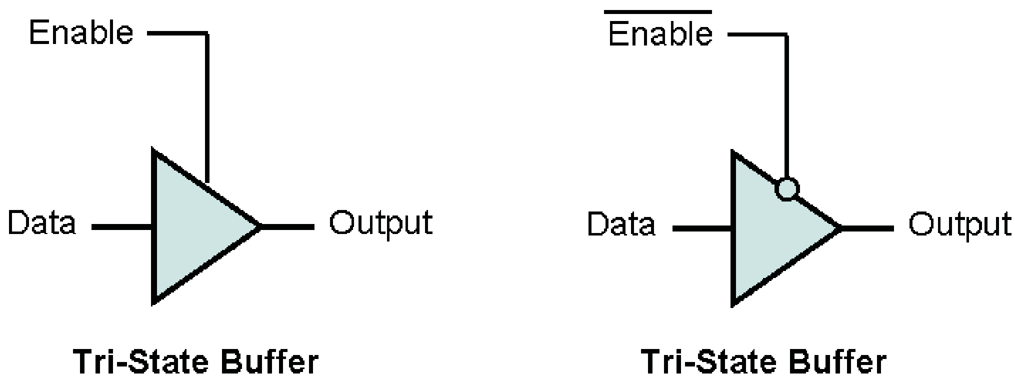


Figure 26. Logic Buffer with 3-State Output

TI offers several types of gate functions with 3-state outputs by noninverted or inverted output. Table 9 Figure 27 provides information for buffer selection.

Table 9. Buffer Selection

INPUT (DATA)		OUTPUT (DATA)		INVERTER	NON-INVERTER	NAND	3-STATE OUTPUT	DEVICE	AHCxG	AHCTxG	LVCxG	AUPxG	AUCxG	AUPxT
TTL/ CMOS	SCHMITT TRIGGER	TTL/ CMOS	OPEN DRAIN											
	√	√			√			17			•	•	•	•
	√	√		√				14	•	•	•	•	•	•
√		√			√		√	125 126	•	•	•	•	•	•
√		√			√		√	240			•	•	•	
√			√	√				06			•	•	•	
√			√		√			07			•	•	•	
√			√			√		38			•			

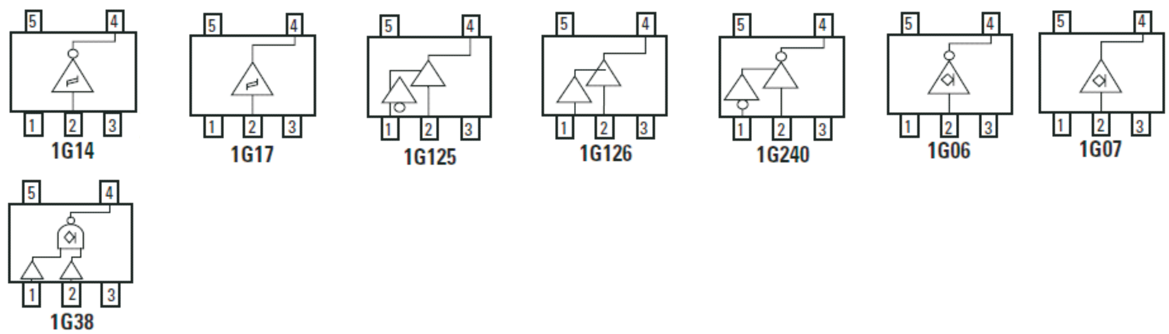


Figure 27. Buffer Selection

4.4 *Miscellaneous Functions*

The Little Logic family offers not only standard gates of AND, NAND, OR, NOR, etc., but also other useful special functions of buffer multiplexer outputs, and decoder and latches/flip-flop gates for fixing the system to manage the digital circuit.

The buffer multiplexer is a useful gate managing unlimited control pins to select the desired control signal. Figure 28 shows a typical example of using different multiplexers.

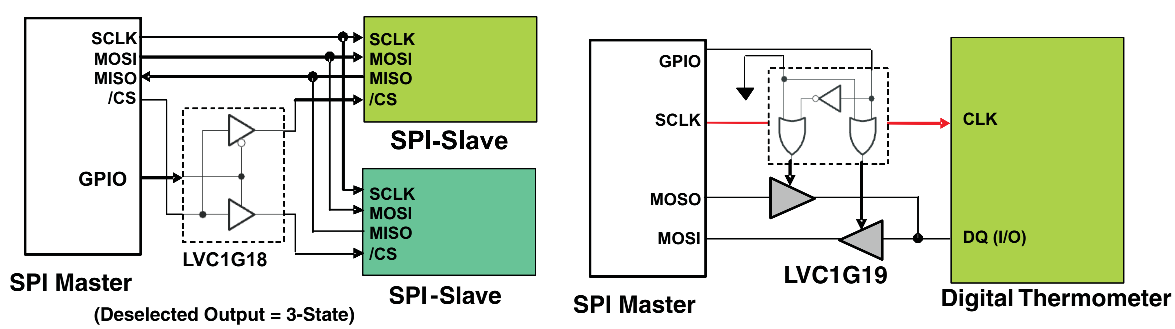


Figure 28. Typical Design Example With Buffer Multiplexer

Section 4.4 provides selection guidelines for buffer multiplexer outputs.

Table 10. Buffer Multiplexer Output Selection

	OUTPUT	SN74LVC1G	SN74LVC2G	SN74AUP1G	SN74AUC1G
1 to 2 MUX (18)	3-state	√		√	
1 to 2 MUX (19)	Buffer	√		√	√
2 of 3 MUX (29)	Buffer/decode	√		√	
2 of 4 MUX (139)	Buffer/decode	√		√	
2 to 1 Selector (157)	Buffer	√	√		

TI offers several selections of latch/flip-flop gate functions and the SN74LVC1G373 is useful in memory applications to manage read/write with latched output. The latched output is showing *high* or *low* when the latch-enable (LE) control pin is enabled, and it decreases memory corruption by malfunction of floating or unstable switching levels caused by battery drop (see Figure 29).

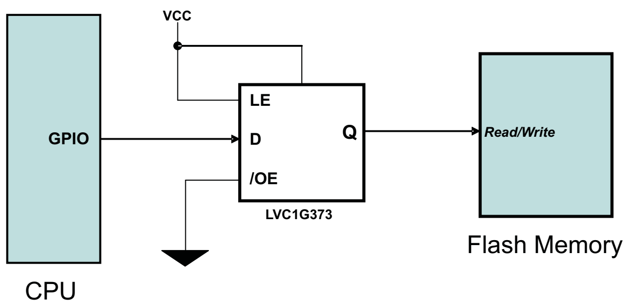


Figure 29. Typical Design Example With D-Latch

4.5 Level Shifter

5 Little Logic Package Options/Trend

This section contains a top-view illustration of the package pinout(s) and a bottom view of certain nonleaded packages. Semiconductor packaging information, including package dimensions, is available on ti.com.

5.1 Package Symbol Identification

TI Little Logic has many package options that can be selected, and each package has its own representative letters as shown in Figure 30.

In general, Little Logic family has 4-, 5-, 6-, and 8-pin packages. Most 5- and 6-pin packages have the same dimension or size.

SN74 AUP 1G 00 DSF R

DBV	5/6Leads SOT-23
DCK	5/6Leads SC-70
DPW	5Leads X2QFN
DRL	5/6Leads SOT553/563
YZP	5/6/8 NanoStar™
YFP	4/5/6/8 NanoStar™
YZV	4Leads DSBGA
DRY	5/6 QFN
DCT	8Leads SM8
DCU	8Leads US8
DSF	5/6Leads uQFN
RSE	8Leads QFN
DQE	8Leads uQFN

Figure 30. Little Logic Package Symbol Nomenclature

5.2 *Package Dimension Comparison*

Most single-gate/channel devices are in 4-, 5-, and 6-pin packages. TI offers eight types of smaller packages as shown in Figure 31.

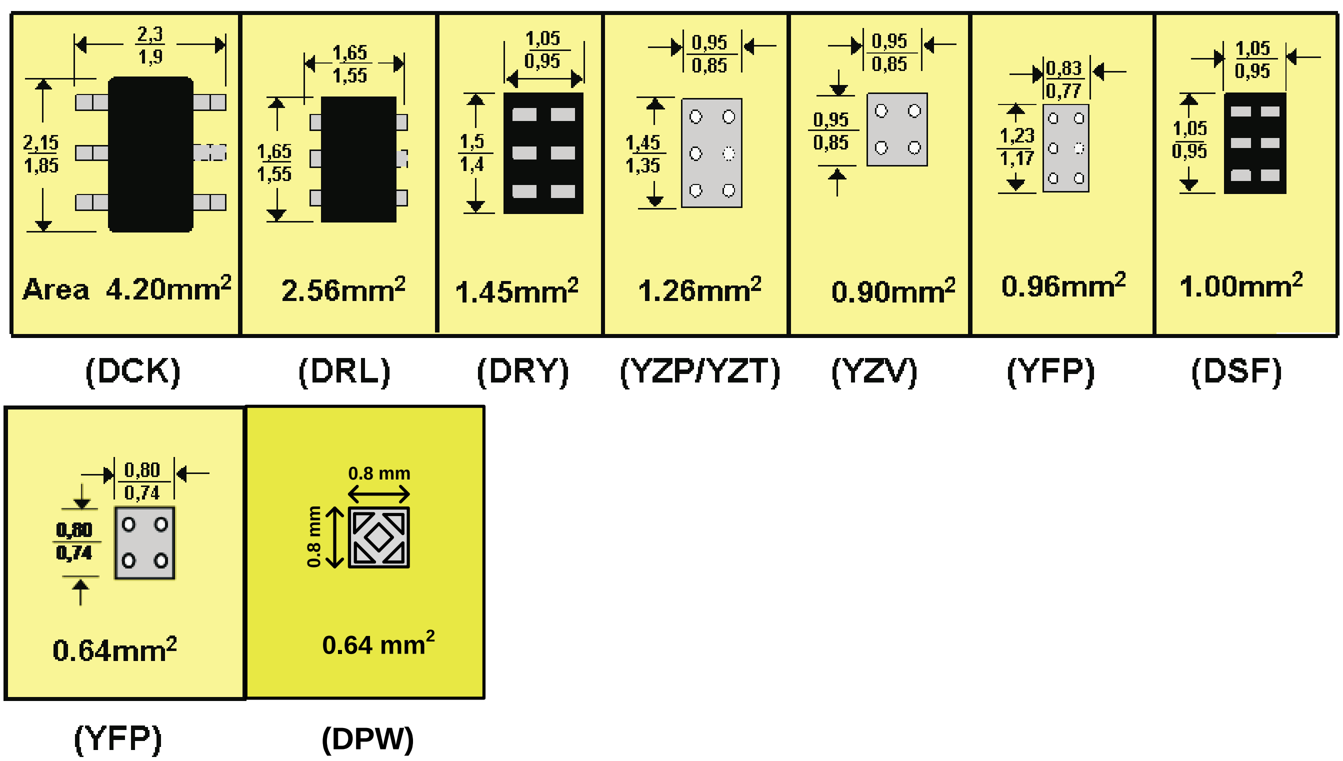


Figure 31. 4-/5-/6-Lead Package Dimensions

Most dual-gate/channel devices are in 8-pin packages as shown in Figure 32.

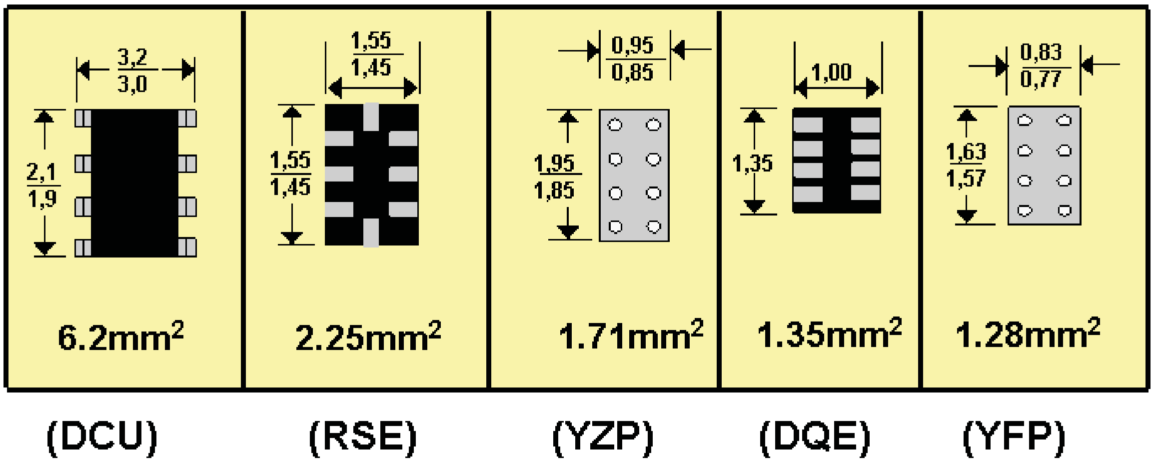


Figure 32. 8-Lead Package Dimensions

SC-70 (DCK) is mostly used for 5-6-pin single gates and US8 (DCU) is mostly used for 8-pin dual/triple gates. TI offers alternative smaller packages for two types of DSBGA (YZP, YFP) and for the µQFN (DSF/DQE) for space-conscious applications such as smartphones, slim notebooks, and portable equipment.

5.2.1 SC-70 vs YFP and DSF Packages

DSF is a micro quad flat no-lead (µQFN) package and YFP is a die-sized ball grid array (DSBGA) package, which are alternative package options for systems with space constraints to implement logic.

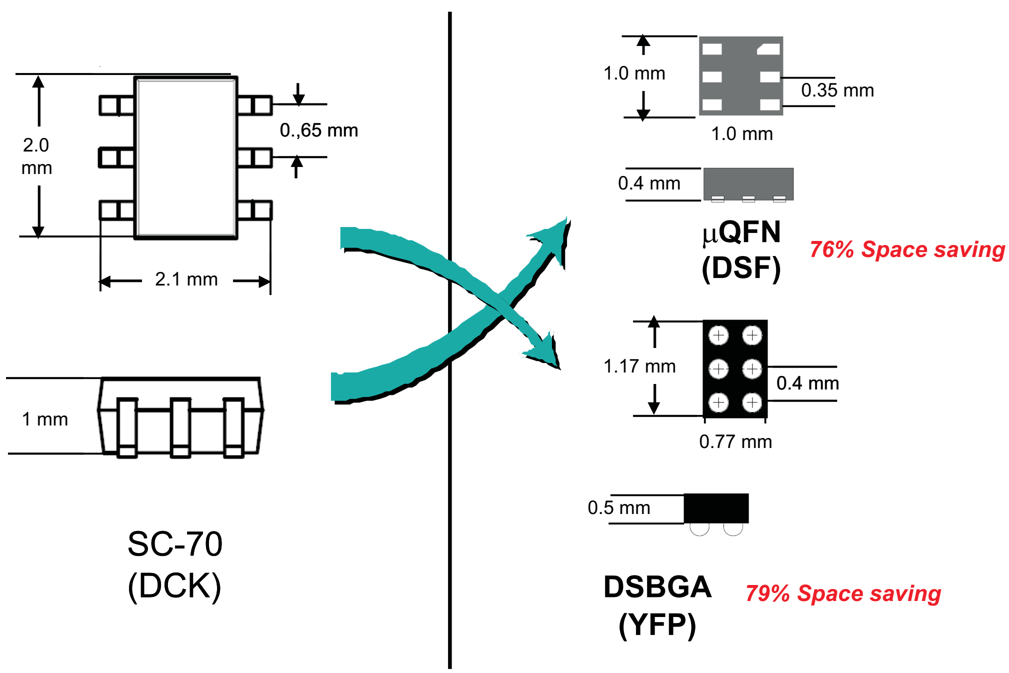


Figure 33. SC-70 vs YFP and DSF Packages

5.2.2 US8 vs YFP and DQE Packages

DQE is a µQFN package and YFP is a DSBGA package, which are alternative package options for systems with space constraints to implement logic.

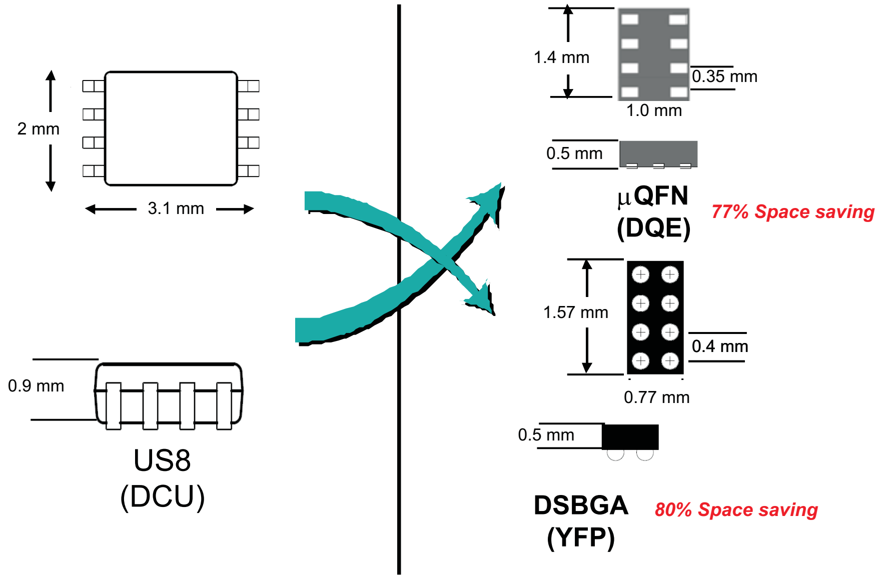


Figure 34. US8 vs YFP and DQE Package

5.3 Package Options for Little Logic

Little Logic package is becoming the industry standard and can be found at most equipment and logic suppliers by different naming systems.

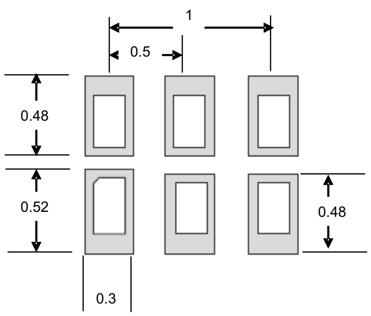
Table 11. Package Suffix Crossing

PACKAGE	TI	FAIRCHILD	ON	TOSHIBA	NXP
NanoStar™ WCSP	YZP/YFP	–	–	–	–
SOT-23 (5 pin)	DBV	M5	DT	F	GV
SC-70 (5 pin)	DCK	P5	DF	FU	GW
SOT-23 (6 pin)	DBV	DT	–	–	–
SC-70 (6 pin)	DCK	P6	DF	–	DW
SOT563 (6 pin)	DRL	–	XV5	ESV	
QFN (6 pin)	DRY	L6	MTR	–	GM
µQFN (6 pin)	DSF	FH		–	GF
NanoStar™ (4 ball)	YZP	–	–	–	–
SSOP (8 pin)	DCT	–		FU	–
VSSOP (8 pin)	DCU	K8	US	FK	DC
QFN (8 pin)	RSE	L8	–	–	GM
µQFN (8 pin)	DQE	–	–	–	–
X2QFN	DPW	–	–	–	–

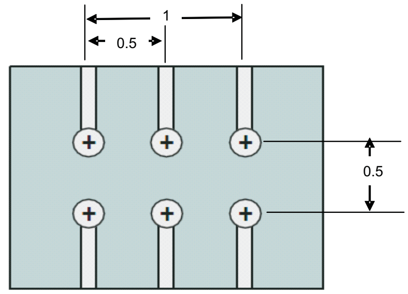
5.4 DRY (QFN) and DSBGA (YZP) Packages

DRY (QFN) and DSBGA (YZP) packages can be designed into PC boards by carefully considering each different soldering land pattern.

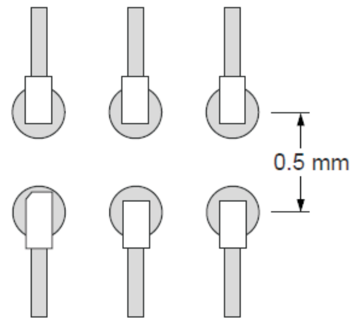
The DSBGA (YZP) package is physically smaller than DRY (QFN), but by using the DSBGA land pattern PC board, the DRY could fit in the same footprint. Figure 35 shows the solder land patterns.



DRY (QFN) Land Pattern



YZP (DSBGA) Land Pattern



Using DSBGA Land Pattern with DRY (QFN) Package

Figure 35. DRY (QFN) and YZP (DSBGA) Land Patterns

Using the DRY (QFN) land pattern for the DSBGA (YZP) is not recommended, as the DRY (QFN) requires a larger land pattern, which may cause solder starvation due to the limited solder space for DSBGA footprint coverage.

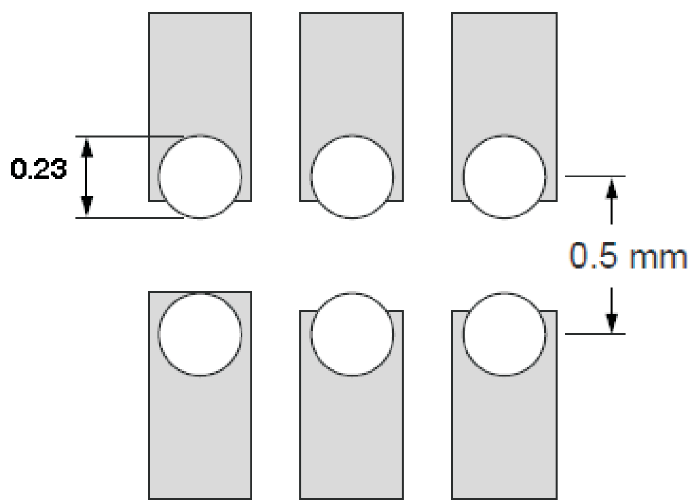


Figure 36. DRY (QFN) Land Pattern With DSBGA (YZP) Package

6 Summary

TI offers not only different product families, but also multiple packages options for any PC board design requirement.

SC-70 (DCK) is a mainstream package widely using in desktop-based PC board designs, such as computer desktops, servers, set-top boxes, and telecommunication and wireless cards.

SOP (DRL) also is a mainstream package and keeps the advantages of a lead-frame package with smaller size for manufacturing considerations.

The QFN series (DRY/6 pins, DSF/6 pins, RSE/8 pins, and DQE/8 pins) are alternative packages for space-constrained equipment including mobile smart phones, portable projectors, DVD players, and handheld equipment.

The DSBGA series (YZV/4 balls, YZP/5, 6, 8 balls, and YFP/4, 5, 6, 8 balls) are the smalles packages targeted to portable equipment.

7 References

Input and Output Characteristics of Digital Integrated Circuits (SDYA010)
Designing With TI Ultra-Low Voltage CMOS (AUC) Octal and Widebus™ Devices (SCEA033)
Selecting the Right Texas Instruments Signal Switch (SZZA030)
5-V to 3.3-V Translation With the SN74CBTD3384 (SCDA003)
Understanding and Interpreting Standard-Logic Data Sheets (SZZA036)
AHC/AHCT Designer's Guide (SCLA013)
Preventing Excess Current Consumption on Analog Switch (SCDA011)

8 Glossary

AHC — Advanced high-speed CMOS logic

AUC — Advanced ultra-low voltage CMOS logic

AUP — Advanced ultra-low power logic

CMOS — Complementary metal-oxide-silicon: a device technology that has balanced drive outputs and low power consumption

LVC — Low-voltage CMOS logic

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265