Application Brief

I3C Voltage Translator and Multiplexer Quick Reference

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Introduction

The I2C (Inter-Integrated Circuit) protocol has been instrumental in simplifying PCB communication across enterprise, personal electronics and industrial markets. However, as technology advances the demand is shifting towards a more efficient and higher performing interface. I3C (Improved Inter-Integrated Circuit) has become an important trend as I3C supports faster data rates, a fraction of the power consumption, and a new feature set for simple and flexible design. Texas Instruments offers a full portfolio of I3C compatible voltage level translators and multiplexers. This application brief summarizes the latest I3C devices in the interface product category and highlights the key system benefits of using TI I3C products.

I3C Compatible Voltage Translators

Voltage translators, or level shifters, are used to solve logic threshold incompatibilities between two voltage domains. To support the I3C standard, level translators are required to meet a 12.5MHz clock frequency and both open-drain and push-pull interface types.

Wide Voltage I3C Passive Level Translator - TCA39306

TCA39306 is a bi-directional voltage translator used to shift logic levels automatically between a controller and a target device. V_{REF1} accepts supply voltages from 0.9V to 3.3V while V_{REF2} accepts 1.8V to 5.5V. A wide supply voltage range allows TCA39306 to level shift voltage between 0.85V and 5V. Depending on the load condition, TCA39306 can achieve over 100MHz bandwidth. The device is a passive FET based translator which does not provide extra drive capabilities. While the I3C bandwidth is supported, the passive FET architecture can have limitations in some I3C use cases. Refer to section 9.3 of the device data sheet for more information (TCA39306 Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator).

TCA39306 uses external pull-up resistors giving designers the flexibility to size them based on system tradeoffs. Strong pull-ups improve I3C speeds by minimizing RC delay, whereas weak pull-ups consume less power. TCA39306 can also operate as an I3C switch when V_{REF1} and V_{REF2} are tied to GND. Device functional modes are controlled by the voltage on the enable (EN) pin. An external control signal applied to EN can then be used enable and disable the bus path.

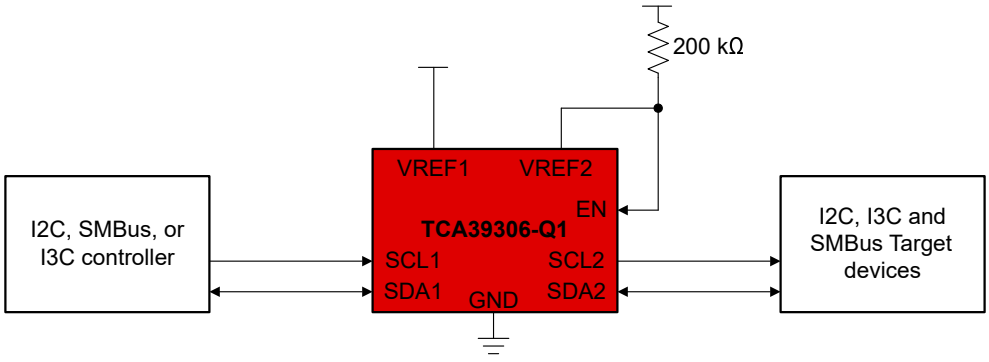

Figure 1. TCA93036 Typical I3C Application

Ultra-low Voltage MIPI I3C v1.1.1 Compatible Level Shifter with Rise Time Accelerators - TCA39416

TCA39416 is a 2-bit MIPI I3C v1.1.1 translator meeting signaling rates up to 12.5Mbps in Single Data Rate (SDR) mode and 25Mbps in High Data Rate (HDR-DDR) mode. Double data rate is achieved in HDR-DDR by sampling data on the rising and falling edge of SCL.

Processors have trended toward lower voltage nodes to maximize the processors operating performance. TCA39416's future-proofing ultra-low voltage range makes TCA39416 adaptable to 1.8V, 1.2V or even 0.8V I/O voltages with up to 10% variance. This improvement significantly reduces system power consumption and cost by avoiding high-precision power converters and LDOs. Both V_{CCA} and V_{CCB} are fully configurable from 0.72V to 1.98V providing design flexibility for V_{CC} rails. V_{CCA} and V_{CCB} can be set to the same voltage due to the symmetric supply functionality. This allows TCA39416 to provide additional drive strength, or signal boost, for I3C busses at the same voltage.

The internal architecture consists of a pass-FET with integrated Rise Time Accelerators (RTAs) and Fall Time Accelerators (FTAs). RTAs enable push-pull signaling, higher data rates, and additional drive strength required in the I3C protocol. This is accomplished by increasing the output slew rate when an input's rising edge is detected. During low-to-high transitions the output resistance is momentarily decreased by bypassing the internal pull up resistors. Both RTAs and FTAs have Gradual Turn Off (GTO) circuitry to minimize overshoots and undershoots during edge rate acceleration. This feature improves signal integrity for I3C communication especially at high transmission rates. TCA39416 also integrates 10kΩ pull up resistors on both A and B ports to help I3C system designers save on cost and board space.

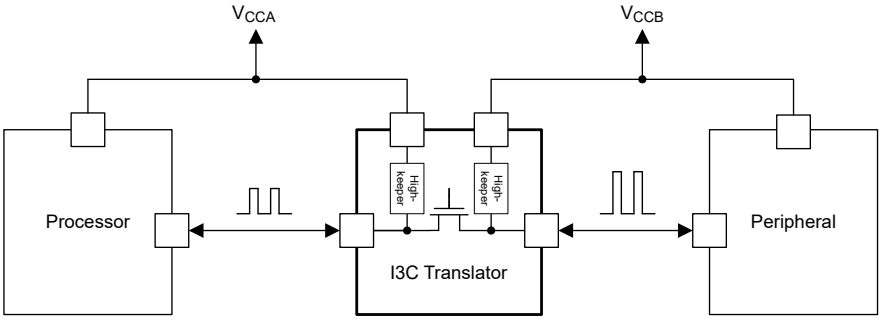

Figure 2. TCA39416 Application Diagram

Table 1. I3C Voltage Translator Summary

	TCA39306	TCA39416
Protocols Supported	I3C, I2C, SMbus	I3C, I2C, SMbus
SCL Frequency (MHz)	12.5MHz	12.5MHz
V_{CCA} (V)	0.9 – 5.5	0.72 – 1.98
V_{CCB} (V)	1.8 – 5.5	0.72 – 1.98
Supply Dependency	V_{CCA} + 0.6V ≤ V_{CCB}	V_{CCA} ≤ V_{CCB}
SDR Mode	✓	✓
HDR-DDR	✓	✓
Integrated pull-up resistor	X	✓
Hi-Z SDA and SCL pins when V_{CC}= 0V	✓	✓
Rise Time Accelerators	X	✓
Available packages (mm²)	SOT-23 (8.12mm²) VSSOP (6.2mm²) X2SON (1.08mm²)	SOT-23 (8.12mm²) X2SON (1.35mm²)

I3C Compatible Multiplexers

Multiplexers and switches are used to switch from multiple inputs and outputs. A multiplexer must support low on-resistance (R_{ON}), low on-capacitance (C_{ON}), high bandwidths and both push-pull and open-drain interfaces for I3C compatibility.

Dual 2:1 Switch Supporting Power-Off Isolation - TMUX136

TMUX136 is a dual 2:1 switch operational over 2.3V to 4.8V. Select pins are compatible with 1.8V control for easy integration with low voltage microcontrollers and processors. The switching architecture of TMUX136 consists of an NFET with a charge-pump allowing it to achieve very low 5.7Ω R_{ON} (typical), and 1.6pF C_{ON} (typical). This provides fast response times with minimal signal degradation during I3C multiplexing.

TMUX136 is rated for 5kV Human Body Model (HBM) and 1kV Charged-Device Model (CDM) ESD performance. Signal paths are isolated while TMUX136 is powered off. This protects down stream components and eliminates the need for power sequencing.

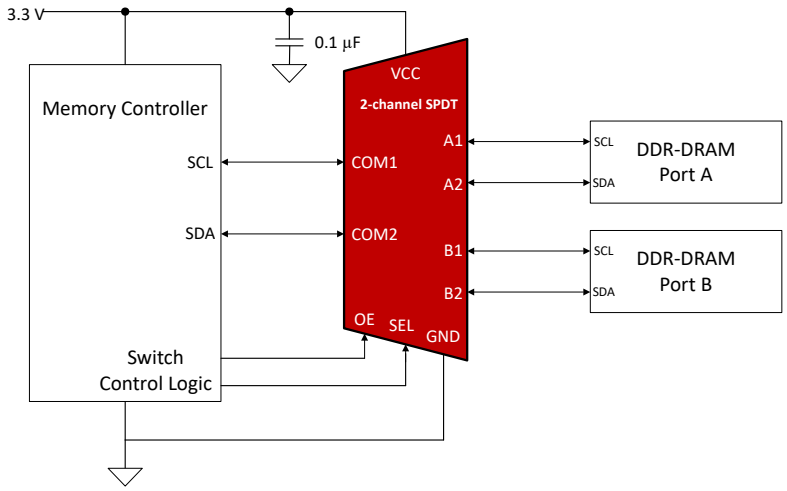

Figure 3. I3C DDR-DRAM Switch Example

High Precision Dual 2:1 Switch with Power-Off Isolation - TMUX121

The TMUX121 is a low capacitance Single Pole, Double Throw (SPDT) switch that enables bidirectional communication. The device is powered from a single 3.3V supply allowing for both 1.8V and 3.3V control of SEL and EN. TMUX121 is excellent for I3C applications due to extremely low typical R_{ON} (3Ω), C_{ON} (2pF), and T_{PD} (60ns).

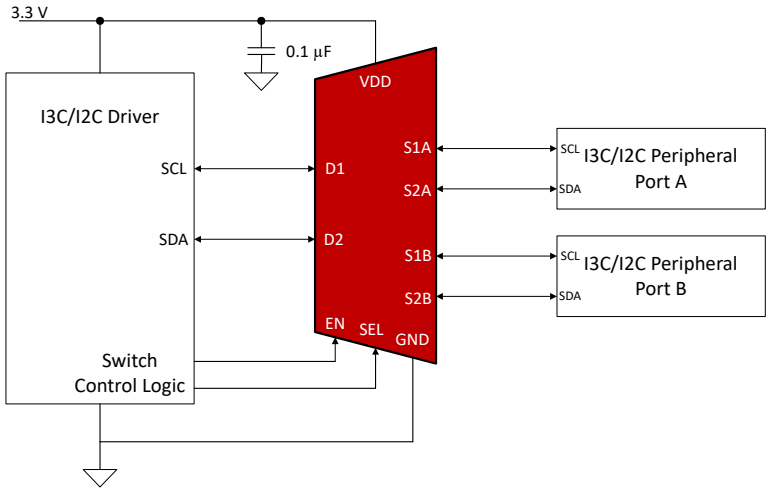

Figure 4. TMUX121 Typical I3C Application

High ESD Protected Dual 2:1 Switch with Power-Off Isolation - TMUX154E

TMUX154E is a dual channel 2:1 switch with ESD protection cells on all I/O ports. V_{CC} is supplied from 3V to 4.3V with 1.8V compatible control logic. I/O ports allow input voltages above V_{CC}. Passing I3C signals have minimal phase and edge distortion due to the 900MHz bandwidth, R_{ON} (6Ω), and C_{ON} (7.5pF).

TMUX154E is rated for 8kV Human-Body Model (HBM) and 1kV Charged-Device Model (CDM) per JESD 22. The device is also rated for high voltage ESD performance from I/O to GND up to 15kV HBM. Internal ESD protection removes the need for external protection devices minimizing cost and design size.

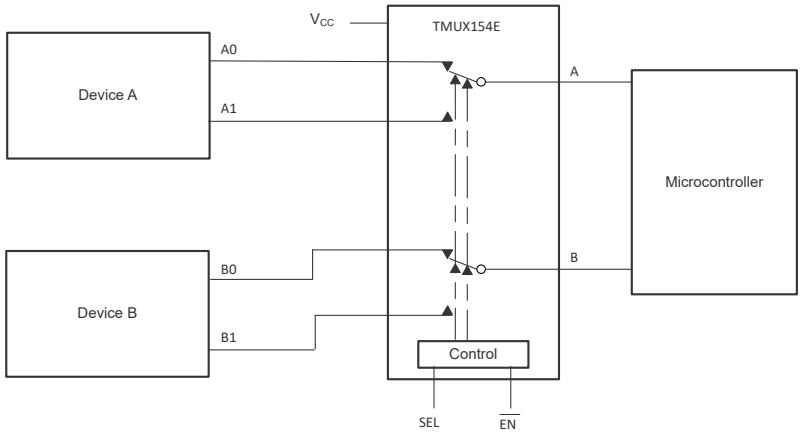

Figure 5. TMUX154E Application Diagram

Quad 2:1 Switch with Fail-safe Logic - TMUX1574

TMUX1574 supports 2Ω R_{ON}, 7.5pF C_{ON}, and a 2GHz bandwidth critical for passing I3C signals with high signal integrity. It includes four 2:1 SPDT switches permitting the device to support two separate lanes of I3C (SDA and SCL). By integrating additional channels, it reduces BOM count and simplifies PCB layout. TMUX1574 operates from a wide supply range of 1.5V to 5.5V with 1.8V compliant control inputs. TMUX1574 also features fail-safe logic which allows control inputs to support up to 5.5V regardless of V_{DD}. This feature provides flexible power sequencing, reduced BOM, and simplifies design.

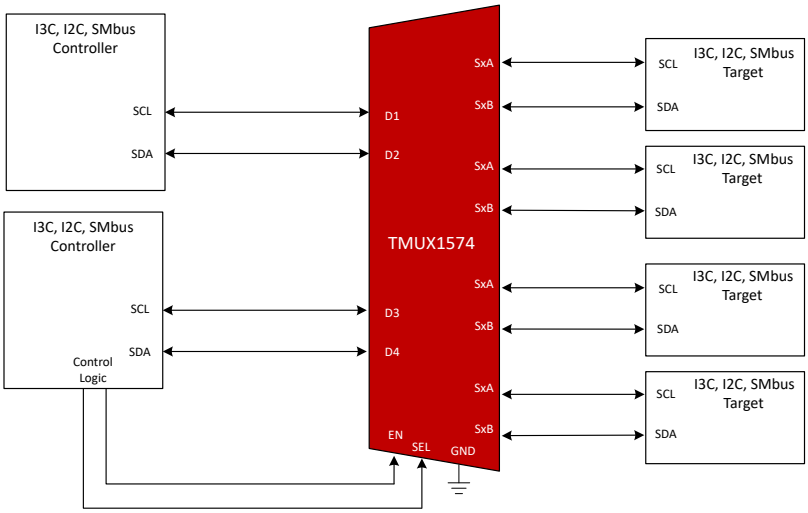

Figure 6. Multiplexing Two I3C Lanes with TMUX1574

Table 2. I3C Multiplexer Summary

	TMUX136	TMUX121	TMUX154E	TMUX1574
Supported Protocols	I3C, I2C, UART, LVDS, Analog	I3C, I2C, UART, LVDS, Analog	I3C, I2C, UART, LVDS, Analog	Analog, I2C, I2S, I3C, JTAG, MIPI, RGMII, SPI, TDM, UART
Configuration	2:1 SPDT, 2 Channel	2:1 SPDT, 2 Channel	2:1 SPDT, 2 Channel	2:1 SPDT, 4 Channel
I/O Voltage (V)	Up to 3.6	Up to 3.6	Up to 5.25	Up to 5.5
Bandwidth (MHz)	6000	3000	900	2000
Typical On-Resistance (Ω)	5.7	3	6	2
Typical Capacitance (pF)	1.5	2	7.5	7.5
I/O Power-off Protection	✓	✓	✓	✓
Interface	Push-pull Open-drain			
Available packages (mm²)	UQFN (3mm²)	UQFN (2.52mm²)	UQFN (2.52mm²)VSSOP (14.7mm²)	SOT-23 (8.4mm²) TSSOP (32mm²) UQFN (4.68mm²)

Enabling High Drive I3C Routing

One of the most important constraints with I3C is the 50pF maximum bus capacitance limit. I2C, in contrast, specifies an eight times higher limit of 400pF. Lowering the maximum load conditions severely limits the trace lengths and the number of target devices an I3C bus can manage. Multi-point communication between multiple controllers and targets adds additional challenges with signal routing, I2C/I3C addressing, and I/O voltage mismatches. These obstacles can be overcome with an I3C level shifter and multiplexer.

TCA39416 provides low voltage level shifting and signal boosting. A host processor or microcontroller operating at I/O voltages of 0.8V or 1.2V can effectively be level shifted to interface with 1.8V I3C components. The RTA circuitry enables an I3C host to provide signal boost to an I3C bus. This feature allows the host device to drive higher capacitive loads.

A controller can communicate to multiple I3C peripherals by utilizing an I3C multiplexer. The multiplexer provides three key advantages. First, multiplexers simplify I3C signal routing by allowing one controller to interface with multiple devices downstream. Secondly, by switching I3C devices it isolates parasitic capacitance added by inactive targets on the bus. This allows the controller to communicate with a target while staying within the I3C loading specification. The third benefit is that multiplexing can remove conflicts if two targets share the same address. I3C is backwards compatible with I2C and a communication node can have many I2C and I3C devices.

Figure 7 shows an example application with a single I3C controller and two selectable target devices. TCA39416 and TMUX136, dual 2:1 multiplexer, provide a full system design for host and target communication by addressing the challenges with I3C. Redundancy can be added to the system by multiplexing redundant peripherals to the I3C transmission line. Multiplexing can also be implemented to provide debug port access to the bus. TCA39416 and TMUX136's ultra small package options maximize PCB area. This design provides scalability to the number of peripherals and required features. For example, swapping in TMUX1574, quad 2:1 multiplexer, doubles the I3C lanes.

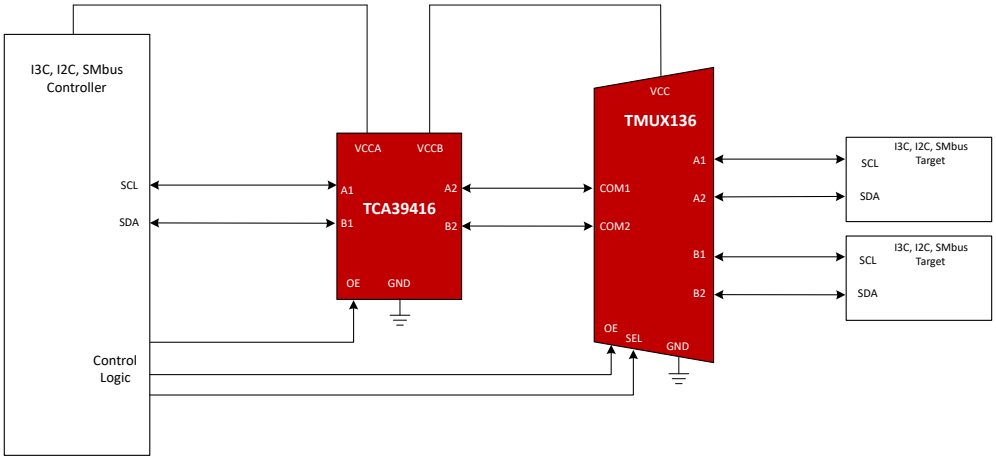

Figure 7. Flexible 2:1 I3C Bus with Signal Boost - TMUX136 + TCA39416

Some designs can require two I3C controllers to interface with the same set of peripheral devices. Crosspoints direct multiple input signals to the outputs. HDS3SS460 is a 4 x 6 passive crosspoint supporting over 5Gbps signal rates. This device can be utilized as a dual channel 2x3 I3C cross point. Functional modes for both channels are selected by the status on the POL, AMSEL, and EN pins. Each channel cannot be controlled independently. HD3SS460's low 1pF C_{ON} and 12Ω R_{ON} provide excellent I3C dynamic performance. As seen in Figure 8, one channel consists of two controllers and 3 targets. The inputs of HD3SS460 are boosted with TCA39416.

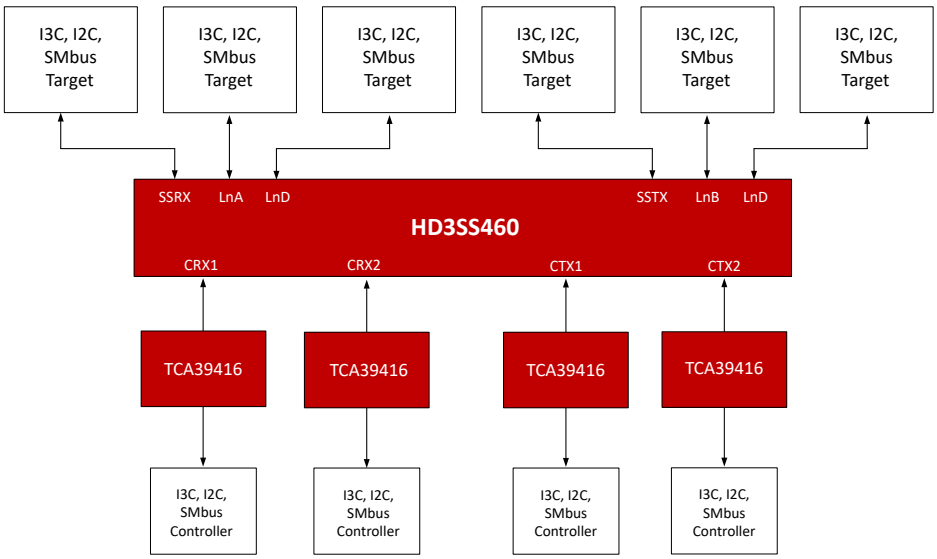

Figure 8. High Drive I3C Dual 2x3 Crosspoint - HD3SS460 + TCA39416

Conclusion

TI's comprehensive I3C level translation and multiplexing portfolios help overcome the challenges associated with designing a reliable I3C interface. Level translators are an efficient and cost effective means to resolving I/O mismatches across an I3C link. In addition, TCA39416's edge rate accelerators provide extra signal boost. Multiplexers with high dynamic switching performance simplify I3C communication by isolating bus capacitance, maximizing processor I/O pins, and introducing overall greater system reliability.

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