

## Backwards Compatibility

The I3C protocol is designed to be backwards-compatible with I2C buses. Within the I3C specification, I3C controllers are expected to be able to operate at I2C speeds of 400 kHz and 1 MHz. As the I2C specification specifies, I2C targets are expected to have a 50-ns deglitch filter on the SDA and SCL pins. I2C devices with this deglitch filter can co-exist on the I3C bus if the designer decides to design the bus this way. [Figure 1](#) shows an example of an I2C target device on an I3C bus.

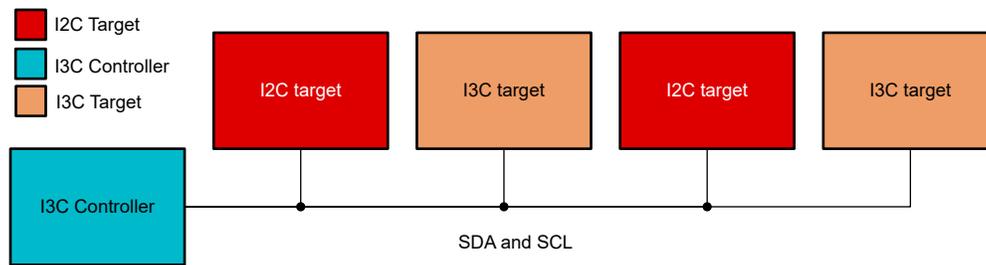


Figure 1. Shared I2C and I3C bus

## Best Practices

In most cases, the system designer does not know if the I2C target device includes the 50-ns deglitch filter. [Figure 2](#) illustrates how the designer can use an I2C switch or passive general-purpose multiplexer to segment the I3C bus.

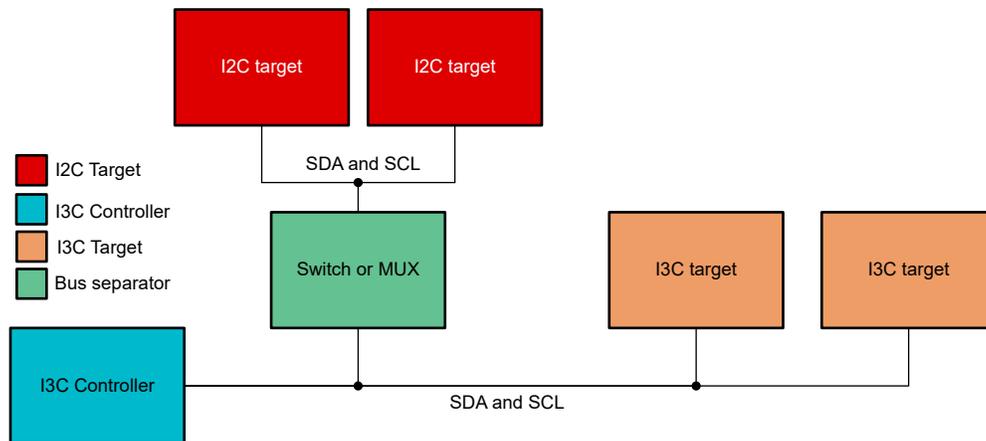


Figure 2. Segmented I2C and I3C Bus

Using a switch or MUX to segment the bus into separate I2C and I3C lanes comes with an added benefit of being able to lower the capacitive loading on the I3C bus when the switch or MUX is disabled or deactivated. This is advantageous because I3C has a capacitive loading limit of 50 pF. I2C devices can have up to 10 pF of capacitive loading which can quickly eat away at the 50-pF limit allowed. I2C-controlled switches are allowed in the I2C specification to exceed 10-pF limit.

Table 1 details a list of potential options for a switch or MUX.

**Table 1. I3C to I2C Bus Segmenting Devices**

Device Name	Type of Device	Comments	Typical Off-Capacitance
TCA39306, PCA9306	Level translator with disable feature	Disabled or deactivated by driving the EN pin low. Tri-state the EN pin to enable the device.	4 pF
TCA9800	I2C 400 kHz buffer and redriver with level translation	Disabled or deactivated by driving the EN pin low. Make the A side face the I3C bus. Disable this device during I3C communication.	2 pF on the A side
TCA9548A	8-channel, I2C switch with level translation	I2C-controlled and includes 50-ns deglitch filter on SDA and SCL. Set downstream channels to disabled during I3C communication.	20 pF
TCA9546A	4-channel, I2C switch with level translation	I2C-controlled and includes 50-ns deglitch filter on SDA and SCL. Set downstream channels to disabled during I3C communication.	15 pF
TCA9543A	2-channel, I2C switch with level translation	I2C-controlled and includes 50-ns deglitch filter on SDA and SCL. Set downstream channels to disabled during I3C communication.	15 pF
TMUX136	2-channel, 2:1, I3C passive multiplexer	I3C- and I2C-compatible passive multiplexer. 1.6-pF on-capacitance, 5.7-Ω on-resistance, 6-GHz bandwidth with powered-off protection. Optimized for flow-through PCB routing.	1.5 pF
TMUX154E	2-channel, 2:1, I3C passive multiplexer	I3C- and I2C-compatible passive multiplexer. 7.5-pF on-capacitance, 6-Ω on-resistance, 900-MHz bandwidth with powered-off protection.	2 pF

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