Application Brief
I3C – Next Generation Serial Communication Interface

TEXAS INSTRUMENTS

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I^2C and SPI have long been the primary interface choice for embedded devices. While these interfaces are relatively simple to implement and have been widely adopted over the years, they both lack some critical features and have limitations. This applies especially for deeply-embedded applications, which can significantly impact designing densely packed systems. In I^2C, these limitations include a 7-bit fixed address that can cause collisions on I^2C buses, no in-band interrupt or target resets (requires additional wires/pins), limited data rate, and the ability of targets to stretch the clock (potentially hanging up the system in long connected sessions). In SPI, some of the major limitations are a requirement for four communication lines with one Chip Select pin per device and many different implementations, due to the lack of a clearly defined standard.

As smart phones, wearables, IoT (Internet of Things) devices, systems in automobiles and server environments become more advanced and complex, the necessity for more streamlined, high performance, scalable and cost-effective communication interfaces are required to control and transmit data with high speeds, in energy-saving and space-saving designs.

I3C (Improved-Inter Integrated Circuit) aims both to fix the limitations of legacy interfaces (I^2C and SPI) and to also add other enhancements. I3C specification developed by MIPI Alliance [1] , is an intelligent multi-featured interface that improves upon the key attributes of traditional I^2C and SPI interfaces to provide a new, unified, and high-performing solution. I3C is a serial communication interface implemented using a complementary metal oxide semiconductor (CMOS) I/O, which uses a two-wire interface to minimize pin counts and number of signal paths between components. It enables the use of higher bandwidth operating modesat very low power levels and allows simpler, yet more flexible design implementation. The I3C standard is designed to retain some backward compatibility with the I²C system, notably allowing designs where existing I²C devices can be connected to an I3C bus, but still supports the ability to switch to a higher data rate for communication at higher speeds between compliant I3C devices.

Figure 1 compares the energy consumption (per bit) of the various MIPI I3C modes with I²C (left) and the corresponding raw bitrates (right) [2].
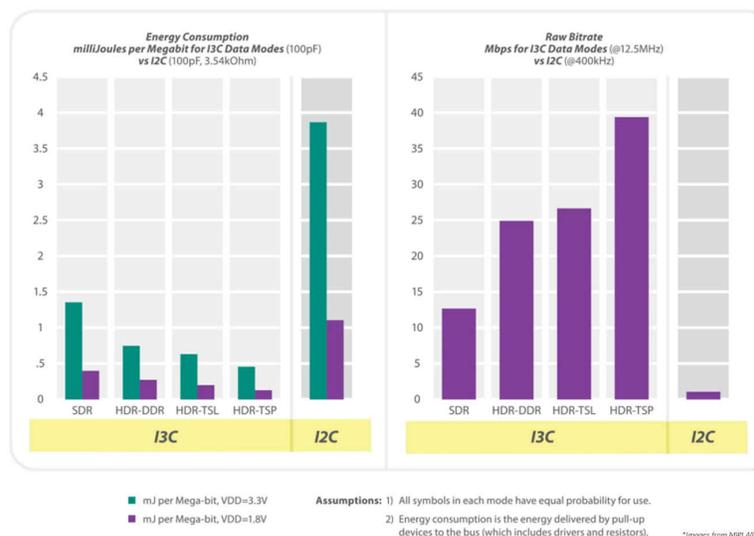

Figure 1. I3C vs. I²C Energy Consumption Per Bit at Higher Data Rates

MIPI I3C was initially intended for mobile applications as a single interface that could be used for all digitally interfaced sensors. However, it is now intended for all mid-speed embedded and deeply-embedded applications, also including a broader set of use cases and industries such as memory management, server control as well as enterprise, factory automation, and communications equipment. Figure 2 summarizes key features of I3C interface.
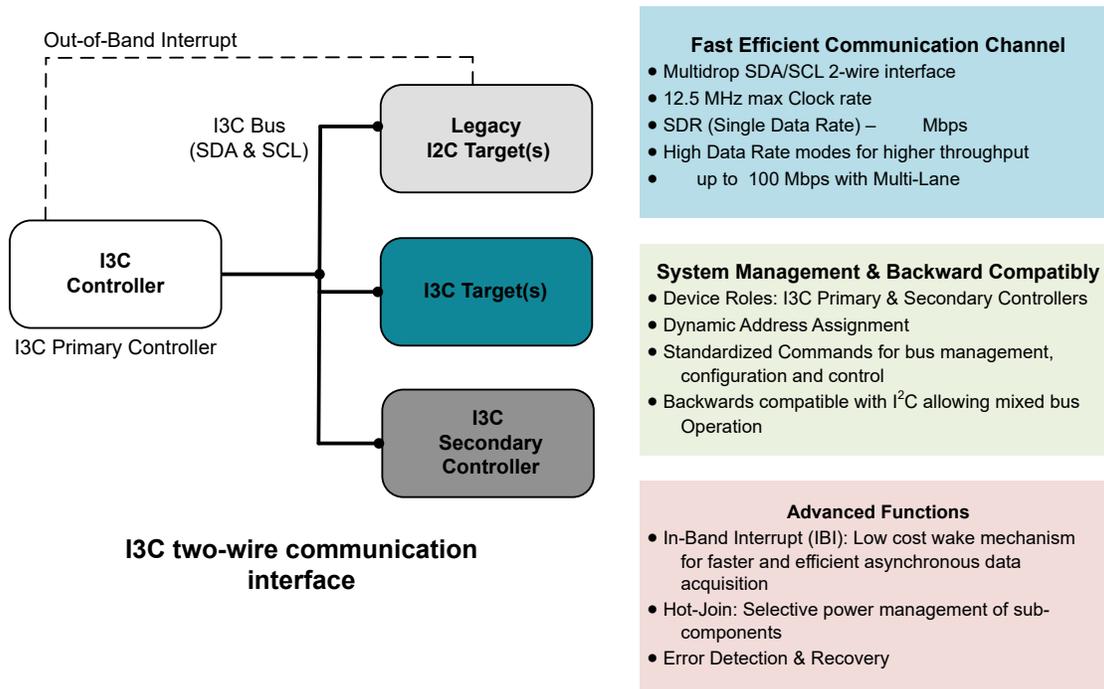
Fast Efficient Communication Channel
- Multidrop SDA/SCL 2-wire interface
- 12.5 MHz max Clock rate
- SDR (Single Data Rate) –   Mbps
- High Data Rate modes for higher throughput
-        up to 100 Mbps with Multi-Lane

System Management & Backward Compatibly
- Device Roles: I3C Primary & Secondary Controllers
- Dynamic Address Assignment
- Standardized Commands for bus management, configuration and control
- Backwards compatible with I^{2}C allowing mixed bus Operation

Advanced Functions
- In-Band Interrupt (IBI): Low cost wake mechanism for faster and efficient asynchronous data acquisition
- Hot-Join: Selective power management of sub-components
- Error Detection & Recovery

I3C two-wire communication interface

Figure 2. MIPI I3C Standardized Interface – Key Features

A few end-equipment applications highlighting key I3C features are referenced:

- Typical smart phones and IoT devices may have a combination of I2C and SPI devices, with four wires for SPI, two wires for I2C, plus an interrupt line for each peripheral device. Additional devices require more logic lines and increase the overall power consumption. I3C provides *In-Band Interrupt* capability that offers low-cost wake mechanism, which is where I3C targets can request an interrupt when the bus is idle; a design that eliminates the need for a separate general-purpose input/output (GPIO) for each target and thus reduces system cost and complexity. I3C also introduces *dynamic addressing*, this is important when changing the priority of a target device so that In-Band Interrupt from the device can be increased or decreased.

- In most PC/Motherboard applications, I3C devices are used where there may be multiple controllers, a large number of endpoint devices, and long traces – all of which can impact bus complexity and signal integrity. I3C's *Multi-Controller and Multi-drop* capabilities, with a well-defined protocol for hand-off between Controllers, provides the ability for devices on the bus to request to take the Controller role. This is so that the bus architecture is not limited to one single fixed Controller device and a number of target devices.

- In I3C, targets are allowed to join the bus after it has already been configured and are assigned a dynamic address by the I3C Controller. With this *Hot-Join* capability in I3C, some devices on the bus can be turned on and off during operation that allows "power segmented" designs, by keeping units active only when needed. This feature is important in applications when powering down a system that may be undesirable, not possible (such as in servers or wireless base stations) or where a hot insertion feature has to be properly designed, which is either in the backplane or the external card.

- DDR5 also uses MIPI I3C as one of the core technologies. Using MIPI I3C instead of I2C, DDR5 offers memory bandwidth improvements, enabling the next generation of high-performance systems and applications, including client systems and high-performance servers. I3C offers a typical data rate of 10 Mbps with options for higher-performance, *High Data Rate (HDR)* Modes that provide speeds in excess of 30 Mbps (for single-lane mode) and 100 Mbps (with quad-lane).

The MIPI I3C Bus interface is an evolutionary specification, that dramatically enhances the speed and flexibility of legacy interfaces, simplifying the development of innovative designs for products such as smartphones, wearables, systems in automobiles and server environments. As the protocol is gaining momentum, migration to the I3C interface enables devices to achieve higher performance with better system management and configuration. This enables I3C as the mainstream technology in enterprise and computing, PC and notebooks as well as automotive and many other applications

References

1. *MIPI Alliance Specification for I3C® (Improved Inter Integrated Circuit)*, version 1.1.1, MIPI Alliance, Inc., 11 June 2021.
2. *MIPI Alliance "Introduction to the MIPI I3C Standardized Sensor Interface", August 2016*

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