Application Brief

Edge and Frequency Detection in TI Programmable Logic Devices

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Introduction

Signal edge detection is an application used across many platforms, from PWM modulation in traction inverter systems to result capture and triggering in test and measurement equipment. Similarly, frequency detection can be used to regulate speeds of motors, sensors, and other devices by comparing the frequency of these devices to a safe reference frequency and using the result to adjust the system accordingly. TI programmable logic devices (TPLD) are able to perform both edge and frequency detection of logic-level signals. While TPLD can implement discrete edge and frequency detection circuits through use of integrated lookup tables (LUTs), this article focuses on the functionality of TPLD edge detect and frequency detect modules.

Programmable Filter, Edge Detect, Deglitch Filter

The programmable filter (PFLT), edge detect (EDET), and deglitch filter (FILTER) modules, shown in Figure 1, all function the same way in terms of edge detection. Each module can be configured to detect the rising edge, falling edge, or both edges of the incoming input signal. When the appropriate edge is detected, the module outputs a short pulse. When using the PFLT module, this pulse is approximately the length of the selected RC delay, determined by the PFLT *Delay Time* option. When using the EDET or FILTER modules, the pulse length is limited to that of the first RC delay of the PFLT module. The EDET and FILTER both have an option for inverted output. Although the EDET module instantiates the internal oscillator upon being selected, the oscillator is not necessary for the EDET to operate properly and thus can be powered down if not being used elsewhere. Simulation of both edge detection using the PFLT module is shown in Figure 2, where the output of the programmable filter is provided in blue and the input is shown in orange.

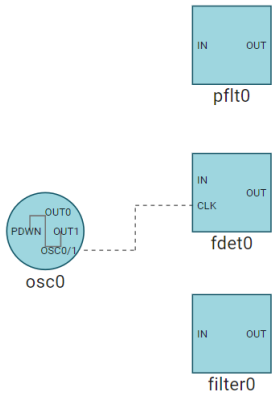

Figure 1. Programmable Filter, Edge Detect, and Deglitch Filter Modules

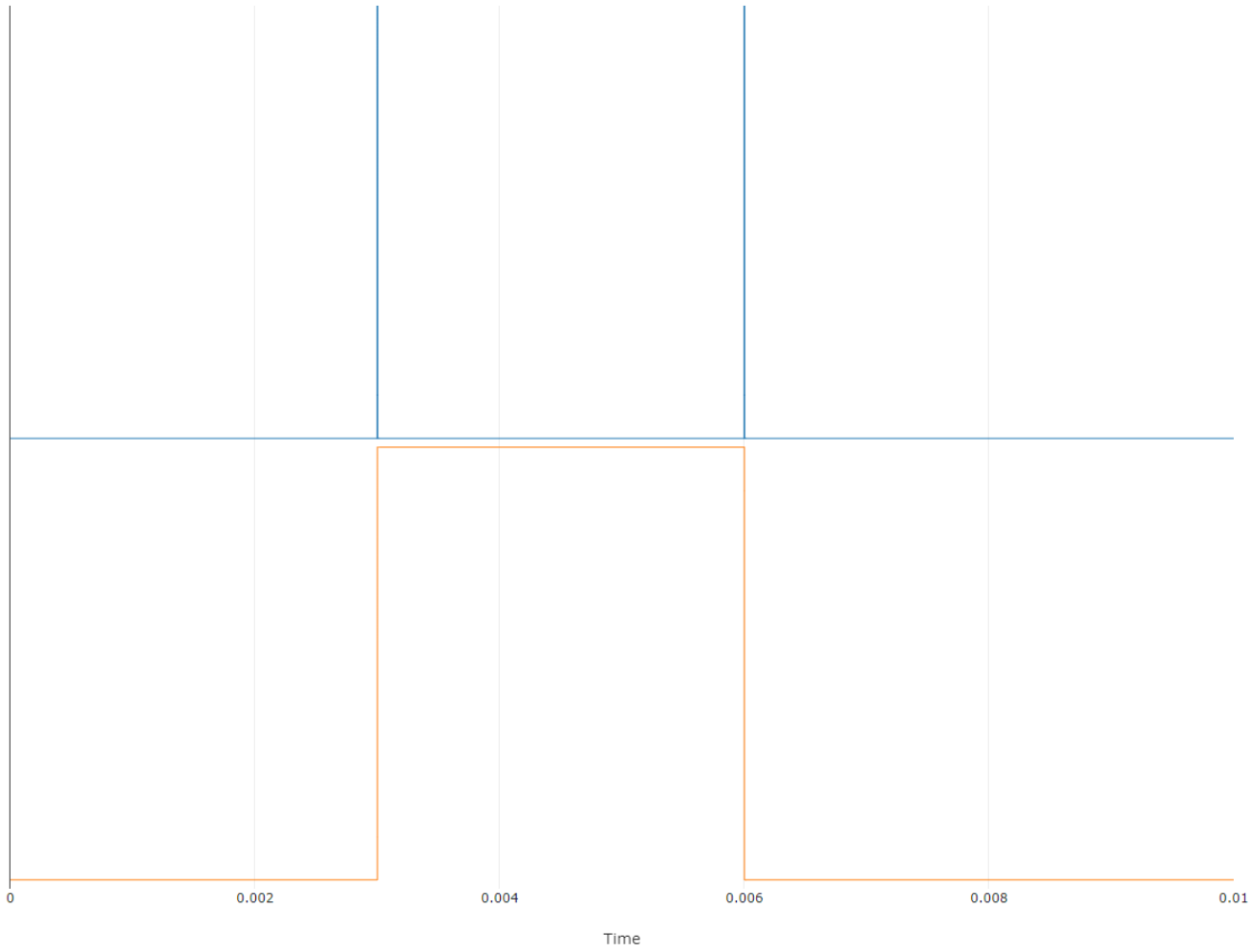

Figure 2. Programmable Filter Both Edge Detect Simulation

Delayed Edge Detect

Depending on the specific TPLD, some delay modules have an option for *Delayed Edge Detector*. The module and this option are shown in Figure 3. When the module is set to delayed edge detect mode, the *Delay Mode* option is used to select whether the rising, falling, or both edges of the incoming input signal are detected. The delay module then operates similarly to the EDET module described in Programmable Filter, Edge Detect, Deglitch Filter, except the output pulses are delayed by an amount of clock cycles determined by the *Control Data* setting. A simulation of the delay module in delayed edge detect mode, delaying both edges with control data of 3, is shown in Figure 4. The clock signal into the DLY module is shown in blue, the input is orange, and the delayed edge detect output is shown in green. Notice that the delay pulses appear five clock signals after the initial edge is detected (the two extra clock signals are due to the delay two D Flip Flop sync on the input).

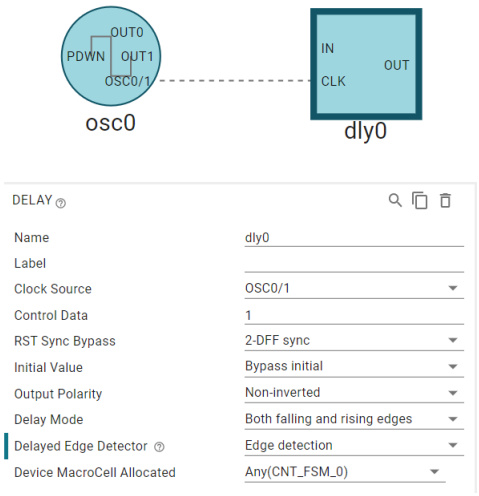

Figure 3. Delay Module With Configuration Options in InterConnect Studio (ICS)

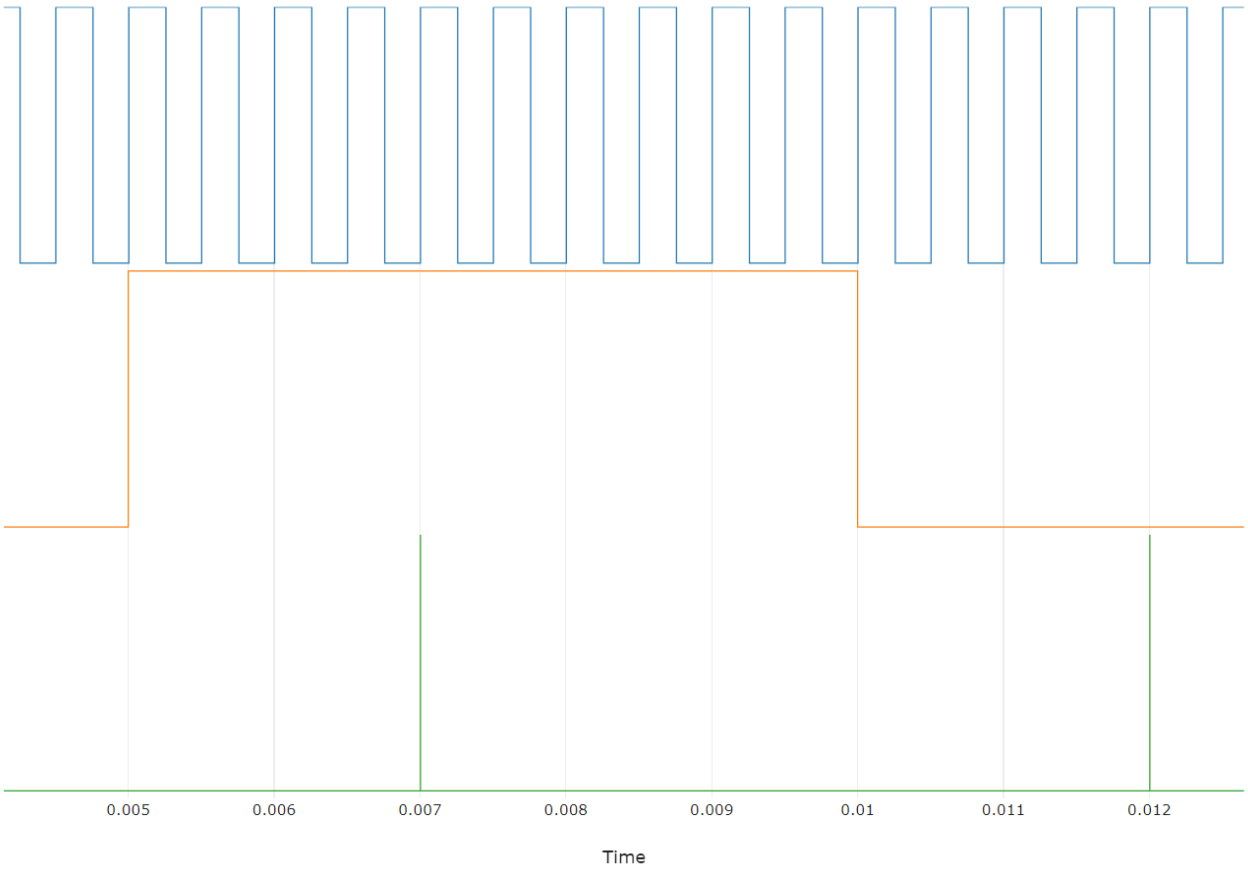

Figure 4. Delayed Edge Detect Simulation (Control Data = 3)

Other delay modules can have an *Output Edge Select* option instead of a delayed edge detect. This option enables a second output on the delay module which functions the same as the output on the EDET module described prior.

Frequency Detect

TPLD frequency detect (FDET) module shown in Figure 5 acts as a frequency comparator, outputting low or high depending on if the input signal provided on *IN* has a lower or higher frequency than the reference signal provided on the *CLK* pin. The FDET module functions by counting the edges of the incoming signal against the rising edges of the reference clock signal. The module outputs low if the internal count of the reference clock signal reaches zero before the count of the input signal, and high otherwise. The FDET module can be configured to count rising, falling, or both edges of the input signal.

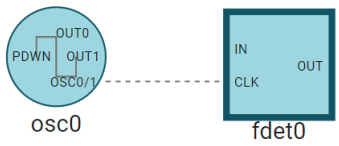

Figure 5. Frequency Detect Module

Figure 6 shows a circuit that muxes between 500Hz and 3kHz input signals and feeds them to a FDET module which is given a 2kHz reference. Figure 7 shows the simulation of this circuit in ICS, with the constant frequency clock signal shown in blue, the input with varying frequency shown in orange, and the module output shown in green. By setting the *Clock Source* option to an external clock, the FDET module can be given an external reference frequency to be compared against as opposed to one generated by the internal oscillator.

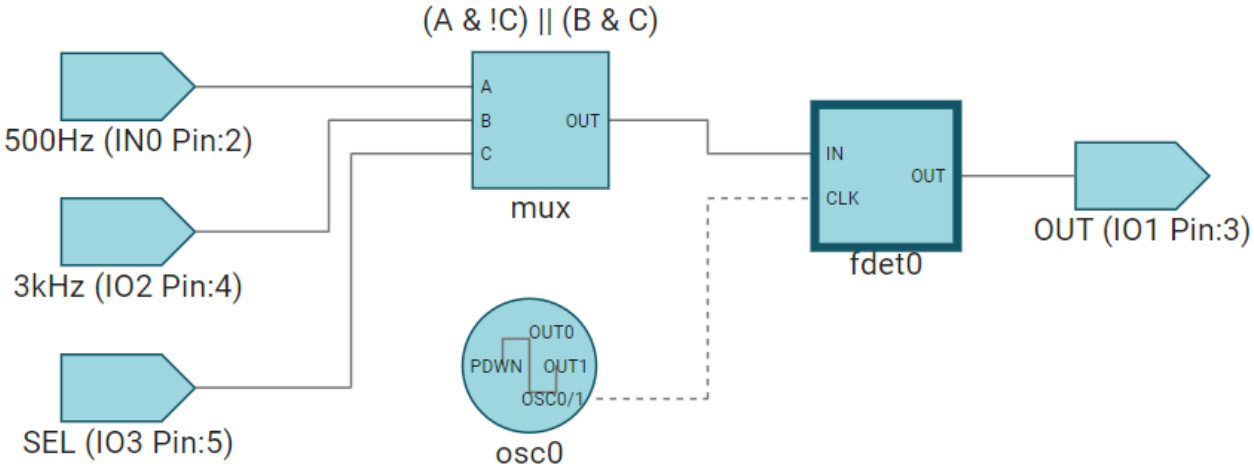

Figure 6. Frequency Detect Mux Circuit

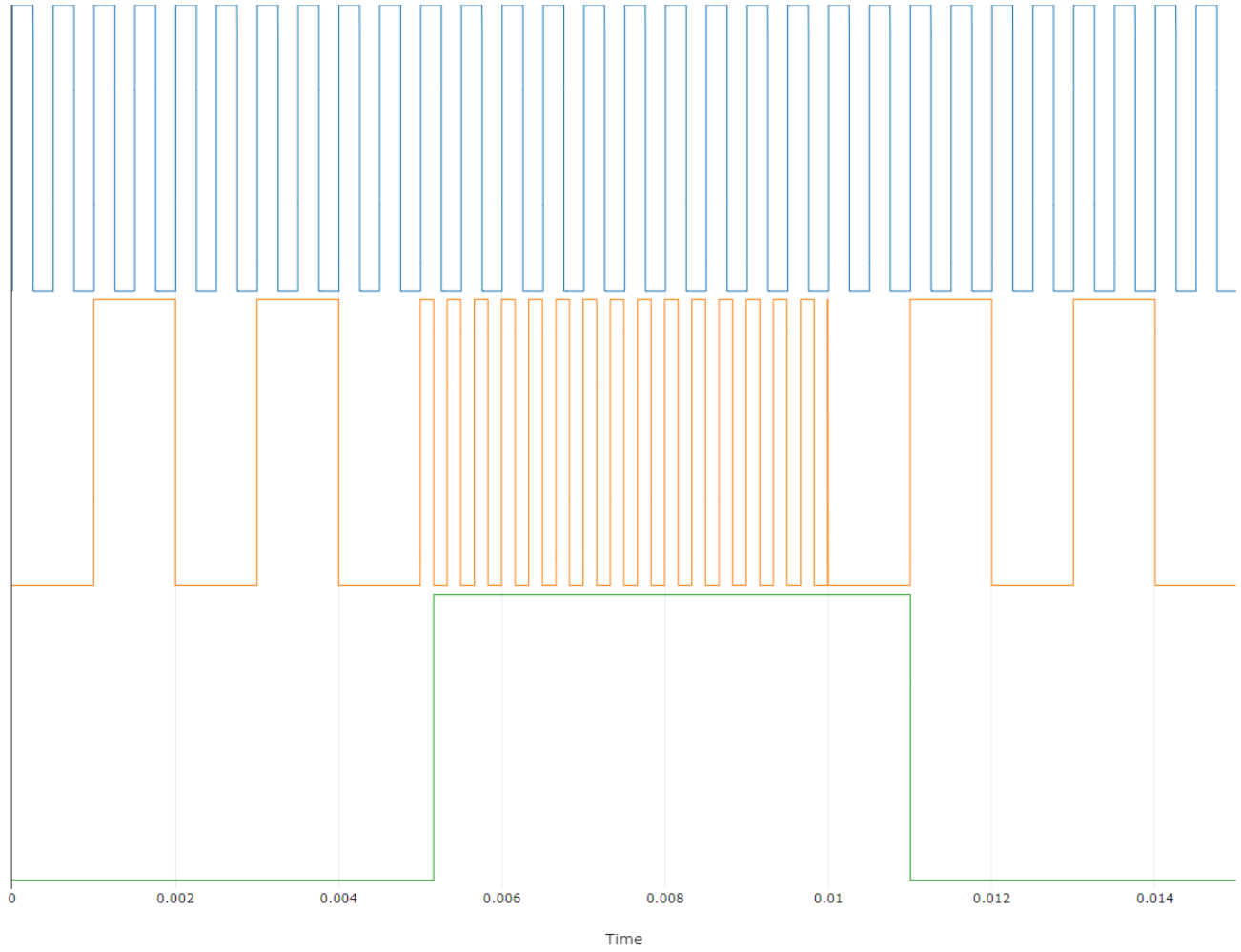

Figure 7. Frequency Detect Mux Circuit Simulation

Conclusion

TPLD integrated modules allow the devices to provide numerous methods of rising and falling edge detection, as well as frequency comparison of two signals. This allows TPLD to act effectively in detecting power good signals, generating resets, PWM and duty cycle adjustments, or any other application that utilizes basic edge detection or frequency comparison.

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