# Application Brief **PWM Generators in TI Programmable Logic Devices**



Malcolm Lyn

# **Application Description**

Pulse-width modulation (PWM) is a method of providing a square or rectangular wave signal with a varying duty cycle commonly used in applications such as power conversion or controlling LED brightness. Some TI Programmable Logic Devices (TPLD) offer integrated pulse-width modulation generators that allow a designer to easily generate and control a square wave with variable duty cycle. This document provides an overview of the PWM generators included in the TPLD1202, namely what the available settings are and how to configure them in InterConnect Studio (ICS).

#### **PWM Generator Components**

When instantiated in ICS, the PWM generator (*pwm0*) appears alongside a counter module (*cnt0*) in Finite-State Machine (FSM) mode, as well as an internal oscillator (*osc0*), as shown in Figure 1.



Figure 1. PWM Generator in ICS

The internal oscillator is automatically set to act as the clock to both the counter and PWM generator. The internal oscillator has settings that allow for a change in output frequency. You can also divide the frequency by changing the clock source setting on either the counter or PWM generator; the clock source setting also allows for use of an external clock source if desired. Note that to avoid output distortions, the counter and PWM generator uses the same clock source and operates at the same frequency. Configuration of the oscillator module is described in more detail in *Utilizing Timing Components in TPLD*.

# **Counter FSM Functionality**

By default, the counter FSM works by counting down one value from the *Control Data* value for every clock pulse received until the internal count value is zero, at which point FSM provides an output pulse for one clock cycle, then resets. Figure 2 shows an example ICS counter simulation where the *Control Data* was set to 3 as seen in the counter settings shown in Figure 3; note that the counter (yellow) pulses high every three clock cycles (blue).



COUNTER 💿		<u>م</u> [] أ
Name	cnt0	
Label		
Clock Source	External Clock	•
Control Data	3	
RST Sync Bypass	2-DFF sync	•
Initial Value	Bypass initial	•
Output Polarity	Non-inverted	*
Reset Mode	High Level Reset	*
Enable FSM Mode	✓	
UP Sync Bypass	2-DFF sync	•
KEEP Sync Bypass	Bypass 2-DFF	•
Device MacroCell Allocated	Any(CNT_FSM_0)	~

Figure 2. Counter Module Settings





The *DATA* connection shown in Figure 1 is the counter providing current internal count value to the PWM generator. This value determines the duty cycle of the PWM generator outputs. The duty cycle of the PWM signal can be calculated by: Duty cycle (%) = (*DATA* / 256) × 100, with a minimum duty cycle of 0% (0/256) and



a maximum of 99.61% (255/256). Each change in count value provides an additive 0.39% increase or decrease in duty cycle.

The counter input signals *UP*, and *KEEP* as seen in Figure 1 exist when the *Enable FSM Mode* setting, visible in Figure 2, is selected for a given counter (counters providing *DATA* to a PWM are locked in FSM mode). These signals can be used to control the internal count value/*DATA* provided by the counter and thus dynamically change the duty cycle of the PWM generator. A logic high on *UP* causes the counter to count up to 255 before emitting a pulse, instead of down to 0. A logic high on *KEEP* maintains the current internal count value, regardless of any incoming clock pulses. A logic high on the *RST* input resets the current internal count value to the initial value set by the *Control Data* setting.

Figure 4 shows an ICS simulation of a counter with the various FSM signals employed. From top to bottom, blue is the clock, yellow is the counter output, green is the *KEEP* input, red is the *RST* input, and purple is the *UP* input.





# **PWM Generator Configuration**

In addition to the *CLK* and *DATA* connections, the PWM generator has a *PUP* (power-up) input that must be a logic high for the generator to provide an output signal, and two outputs *OUT*+ and *OUT*- that are in-phase with each other by default, as seen in Figure 1. The PWM configuration options are shown in Figure 5.



PULSE WIDTH MODULATOR 🔊		9 E E
Name	pwm0	
Label		
Clock Select	OSC0/1	•
Output - Inversion		
Output + Inversion		
Deadband Time	No Deadband	-
Source Select	CNTFSM0	Ψ.
Device MacroCell Allocated	Any(PWM_0)	•

#### Figure 5. PWM Configuration Options

Both *OUT*+ and *OUT*- can be inverted by checking the appropriate *Output Inversion* box. A deadband of 0, 1, 2, or 5 clocks can be selected for *OUT*-; this setting reduces potential for shoot-through current when the PWM is used on circuits such as an H-bridge. A simulation waveform of the PWM generator with *DATA* of 128 (50% duty cycle), inverted *OUT*- output, and 5-clock deadband is shown in Figure 6. *OUT*- is blue and *OUT*+ is yellow. One full output period takes 255 clock cycles and is determined by the PWMs input clock source.



Figure 6. PWM Simulation

# **Example Circuit**

4

The circuit in Figure 7 is configured to dynamically vary the PWM generator's duty cycle in an example overvoltage and undervoltage detection and control application. The PWM is set to run at 50% duty cycle



by default (*cnt0* is given a control data of 128), with *KEEP* set to be a logic high. The multi-channel analog comparator (*mcacmp0*) is used to detect voltages below 800mV and above 1.216V. When a voltage above 1.216V is detected, *KEEP* is set low and the counter is allowed to count down to decrease the duty cycle until the voltage falls below the 1.216 V threshold. When a voltage below 800mV is detected, the *KEEP* is set to low and *UP* is set high so that the counter increases the duty cycle. Simulation of this circuit is shown in Figure 8. The PWM output is shown in blue, and the input voltage is shown in yellow.









As previously described in Counter FSM Functionality, the counter module counts down to 0 or up to 255 and then resets the count value. Thus, additional circuitry is required to pause *cnt0* near the values of 0 or 255 to maintain the minimum and maximum duty cycle and prevent the counter from looping. This circuitry is shown in Figure 9; *cntOV* is configured with a control data of 125 (three lower than *cnt0*) and *cntUV* is configured



with a control data of 131 (three higher than *cnt0*). Upon entering a overvoltage state, both *cnt0* and *cntOV* are reset and begin counting down; *cntOV* counts to 0 before *cnt0* due to having a lower control data, and the corresponding output pulse is latched by *dff0* and used to set *KEEP* high and hold the current count value of *cnt0*. For an undervoltage state, *cntUV* operates the same way, counting up instead of down.



Circuitry to stop cnt0 from looping

#### Figure 9. PWM Looping Prevention Circuit

To maintain that *cntOV* and *cntUV* finish counting before *cnt0*, *cnt0* must also be reset upon a transition to an overvoltage or undervoltage state. This means the duty cycle resets to 50% upon a transition to either state. The logic for controlling the reset and FSM signals into *cnt0* is shown in Figure 10.



#### Figure 10. PWM Counter FSM Control Circuit

#### Additional Considerations

Figure 8 shows that the PWM output reaches the maximum and minimum duty cycle values rather quickly. More gradual changes in duty cycle can be achieved by setting the counter clocks slower than the PWM clock, although this can result in occasional glitching in the PWM output due to clock jitter and skew.

The PWM duty cycle can also be controlled using the I2C or SPI Receiver and writing the desired control data to the appropriate counter FSM's data register.

#### Conclusions

The PWM module allows for TPLD to generate square waves with varying duty cycles. By incorporating several different logic functions and analog sensors, TPLD provides an integrated design for real-time PWM generation and control.

Learn more about TI's portfolio of programmable logic devices

# Trademarks

All trademarks are the property of their respective owners.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated