Application Note

Using Lookup-Tables in Programmable Logic

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ABSTRACT

This application note provides a description of what lookup tables (LUT) are. This document also describes how to use lookup tables in InterConnect Studio, the software created to support TI's TPLD family of devices.

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1 What is a Lookup Table

A lookup table (LUT) is a programmable way to perform digital logic functionality. One way to think about a LUT is as a fill in the blank truth table. For example Table 1-1 is a blank 3 input LUT. This looks very similar to every 3 input truth table, but the outputs are defined by the user instead of a predefined function.

Table 1-1. 3 Input Lookup Table

C	B	A	OUT
0	0	0	REG 0
0	0	1	REG 1
0	1	0	REG 2
0	1	1	REG 3
1	0	0	REG 4
1	0	1	REG 5
1	1	0	REG 6
1	1	1	REG 7

In discrete logic, if the desired function is Equation 1, a simple discrete logic design is to use a 3 input AND gate with a NOT gate on the A input. With a LUT, completing this functionality is simply to set REG 6 to 1 (logic high) and the rest to 0 (logic low) as shown in Table 1-2

$$Q = \overline{A} \cdot B \cdot C \tag{1}$$

Table 1-2. A B C Truth Table

C	B	A	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Implementing LUTs allows for more flexibility in the design, and using programmable logic, such as the TPLD1201, allows designers to make quick changes to logic functionality without any changes to the board or material list.

2 Thinking About a Lookup Table as a MUX

For many familiar with discrete logic, the logic becomes easier to think of the LUT as if there was a multiplex (MUX).

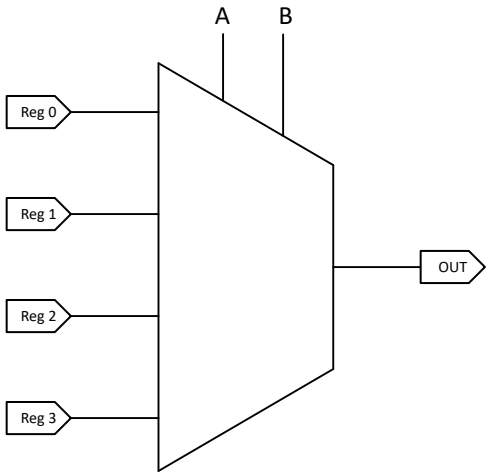

Figure 2-1. MUX Representation of a LUT

Table 2-1. MUX Truth Table

B	A	OUT
0	0	Reg 0
0	1	Reg 1
1	0	Reg 2
1	1	Reg 3

As shown in Figure 2-1 the inputs are more like select pins than actual inputs into logic gates. When A and B are both low Reg 0 is present at the output. When A is high and B is low Reg 1 is present at the output. When A is low and B is high Reg 2 is present at the output. When A and B are both high Reg 3 is present at the output . This means the user is not altering paths within the programmable logic when setting the LUT, but instead changing the value being pushed through by the MUX at any one time

3 How to Configure a Lookup Table

InterConnect Studio (ICS) is the software used to configure a TPLD. Once ICS is launched and a device is selected. Figure 3-1 shows the default configuration of a LUT when the LUT is added to a design. The name field can be set to any value using alpha numeric characters. This value then is always present just below the block in the design space. The label field is a multiline version of the name field. The value entered there is always present in the design space above the block. More information on these fields can be found in *ICS User Guide* . To change the amount of inputs available select the inputs drop down and select the desired number. A higher input hardware LUT can be allocated to a lower input count LUT in InterConnect Studio. For example when using a 2 input LUT in the design a 3 input LUT can be allocated. In this instance the extra input is tied to ground internally and the equation/table calculator automatically accounts for that input being 0 constantly.

Figure 3-1. Default LUT config

The ways to configure the LUT are

- Using a predefined logic function. Those options are
  - AND
  - OR
  - XOR
  - NAND
  - NOR
  - XNOR
  - INVA
- Using a table as shown in Figure 3-3
- Writing an equation as shown in Figure 3-4. For more information on allowed characters please see *ICS User Guide* .

These options can be selected from the Boolean function field as shown in Figure 3-2

Figure 3-2. LUT Selectable Options

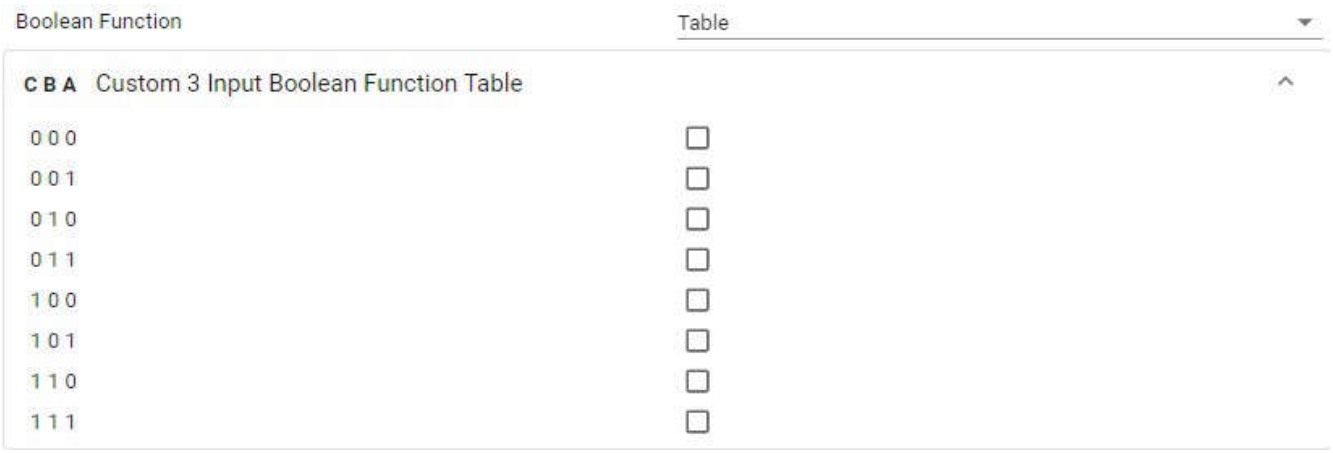

Figure 3-3. LUT Table Option

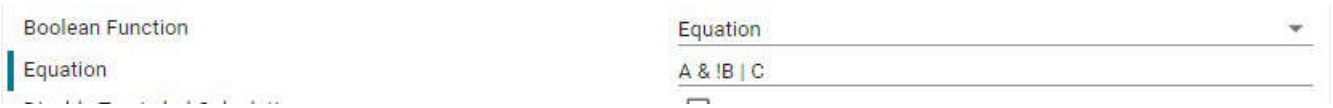

Figure 3-4. LUT Equation Option

4 Using Lookup Tables to Reduce Schematic

Figure 4-1 is an example of a bus arbitration logic. The purpose of this logic is to determine which controller has priority on the bus at any given time. If both RX are low the buses are being held high. Each color box represents a different physical device. Table 4-1 shows the total area of this design upon discrete implementation without even accounting for tolerances between devices or traces needed to interconnect the devices.

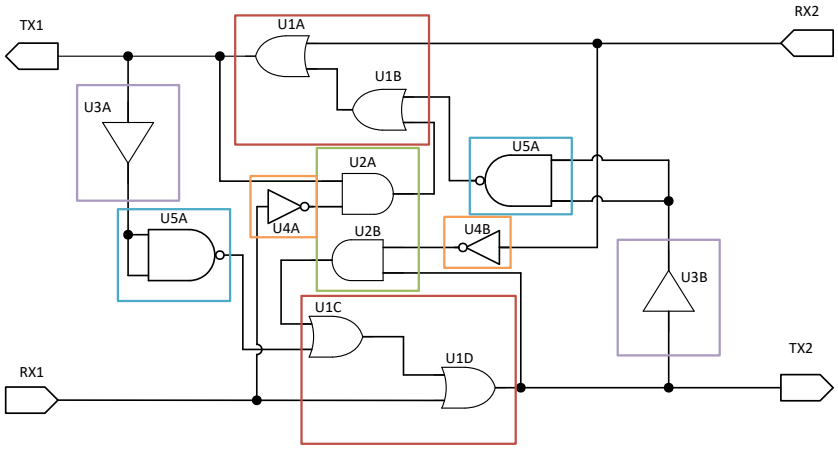

Figure 4-1. Bus Arbitration Schematic

Table 4-1. Area of a Discrete Design

Quantity	Device	Function	Color	Area (mm^2)
1	SN74LV32APWR	Quad OR gate	Red	22.0
1	SN74LVC2G08DCUR	Double AND gate	Green	4.60
1	SN74LVC2G07DBVR	Double buffer	Purple	4.64
1	SN74LVC2G04DBVR	Double inverter	Orange	4.64
1	SN74LVC2G132DCTR	Double NAND gate	Blue	8.26
5	Total			44.14

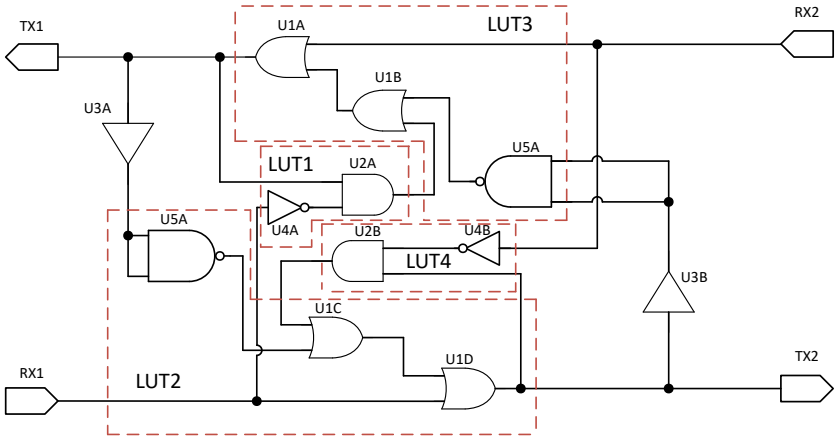

Figure 4-2. Schematic Separated Into Groups

By looking at the inputs to certain groupings of logic gates we can separate this design into 4 groups. Each one of these groups can be simplified down into a single LUT as shown in Figure 4-2.

Now that the schematic has been separated as such we can bring this design into ICS we can create a configuration with 4 pins and 4 LUTs to complete this schematic as shown in Figure 4-3.The configuration of lut1 is 2 input with the table shown in Table 4-2. The configuration of lut2 and lut3 are 3 input with the table shown in Table 4-4. the configuration of lut4 is 2 input with the table shown in Table 4-3.

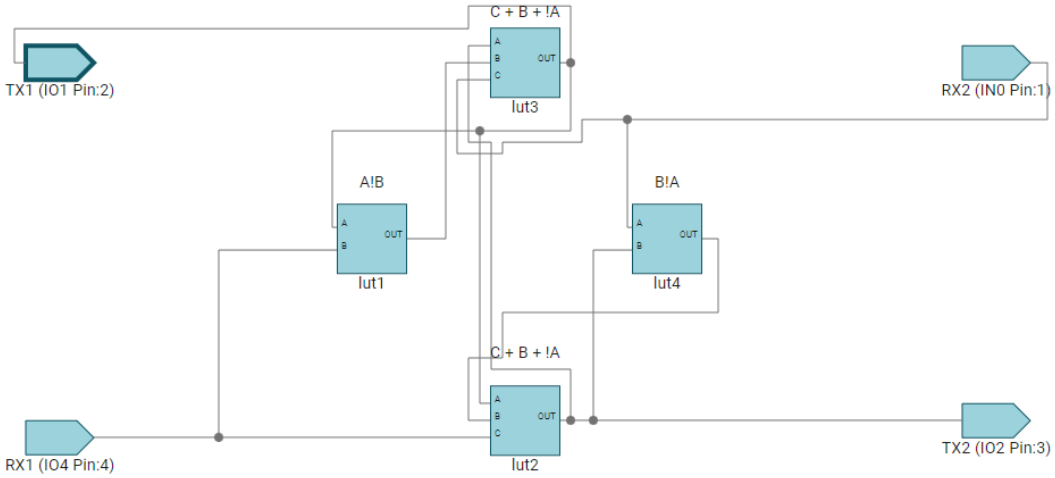

Figure 4-3. Schematic Translated to ICS

Table 4-2. lut1 Config Table

B	A	OUT
0	0	0
0	1	1
1	0	0
1	1	0

Table 4-3. lut4 Config Table

B	A	OUT
0	0	0
0	1	0
1	0	1
1	1	0

Table 4-4. lut2 and lut3 Config Table

C	B	A	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

5 Summary

The Lookup Table is a great, flexible way to incorporate logic needed for a system. Utilizing the LUTs available in the TPLD family means changes to logic can be quick without requiring board changes. Using InterConnect Studio makes configuring a LUT easy, and can condense discrete logic designs into one device.

More information for the TPLD family of devices can be found at *Programmable Array Logic Circuits for Military Applications,* and refer to Table 5-1 for some available devices and evaluation modules to prototype.

Table 5-1. Order Table

Device	EVM
All TPLD	TPLD-PROGRAM
TPLD1201RWBR	TPLD1201-RWB-EVM

6 References

- Texas Instruments, *ICS User Guide.*

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