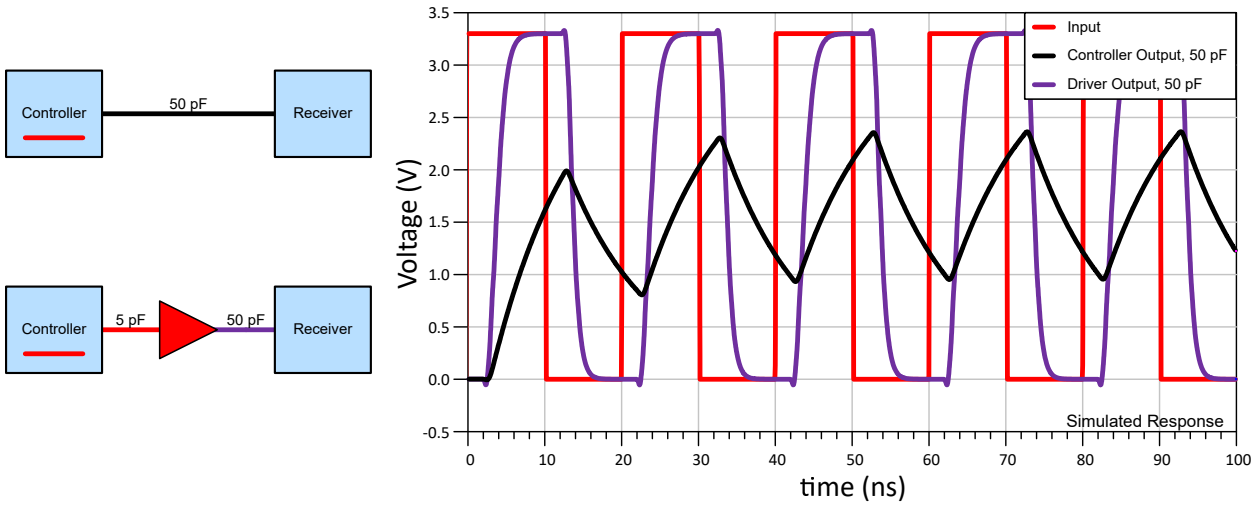
Product Overview

Redrive Digital Signals

System controllers can have weak output drive strength and thus cannot be used to directly transmit over relatively high capacitance signal lines. A logic buffer can be added to reduce loading and improve signal integrity. This can be done at intervals on a bus or trace to improve signal integrity and data rates in particularly large systems.



Left: block diagrams for signal redriving. Right: simulated input (red) and output signals with weak controller (black) and typical buffer driver from the LVC logic family (purple).

Figure 1-1. Signal Redriving Block Diagrams; Simulated Waveforms

Design Considerations

- Reducing load capacitance will decrease output transition time, allowing for faster operation
- Each buffer adds some delay; see the Switching Characteristics table in the device's data sheet
- For traces longer than 12 cm (4760 mil) see *Drive Transmission Lines With Logic*
- *[FAQ] How does a slow or floating input affect a CMOS device?*
- *[FAQ] Where do I find maximum power dissipation for a device?*
- Ask a question on our *Engineer-to-Engineer forum*

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Channels	Features
SN74LVC1G34		1.65 V – 5.5 V	1	High Drive Strength – 32 mA Over-voltage tolerant inputs
SN74HCS125		2 V – 6 V	4	Schmitt-trigger inputs Input and output clamp diodes Three-state outputs
SN74HCS125-Q1	✓			
SN74AUC245		0.8 V – 2.7 V	8	Flow-through pinout Selectable direction Ultra high speed (t_{pd} < 5ns)

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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