Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics

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ABSTRACT

Both buffered and unbuffered CMOS B-series gates, inverters, and high-current IC products are available from TI. Each product classification has application advantages in appropriate logic-system designs. Many CMOS suppliers have concentrated on promoting buffered B-series products, with applications literature focusing on the attributes and use of the buffered types. This practice has left an imbalance in the understanding and application of both buffered and unbuffered gates. In some instances, customers are not using unbuffered products when they are the best choice for the intended application. This application report offers clarification of the relative merits of the buffered and unbuffered CMOS devices.

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Background

Historically, most CMOS gates, inverters, and high-current IC products were unbuffered and exhibited good logic-system performance, speed, noise immunity, and quasi-linear characteristics in a wide variety of applications. As the scope of CMOS products broadened and additional manufacturers began making them, buffered gate and inverter products became available. While initial buffered products were confined to OR and AND functions, buffered NOR and NAND gates were introduced with the same generic 4000A-series designations as the original, widely used, unbuffered gates. Users were surprised by the noninterchangeability of the devices in applications where speed, noise immunity, output impedance, and linear gain-bandwidth characteristics were critical. It is of benefit to CMOS users to have available the definitions and designations of both buffered and unbuffered B-series CMOS devices as determined by the JEDEC CMOS Standardizing Committee under the cognizance of the JC40.2 JEDEC Committee of EIA. The official JEDEC definitions are repeated in the following paragraphs, along with detailed explanations and examples. Comparisons of user-oriented characteristics and the use of buffered and unbuffered gates are also reviewed.

Definitions

Buffered CMOS

A buffered CMOS device is one for which the output ON impedance is independent of any and all valid input logic conditions, both preceding and present, and is said to have a buffered output or to be a buffered CMOS device. All such products are designated by the suffix B.

Unbuffered CMOS

Devices that meet B-series specifications, except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD}, respectively, are marked with the UB designation, including (but not limited to) 4001UB, 4007UB, 4009UB, 4011UB, 4041UB, 4049UB, and 4069UB.

The official JEDEC definitions are applicable primarily to gates, inverters, and high-current (inverting) drivers, such as the specific UB types listed previously. Noninverting gates and drivers, as well as all medium-scale integrated circuit (MSI) and large-scale integrated circuit (LSI B) types are, by definition, B types. There are special analog I/O types that also are B types because they conform to all B standards, except that they have special analog I/O circuitry. Examples of parts that have no buffered or unbuffered significance are 4016B, 4046B, 4051B, 4052B, 4053B, 4067B, 4097B, 4066B, 4511B, and 4528B.

Logic examples of the buffered and unbuffered two-input NOR gates are shown in Figure 1. Note that the buffered logic can be implemented by either a two-input NOR function, followed by two inverters or by two input inverters, followed by the two-input NAND gate and an output buffer. TI uses the latter logic configuration, which has the advantage of optimizing device noise immunity by negating the effect of stacked devices at the input. This characteristic is especially significant for three- or four-input gates where three or four PMOS or NMOS transistors are stacked in series at the input. In this case, the inputs have an effective offset in threshold and reduced input noise immunity.

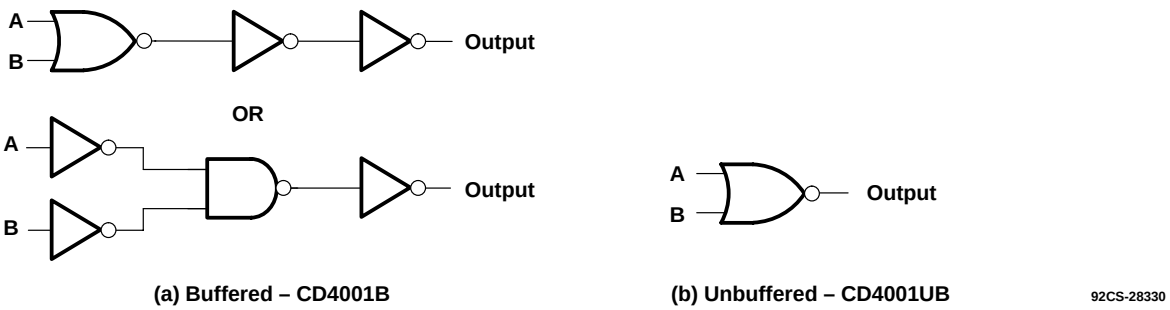


Figure 1. Buffered (CD4001B) and Unbuffered (CD4001UB) Two-Input NOR Gates

Figure 2 is a schematic representation of the TI buffered and unbuffered two-input NOR gates. The improved four-diode-input gate-oxide protection circuit is shown at the inputs.

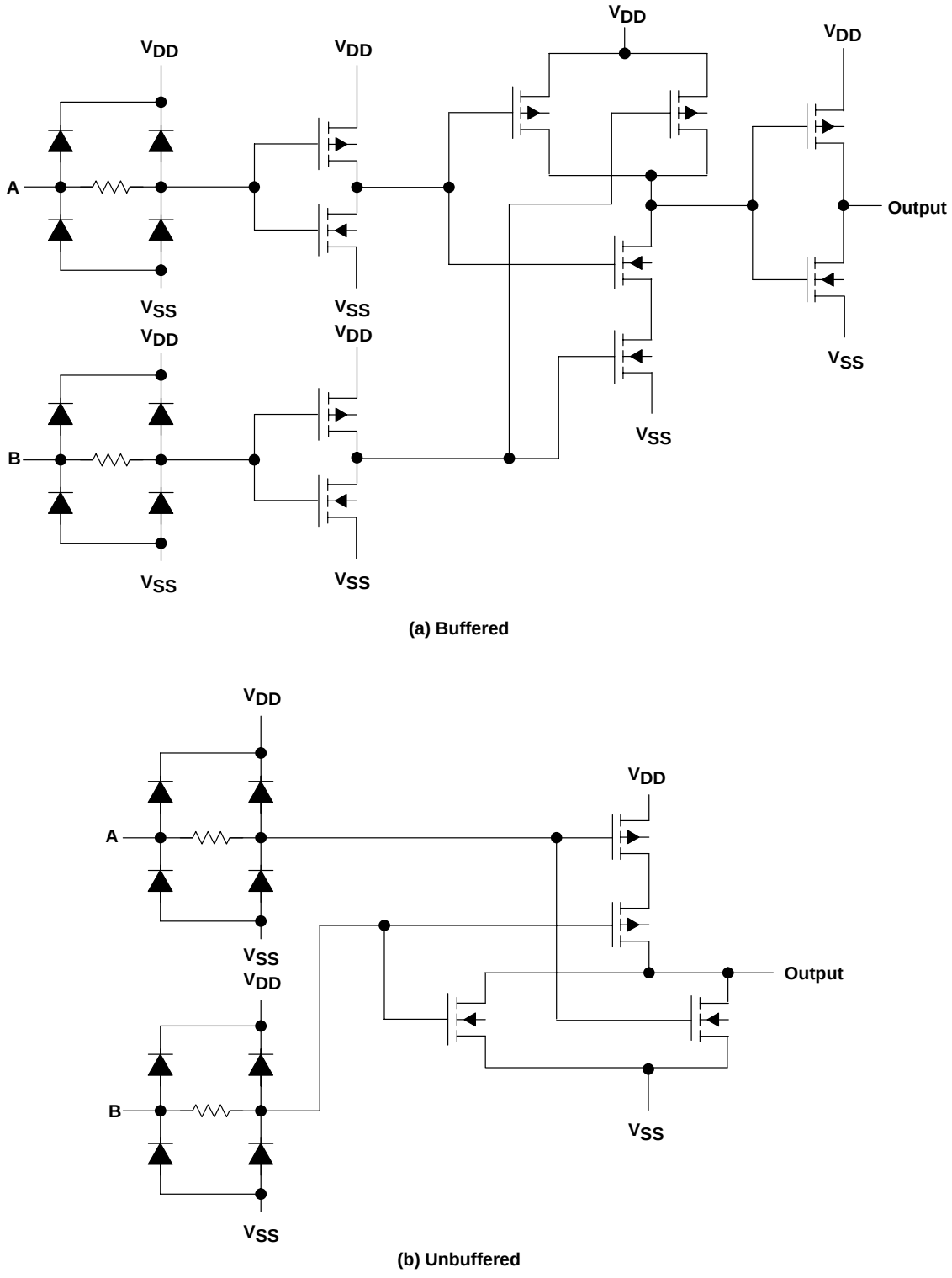


Figure 2. Schematic Diagrams of Buffered and Unbuffered Two-Input NOR Gates

Examples

Examination of the dc performance characteristics of both the buffered and unbuffered two-input NOR gates reveals the two electrical characteristics, output impedance and noise immunity, by which the types are differentiated by the JEDEC standard specifications.

Output Impedance

Buffered Output

Figure 3 shows the buffered output stage and shows the MOS transistor as switched on, with a channel resistance, R, which is the same value for the n switch closed or for the p switch closed.

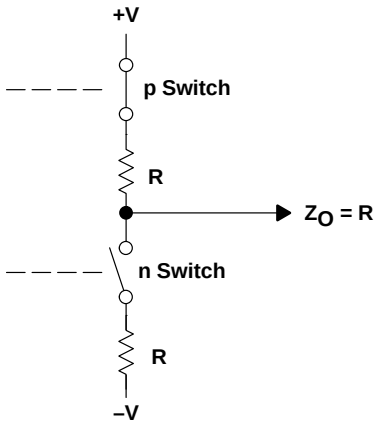


Figure 3. Constant Output Impedance of Buffered Gate

Unbuffered Output

Figure 4 shows the unbuffered two-input gate p- and n-channel MOS switches and appropriate on-channel resistances. Note that the two stacked p-channel switches are designed for an on resistance of R/2, so that the output impedance is R when both the logic inputs are low [see Figure 4(b)]. In Figure 4(a), the output impedance is R to the negative supply terminal (usually ground) for an input logic state of 1, or input high. Figure 4(c) shows the condition when the unbuffered gate has an output impedance of R/2 for both logic inputs high, hence, the variable output impedance of the unbuffered gate. For a four-input gate, this variable is R to R/4. The maximum output resistance of TI buffered or unbuffered gates is R. Thus, minimum I_{OL} and I_{OH} specifications for buffered and unbuffered gates are identical.

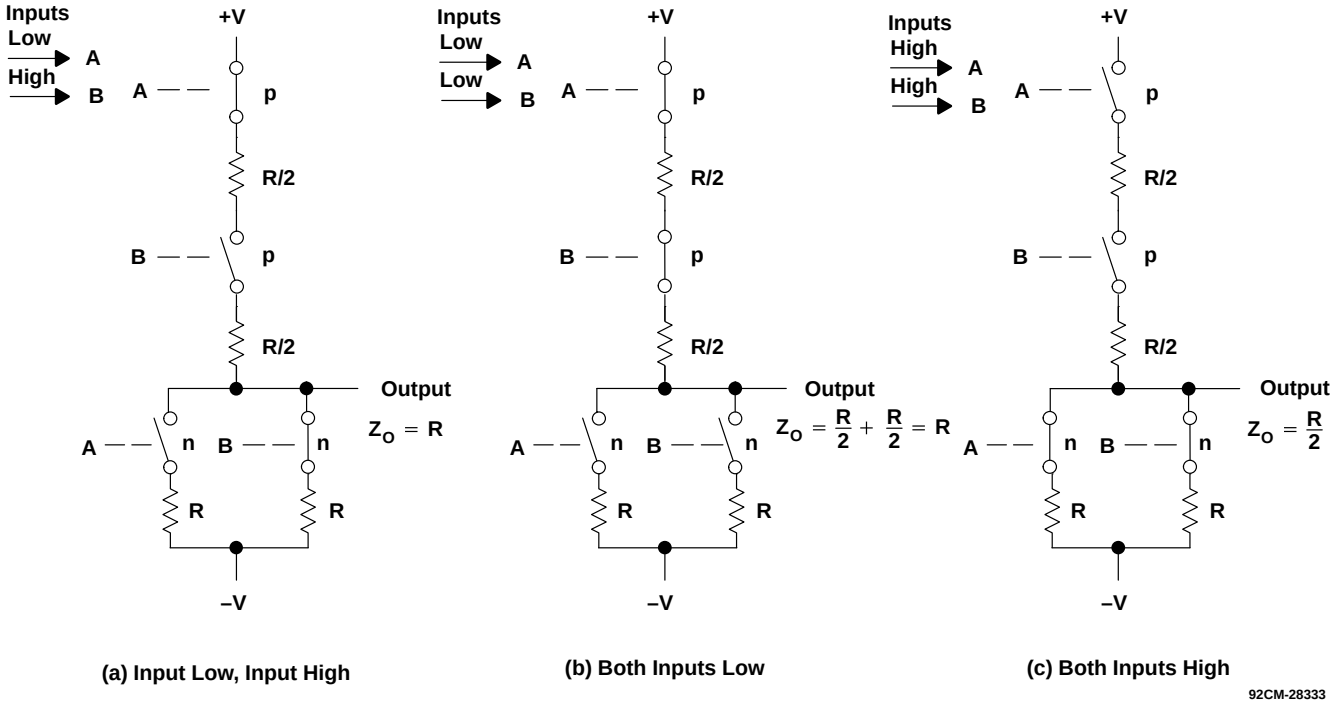


Figure 4. Variable Output Impedance of Unbuffered Two-Input NOR Gate (The Resistors Represent the ON Impedance of a p- or n-Channel MOS Transistor)

Noise Immunity

The second JEDEC-defined difference between the buffered and unbuffered CMOS gates (or inverters) is the difference in input noise-immunity characteristics.

Buffered NOR Gate

The buffered two-input NOR gate voltage-transfer characteristics are square shaped because of the gain of three CMOS stages from input to output (see Figure 5). Figure 5 shows that noise voltage inputs of ±1.5 V at V_{DD} = 5 V and ±4 V at V_{DD} = 15 V will have little discernible effect on the output voltage; i.e., noise immunity for all logic states is optimally high as is noise margin, 1 V at V_{DD} = 5 V and 2.5 V at V_{DD} = 15 V.

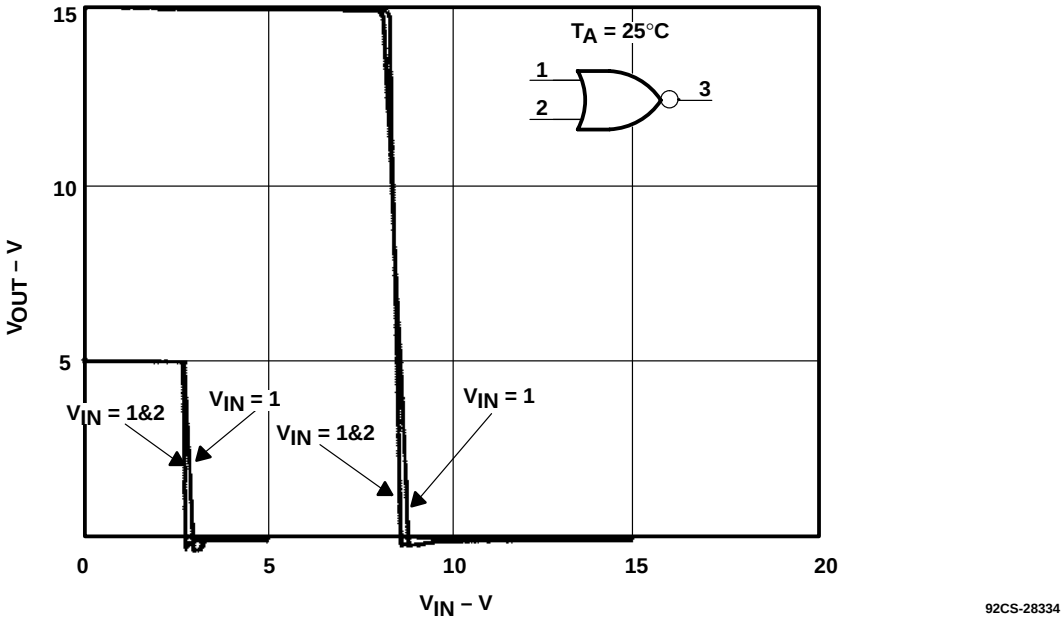
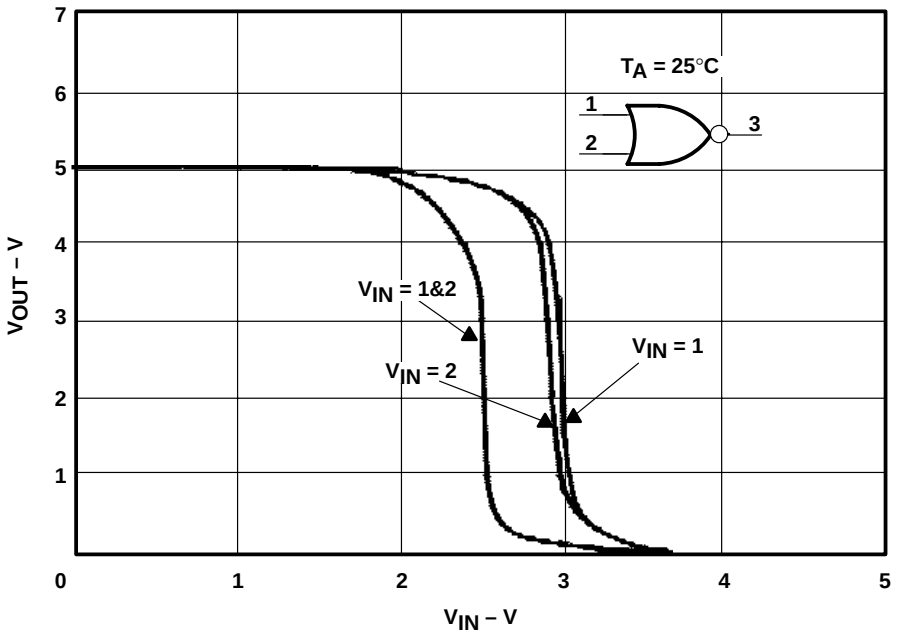


Figure 5. Voltage Transfer Characteristics of Buffered Two-Input NOR Gate (CD4001B)

Unbuffered NOR Gate

Figure 6 shows the rounded voltage transfer characteristics of the two-input unbuffered NOR gate. Also evident is the shift in the transfer curve for the different logic input states. Compare these curves to those of Figure 5, and the effects of the nonbuffered inputs, as well as the gain differences, are evident. The rounded characteristics require a noise-immunity specification of 20% of V_{DD} at 5 V, 10 V, and 15 V, as well as a reduced noise margin, 0.5 V at V_{DD} = 5 V and 1 V at V_{DD} = 15 V.



(a) V_{OUT} = 5 V

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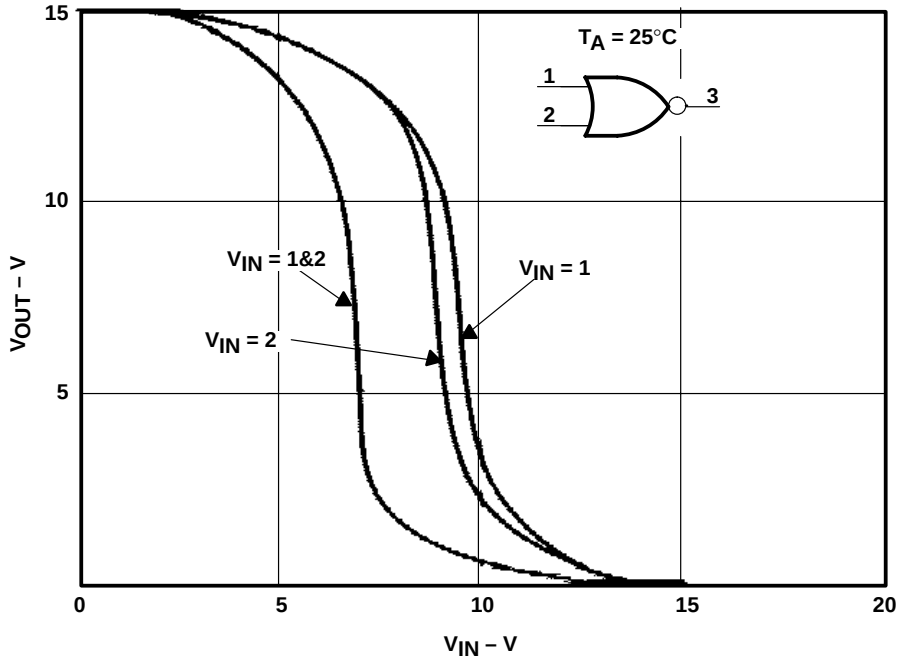

(b) V_{OUT} = 15 V

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Figure 6. Voltage Transfer Characteristics of an Unbuffered Two-Input NOR Gate (CD4001UB) With Output Voltages of 5 V and 15 V

The previous definitions use gate characteristics to illustrate the JEDEC definitions for buffered and unbuffered characteristics relative to variable output impedance and noise-immunity performance. Inverters and high-current drivers also can be defined as buffered (B) types or unbuffered (UB) types by virtue of the squared or rounded transfer characteristics of Figures 5 and 6, respectively. Even though both types have a single NMOS and single PMOS output transistor, the rounded transfer characteristic of the unbuffered inverters makes them UB types by virtue of:

- Reduced noise-immunity performance, where the 20% rating is applicable
- Varying output impedance, as a function of input voltage change along the rounded portion of the transfer curve

Comparisons

Table1 shows the qualitative comparisons of user-oriented performance characteristics of buffered and unbuffered CMOS gates, inverters, or drivers.

Table 1. Comparison of Buffered and Unbuffered Gate Characteristics

CHARACTERISTICS	BUFFERED GATE	UNBUFFERED GATE
Propagation delay	Slow	Fast
Noise immunity/margin	Excellent	Good
Output impedance and output transition time	Constant	Variable
AC gain	High	Low
Output oscillation for slow inputs	Yes	No
Input capacitance	Low	High

Table 2 is a quantitative comparison of the key performance characteristics, with explanations for propagation delay, noise immunity, output impedance, and output transition time.

Table 2. Characteristics of Buffered and Unbuffered Gates

CHARACTERISTICS			BUFFERED GATES	UNBUFFERED GATES
Typical propagation delay		V_{DD} = 5 V, C_L = 50 pF	150 ns	60 ns
		V_{DD} = 10 V	65 ns	30 ns
		V_{DD} = 15 V	50 ns	25 ns
Noise immunity/margin			30% of V_{DD} at 5 V and 10 V; 27% at 15 V	20% of V_{DD} at 5 V, 10 V, and 15 V
Noise margin		V_{DD} = 5 V	1 V	0.5 V
		V_{DD} = 10 V	2 V	1.0 V
		V_{DD} = 15 V	2.5 V	1.0 V
Typical output impedance	V_{DD} = 5 V, V_O = ±0.4 V	Two-input gate	400 Ω	200 Ω to 400 Ω
		Three-input gate	400 Ω	133 Ω to 400 Ω
		Four-input gate	400 Ω	100 Ω to 400 Ω
Typical output transition time	V_{DD} = 5 V, C_L = 50 pF	Two-, three-, and four-input gates	100 ns	50 ns to 100 ns
AC gain		V_{DD} = 10 V	≈68 dB	≈23 dB
AC bandwidth		V_{DD} = 10 V	280 kHz	885 kHz
Output oscillation for slow inputs			Susceptible for t_r, t_f > 1 ms	Not susceptible for t_r, t_f to 100 ms
Typical input capacitance		Average	1 pF to 2 pF	2 pF to 3 pF
		Peak	2 pF to 4 pF	5 pF to 10 pF

Propagation Delay

Propagation delay times in Table 2 are applicable to TI two-, three-, and four-input NOR and NAND gates.

Noise Immunity

Table 3 shows the detailed data-sheet input-voltage specifications for buffered and unbuffered gates. From the test conditions in Table 3, the user-oriented noise immunity and noise-margin data of Table 2 are derived. Also, refer to Figures 5 and 6 for the voltage-transfer characteristics that illustrate the reason for the different input-voltage-specification requirements for buffered and unbuffered devices.

Table 3. Input-Voltage Specifications

CHARACTERISTICS		V_O	V_{DD}	LIMITS MIN	LIMITS MAX	UNIT
V_{IL} Input voltage	Buffered	4.5	5		1.5	V
		9	10		3	
		13.5	15		4	
	Unbuffered	4.5	5		1	
		9	10		2	
		13.5	15		2.5	
V_{IH} Input voltage	Buffered	0.5	5	3.5		V
		1	10	7		
		1.5	15	11		
	Unbuffered	0.5	5	4		
		1	10	8		
		1.5	15	12.5		

NOTES: 1. Noise-immunity voltage is the V_{IL} or V_{IH} specification limit.
2. Noise-margin voltage is computed as:
Noise-margin voltage $= V_{IL} – (V_{DD} – V_O)$
$= (V_{DD} – V_{IH}) – V_O$

Output Impedance

For output impedance, refer to Figures 3 and 4 and accompanying descriptions of the constant output impedance of buffered gates and the variable output impedance of unbuffered gates. Note that both buffered and unbuffered TI two-, three-, and four-input gates are designed to meet the same maximum output impedance; output current ratings (I_{OL} and I_{OH}) have the same minimum limit on TI data sheets.

Output Transition Time

The time required for a CMOS output to transfer high or transfer low is constant for buffered gates, but varies according to input logic states for unbuffered gates. Output transition time varies as a function of the driving source resistance of the output, which is state dependent, as indicated in Figure 4, as well as the device output capacitance, which is dependent on both device size and input logic state. Because of variable output capacitance, output transition-time variations are not a linear function of output resistance. As Table 2 shows, TI two-, three-, and four-input unbuffered gates exhibit a net two-to-one difference in output transition time, even though the output resistance has a net four-to-one variation for the four-input gate.

AC Gain and Bandwidth

CMOS linear-mode gain was measured for both the buffered and unbuffered TI two-input NOR gates using the test circuit of Figure 7. Figure 8 shows typical linear-mode gain difference between buffered and unbuffered TI two-input NOR gates. While absolute performance depends on device type (inverters or two-, three-, and four-input gates) and test configurations, Figure 8 defines the approximately three-to-one difference in linear-mode performance between buffered and unbuffered gates.

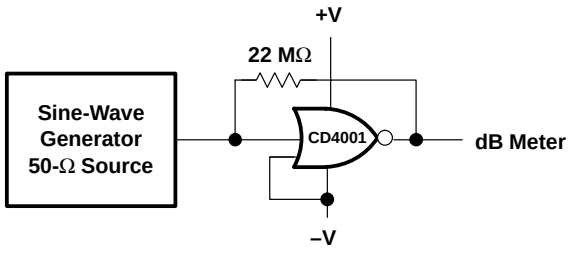

Figure 7. Linear-Gain Test Circuit

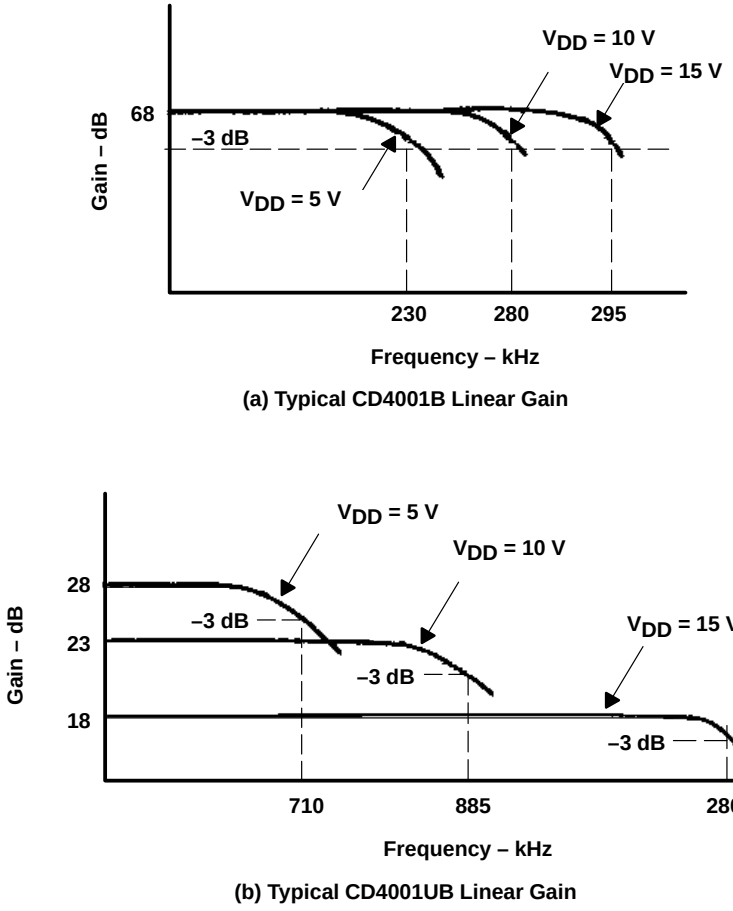

Figure 8. Typical Linear-Mode Gain of Buffered and Unbuffered Two-Input NOR Gates

Output Oscillation for Slow Inputs

The high linear-mode gain of buffered CMOS devices can lead to undesirable oscillation at outputs when input ramps are in excess of approximately 1-ms duration. Figure 9 shows this effect when approximately 1 mV to 2 mV of ac noise within the device bandwidth on the input signal are amplified through the device and tend to develop a few cycles of oscillation between the positive and negative rails under 5-V operation. In contrast, unbuffered gates do not tend to oscillate unless a noise voltage of 200 mV to 300 mV is present within the bandwidth of the device. An input ramp of up to 100-ms duration did not create oscillation in laboratory tests of TI unbuffered gates.

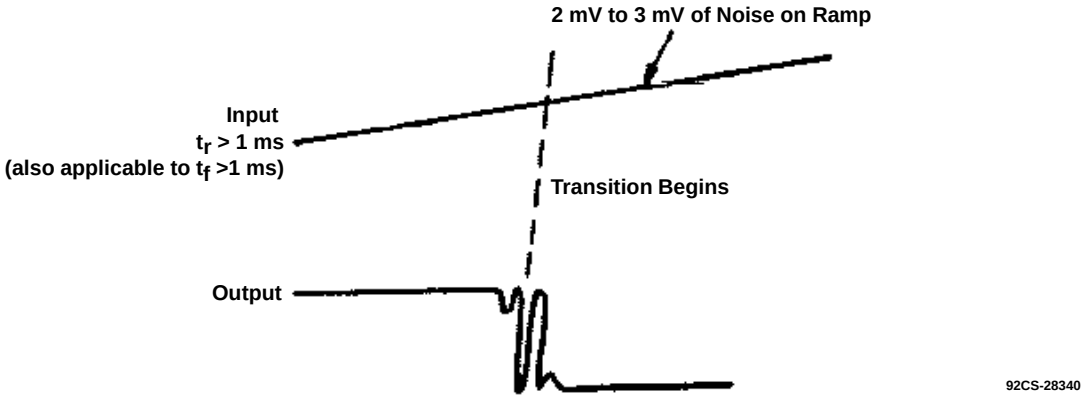

Figure 9. Buffered Output Oscillation for Slow Input

Input Capacitance

Figures 10 and 11 show the dynamic input capacitance of the TI buffered and unbuffered two-input NOR gates, respectively. The large MOS transistor geometry of the unbuffered NOR gate is responsible for the higher peak input capacitance (Miller effect) in the linear switching range. The longer dwell in this linear region also tends to broaden the Miller capacitance and, therefore, increases the effective average input capacitance. Buffered gates and inverters are rated at a maximum input capacitance of 1 unit load (7.5 pF JEDEC standard); unbuffered gates and inverters are rated at 2 unit loads (15 pF maximum). High-current unbuffered drivers, such as the CD4049UB, are rated at 3 unit loads (22.5 pF maximum).

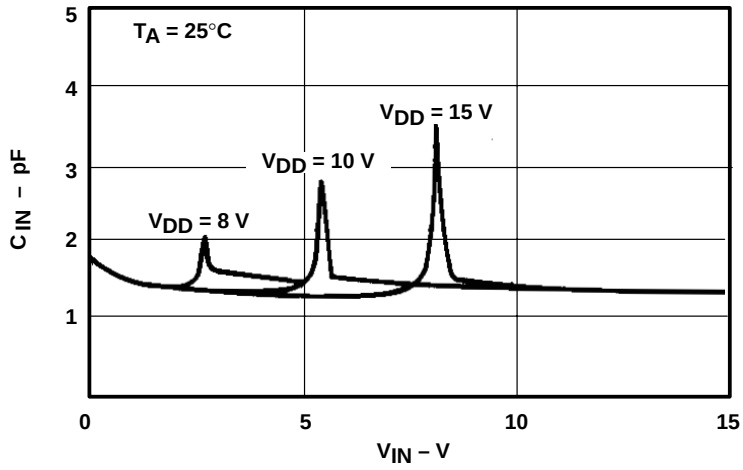

Figure 10. Input Capacitance of Buffered Two-Input NOR Gate (CD4001B)

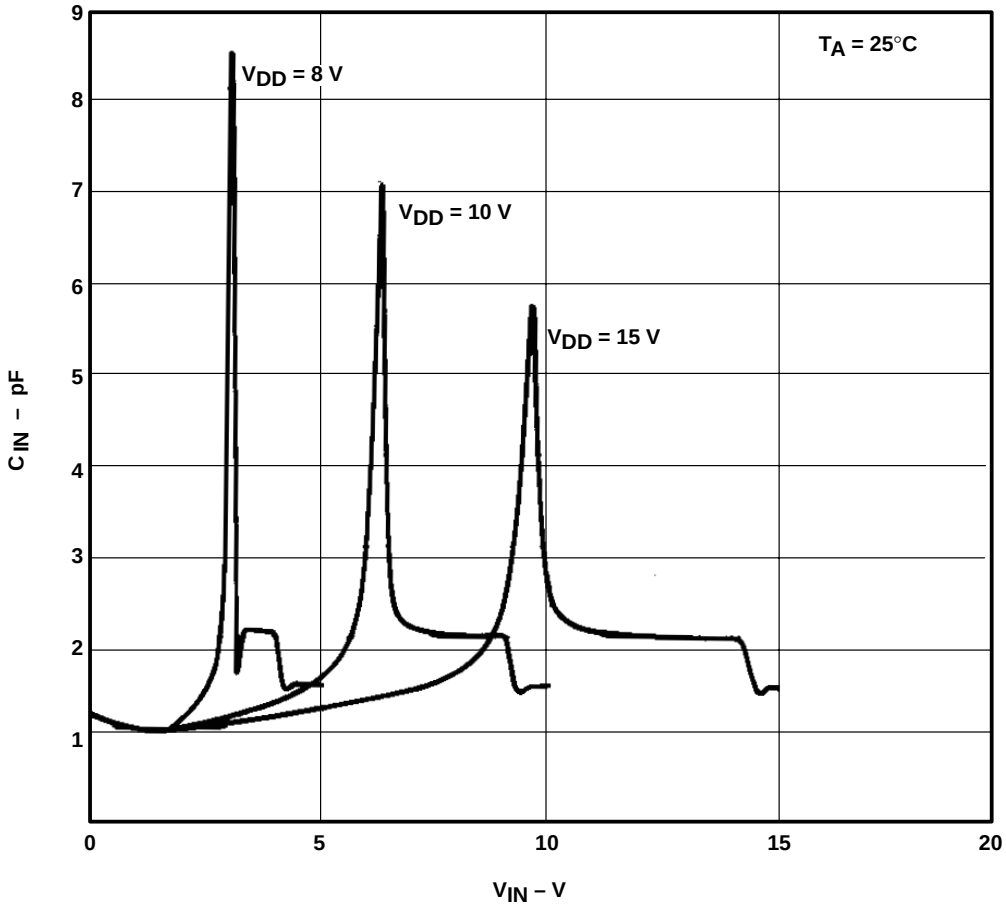

Figure 11. Input Capacitance of Unbuffered Two-Input NOR Gate (CD4001UB)

Applications Guidance

Table 4 summarizes preferred application areas for both buffered and unbuffered TI B-series devices. This information is based on the buffered and unbuffered CMOS device characteristics listed in Table 2, combined with the author's experience and familiarity with the application areas indicated. The information given is general guidance to allow the designer to key-in on the specific performance characteristics of either device type. The data provided in this application report are derived from TI standardized B and UB products whose circuit designs were implemented to match performance between UB and B gate types as closely as possible. For example, device sizes were selected to assure matched output drive. In addition, the process and layout rules followed in B and UB designs of TI devices are identical, as is the use of improved gate-oxide protection circuitry for B and UB devices.

Table 4. Applications of Buffered and Unbuffered CMOS Gates and Inverters

APPLICATION		BUFFERED	UNBUFFERED
High-speed systems			Preferred
High-noise environments, low-speed systems		Preferred	
Ultra-low-frequency systems, inputs <1-kHz sine wave or ramps with t_r, t_f > 1 ms, excluding Schmitt triggers†			Preferred
Gate applications requiring constant output impedance, such as D/A R-2R conversion		Preferred	
Linear amplification	High frequency, moderate gain		Preferred
	Low frequency, high gain	Preferred	

† Applies to gates of inverter designs of astable or monostable multivibrators with t > 1 ms

TI Gate, Inverter, and Driver Products

Table 5 is a list of small-scale integrated (SSI) B and UB products presently in production by TI. Refer to TI data sheets for detailed product information.

Table 5. TI COS/MOS Buffered and Unbuffered Gate, Inverter, and Driver Types

BUFFERED	UNBUFFERED
CD4001B	CD4001UB
CD4002B	CD4007UB
CD4010B	CD4009UB
CD4011B	CD4011UB
CD4012B	CD4041UB
CD4023B	CD4049UB
CD4025B	CD4069UB
CD4050B	
CD4068B	
CD4071B	
CD4072B	
CD4073B	
CD4075B	
CD4078B	
CD4081B	
CD4082B	

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