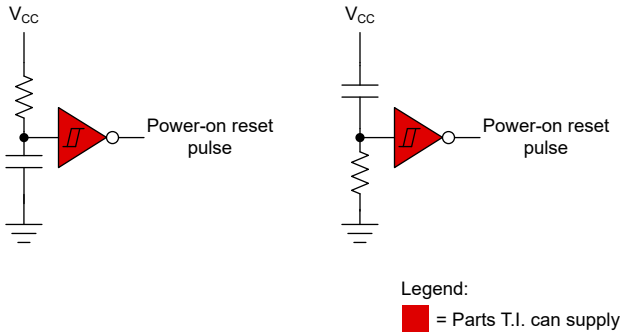
Product Overview

Generate a Power-On Reset Pulse

On device start-up, some logic parts may output an invalid state until cleared. A pulse can be generated when V_{CC} turns on to reset those parts to valid output states.



Design Considerations

- The pulse width is determined by T = RC
  - The standard configuration for a 1-ms pulse is R = 10 kΩ, C = 0.1 µF
- Multiple reset pulse generators with different RCs can be used to delay the pulse to some devices, resetting some before others or triggering clock inputs
- *[FAQ] How does a slow or floating input affect a CMOS device?*
- *[FAQ] Where do I find maximum power dissipation for a device?*
- Ask a question on the TI E2E™ forum

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Channels	Features
SN74LVC1G14		1.65 V – 5.5 V	Inverting buffer	1 channel, Schmitt-trigger inputs
SN74LVC1G14-Q1	✓			
SN74LVC2G14		1.65 V – 5.5 V	Inverting buffer	2 channel, Schmitt-trigger inputs
SN74LVC2G14-Q1	✓			
SN74LVC1G17		1.65 V – 5.5 V	Buffer	1 channel, Schmitt-trigger inputs
SN74LVC1G17-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265