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ALVC Advanced Low-Voltage CMOS Data Book

Including SSTL, HSTL, and ALB







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INTRODUCTION

Since its inception in 1994, the Texas Instruments (TI^{TM}) ALVC (Advanced Low-Voltage CMOS) logic family has been the de facto standard for high-performance low-voltage logic. Designed for operation in the 2.3-V to 3.6-V V_{CC} range, the close to 80 functions of the ALVC family allow the design flexibility and ease needed for today's most demanding high-performance systems. For bus-interface functions, ALVC offers a current drive of 24 mA and static power consumption of 40 μ A. Bus-hold cells on the inputs of ALVC devices eliminate the need for external pullup resistors and prevent inputs from floating.

The ALVC family, which includes innovative functions for memory interleaving, multiplexing, and interlacing to SDRAMS, has gained prominence in the high-speed memory market. The ALVC family offers the industry's most complete line of high-speed memory interface logic devices. A number of ALVC devices feature series damping resistors for improved noise performance. Also, a number of devices without bus hold are ideally suited for PC100 applications.

SSTL (Stub Series-Terminated Logic) is the computer industry's leading choice for next-generation technology in high-speed memory subsystems, adopted by a JEDEC standard and endorsed by major memory module, workstation, and personal computer (PC) manufacturers. Five devices are included in the SSTL section of this data book.

ALB (Advanced Low-Voltage BiCMOS) logic is the fastest BiCMOS logic family available from TI. With clamping diodes to eliminate undershoot and overshoot, these two 3.3-V Widebus™ devices address the high-speed demands of the industry.

HSTL (High-Speed Transceiver Logic) devices accept HSTL-level inputs and produce LVTTL-level output signals. HSTL devices have found a home in select memory-addressing applications.

For more information on these or other TI products, please consult the TI Worldwide Technical Support listing in the back of this data book, or visit the TI logic web page at http://www.ti.com/sc/logic.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i Input capacitance

The internal capacitance at an input of the device

C_{io} Input/output capacitance

Input-to-output internal capacitance; transcapacitance

C_o Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):

 $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

 ΔI_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5 \text{ V}$

I_{l(hold)} Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input

Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} High-level output current

The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

^{*}Current out of a terminal is given as a negative value.



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

I_{OZ}, I_{OZPU/PD}

Off-state (high-impedance-state) output current (of a 3-state output)

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establishes the high-impedance state at the output

t_a Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c Clock cycle time

Clock cycle time is 1/f_{max}.

t_{dis} Disable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} Enable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{\text{OE}}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.
 - 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

^{*}Current out of a terminal is given as a negative value.



t_{PLH} Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{sk(o)} Output skew

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.
 - 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

t_w Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{II} Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

V_{IT+} Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT}_

V_{IT}— Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}



EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level ↓ = transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)Z = off (high-impedance) state of a 3-state output

a . . . h = the level of steady-state inputs A through H, respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 \overline{Q}_0 = complement of Q_0 or level of \overline{Q} before the indicated steady-state input

conditions were established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or \uparrow

= one high-level pulse = one low-level pulse

Toggle = each output changes to the complement of its previous level on each active

transition indicated by \downarrow or \uparrow

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, $\neg \neg \neg \neg \neg$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)



Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE

INPUTS						OUTI	PUTS						
CLEAR	МО	DE	CLOCK	SEF	RIAL	PARALLEL		٥.	0. 0-		. 0-	0-	
CLEAR	S1 S0	CLOCK	LEFT	RIGHT	Α	В	С	D	QA	QB	QС	Q_{D}	
L	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
Н	Х	Χ	L	Х	Х	Х	Χ	Χ	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q _{D0}
Н	Н	Н	↑	Х	Х	а	b	С	d	а	b	С	d
Н	L	Н	↑	Х	Н	Н	Н	Н	Н	Н	Q_{An}	Q_{Bn}	Q _{Cn}
Н	L	Н	↑	Х	L	L	L	L	L	L	Q_{An}	Q_{Bn}	QCn
Н	Н	L	↑	Н	Х	Х	Χ	Χ	Χ	Q _{Bn}	Q_{Cn}	Q_{Dn}	Н
Н	Н	L	↑	L	Х	Х	X	Χ	Χ	Q _{Bn}	Q_{Cn}	Q_{Dn}	L
Н	L	L	Х	Х	Х	Х	Χ	Χ	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output Q_A , data entered at B is at Q_B , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B , the previous levels of Q_B and Q_C are now at Q_C and Q_D , respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

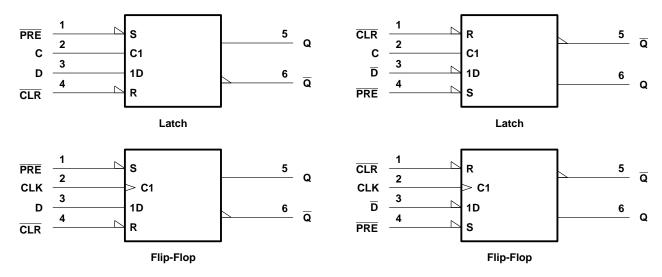
The function table functional tests do not reflect all possible combinations or sequential modes.

D-TYPE FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called preset (PRE). An input that causes a \overline{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (\overline{PRE} and \overline{CLR}) if they are active low.

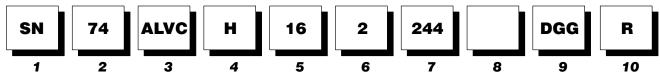
The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \overline{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\searrow) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

Example:



1 Standard Prefix

Example: SNJ - Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 – Military 74 – Commercial

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/
Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic

AHC/AHCT - Advanced High-Speed CMOS Logic

ALB – Advanced Low-Voltage BiCMOS ALS – Advanced Low-Power Schottky Logic

ALVC - Advanced Low-Voltage CMOS Technology

AS - Advanced Schottky Logic

AVC - Advanced Very Low-Voltage CMOS Logic

BCT - BiCMOS Bus-Interface Technology

CBT - Crossbar Technology

CBTLV - Low-Voltage Crossbar Technology

F - F Logic

FB - Backplane Transceiver Logic/Futurebus+

GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transceiver Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage CMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology

S - Schottky Logic

SSTL – Stub Series-Terminated Logic
TVC – Translation Voltage Clamp Logic

4 Special Features

Examples: Blank = No Special Features

D – Level-Shifting Diode (CBTD)

H - Bus Hold (ALVCH)

R - Damping Resistor on Inputs/Outputs (LVCR)

S - Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals

1G - Single Gate

8 – Octal IEEE 1149.1 (JTAG)

16 - Widebus™ (16, 18, and 20 bit)

18 - Widebus IEEE 1149.1 (JTAG)

32 - Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options

2 - Series-Damping Resistor on Outputs

4 – Level Shifter 25 – 25-Ω Line Driver

7 Function

Examples: 244 - Noninverting Buffer/Driver

374 - D-Type Flip-Flop

573 – D-Type Transparent Latch 640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision Letter Designator A–Z

9 Packages

Examples: D, DW - Small-Outline Integrated Circuit (SOIC)

DB, DL - Shrink Small-Outline Package (SSOP)

DBB, DGV - Thin Very Small-Outline Package (TVSOP)

DBQ - Quarter-Size Outline Package (QSOP)

DBV, DCK – Small-Outline Transistor Package (SOT)

DGG, PW - Thin Shrink Small-Outline Package (TSSOP)

FK – Leadless Ceramic Chip Carrier (LCCC)*
FN – Plastic Leaded Chip Carrier (PLCC)

GB - Ceramic Pin Grid Array (CPGA)*

 $\mathsf{GKE},\,\mathsf{GKF}-\mathsf{MicroStar}\;\mathsf{BGA^{\scriptscriptstyle\mathsf{TM}}}\;\mathsf{Low\text{-}Profile}\;\mathsf{Fine\text{-}Pitch}$

Ball Grid Array (LFBGA)

HFP, HS, HT, HV - Ceramic Quad Flatpack (CQFP)*

J, JT – Ceramic Dual-In-Line Package (CDIP)*

N, NP, NT – Plastic Dual-In-Line Package (PDIP)

NS, PS - Small-Outline Package (SOP)

PAG, PAH, PCA, PCB, PM, PN, PZ - Thin Quad Flatpack

(TQFP) or Thin Shrink Small-Outline Package (TSSOP)

PH, PQ, RC – Quad Flatpack (QFP)

W, WA, WD - Ceramic Flatpack (CFP)*

* Military Only

10 Tape and Reel

Devices in the DB and PW package types include the R designation for reeled product. Existing products designated as LE may maintain that designation, but are being converted to R.

Examples:

Existing Nomenclature – SN74LVTxxxDBLE New Nomenclature – SN74LVTxxxADBR

LE – Left Embossed (valid for DB and PW packages only)

R – Standard (valid for all surface-mount packages except some DB and PW devices)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

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NOTIFICATION OF PACKAGE NOMENCLATURE ALIAS (for Standard Linear and Logic device names of greater than 18 characters)

TI is converting from its current order-entry system to a more advanced system. This conversion requires modifications, both internal and external, to TI's current business processes. This new system will ultimately provide significant improvements to all facets of TI's business – from production, to order entry, to logistics. One change required is a limitation of TI part numbers to no more than 18 characters in length. Based on customer inputs, Standard Linear and Logic determined the least disruptive implementations as outlined below:

Package alias

TI will use a package alias to denote specific package types for devices currently exceeding 18 characters in length. Table 1 shows a mapping of package codes to an alias single-character representation.

Table 1

CURRENT PACKAGE CODE	ALIAS	
DL	L	
DGG/DBB	G	
DGV	V	
DLR	LR – tape/reel packing	
DGGR/DBBR	GR – tape/reel packing	
DGVR	VR – tape/reel packing	

Current: SN74 ALVCH 162269A DGGR New: SN74 ALVCH 162269A GR

2. Resistor-option nomenclature

For devices greater than 18 characters with input and output resistors, TI will adopt a simplified nomenclature to designate the resistor option. This will eliminate the redundant "2" (designating output resistors) when the part number also contains an "R" (designating input/output resistors).

Input/Output Resistor
Output Resistor

Current: SN74 ALVCH R 16 2 245 A New: SN74 ALVCH R 16 245 A

There is no change to the device or data-sheet electrical parameters. The packages involved and the changes in nomenclature are noted in Table 1.

These nomenclature changes are being gradually implemented. The first customer-visible conversions for TI logic devices will be made to data sheets. Over the next few months, TI logic data sheets will be updated. These changes in device nomenclature do not reflect a change in device performance or process characteristics.

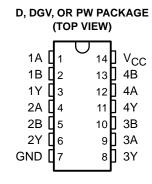
General Information	1
ALVC Gates/Octals	2
ALVC Widebus™/Widebus+™	3
ALVC Widebus™ With Series Damping Resistors	4
ALVC Dual-Supply-Voltage Translators	5
SSTL	6
HSTL	7
ALB	8
Mechanical Data	9
Output Derating Curves	A

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- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Package Options Include Plastic** Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) **Packages**



description

This quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

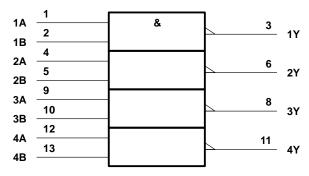
The SN74ALVC00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74ALVC00 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

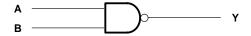
INPUTS		OUTPUT
Α	В	Υ
Н	Н	L
L	X	Н
Х	L	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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SCES115C - JULY 1997 - REVISED AUGUST 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	: D package	127°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{sta}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
VIH		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	C
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	ľ	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
Vo	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA
ІОН	High-level output current	V _{CC} = 2.7 V		-12	
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Low lovel output ourrent	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDI	TIONS	Vcc	MIN	TYP	MAX	UNIT
	I _{OH} = -100 μA		1.65 V to 3.6 V	V _C C-0.	2		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	I _{OH} = -6 mA		2.3 V	2			
Voн			2.3 V	1.7			V
	I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA		3 V	2			
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA		1.65 V			0.45	
VOL	I _{OL} = 6 mA		2.3 V			0.4	V
VOL	I _{OL} = 12 mA		2.3 V			0.7	V
	IOL = 12 IIIA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
lį	$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
Icc	$V_I = V_{CC}$ or GND,	₁ = 0	3.6 V			10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Of	ther inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		4.5		pF

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

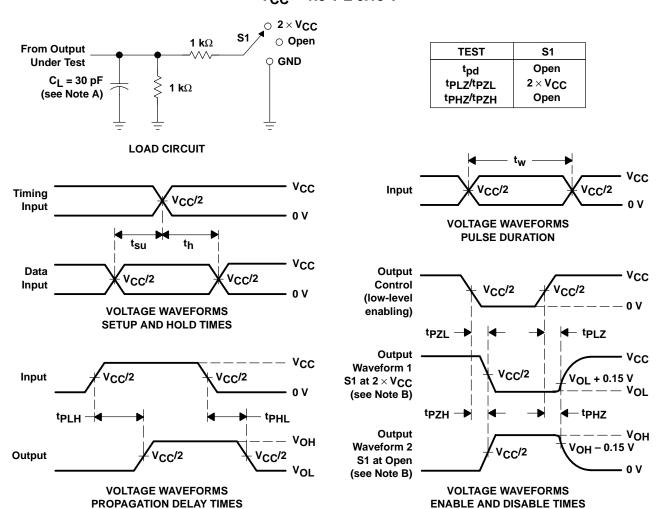
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	A or B	Υ	1	4.4	1	2.8		3.2	1	3	ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST C	TEST CONDITIONS		V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	C _L = 0,	f = 10 MHz	20	21	23	pF

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$

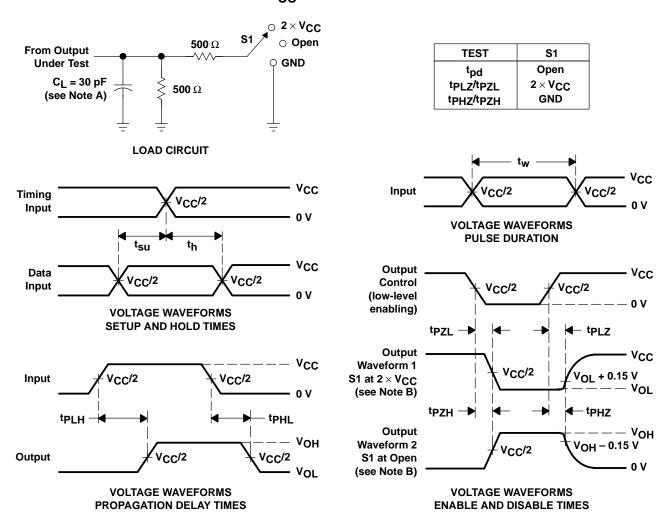


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



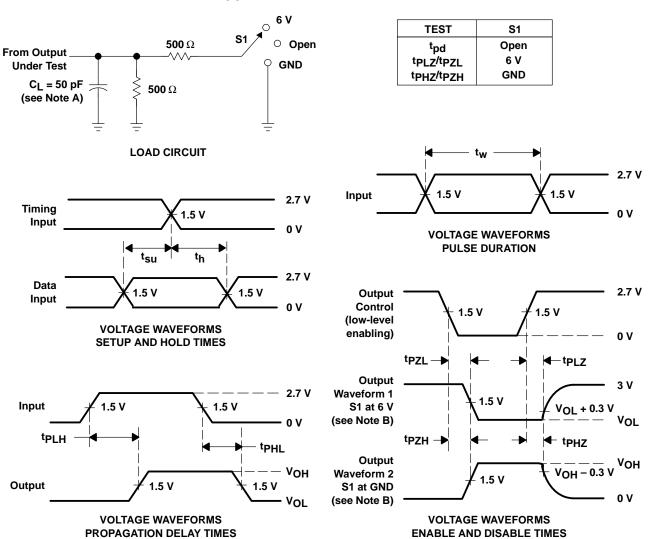
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V

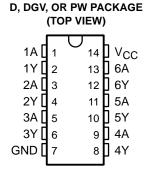


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages



description

This hex inverter contains six independent inverters designed for 1.65-V to 3.6-V V_{CC} operation.

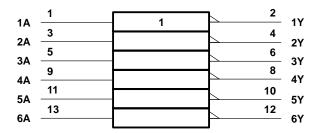
The SN74ALVC04 performs the Boolean function $Y = \overline{A}$.

The SN74ALVC04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, IOK (VO < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	127°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{sto}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _C C	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ _I	Input voltage		0	VCC	V
۷o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High loved output ourrent	V _{CC} = 2.3 V		-12	A
ІОН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Low lovel output ourrent	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	•		5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
	ΙΟΗ = -100 μΑ		1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Voн			2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
			3 V	2.4			
	$I_{OH} = -24 \text{ mA}$		3 V	2			
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VoL	$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL	I _{OL} = 12 mA		2.3 V			0.7	V
	IOL = 12 IIIA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
lį	$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			10	μΑ
∆lcc	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		3.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
	(1001701)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	‡	1	3		3.3	1	2.8	ns

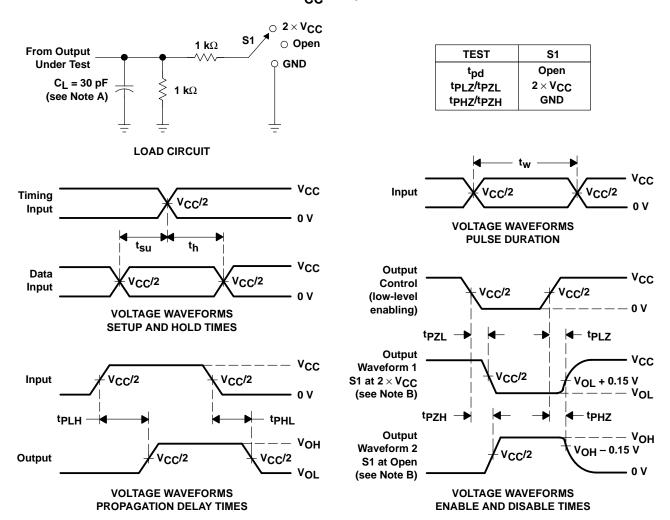
[‡] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAINETER	TEST CONDITIONS	TYP	TYP TYP		ONIT
C _{pd}	Power dissipation capacitance per inverter	$C_L = 0$, $f = 10 \text{ MHz}$	‡	23	27.5	pF

[‡] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

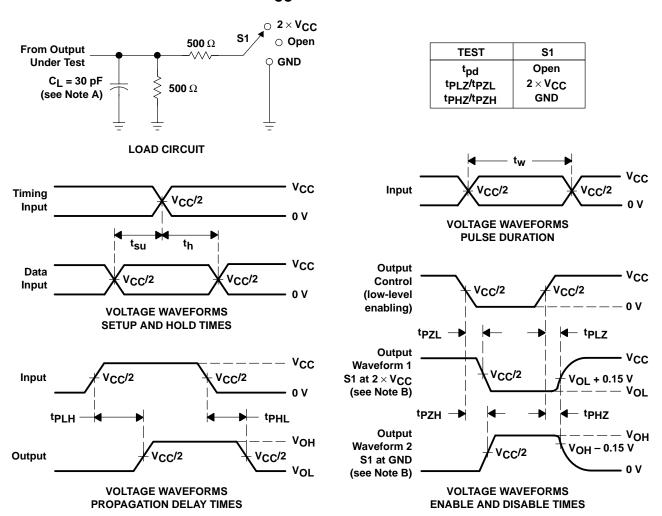


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



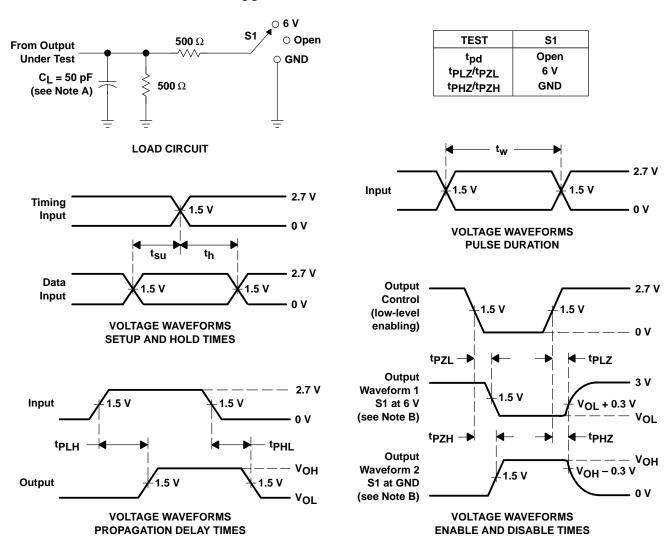
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



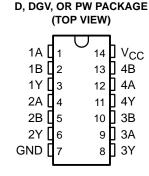
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SCES101D - JULY 1997 - REVISED AUGUST 1998

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-AND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

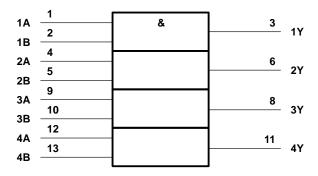
The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

The SN74ALVC08 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	Х	L
Х	L	L

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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TEXAS INSTRUMENTS

SCES101D - JULY 1997 - REVISED AUGUST 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, IOK (VO < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	127°C/W
	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{sto}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ _I	Input voltage	-	0	VCC	V
۷o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	I Pala Java Lauda et avezant	V _{CC} = 2.3 V		-12	mA
ІОН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Law laws and a standard assessed	V _{CC} = 2.3 V		12	^
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	•	0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	NDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
	I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Voн			2.3 V	1.7			V
	I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA		3 V	2			
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
Voi	$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL	I _{OL} = 12 mA		2.3 V			0.7	V
	IOL = 12 IIIA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
lį	$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		4.5		pF

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

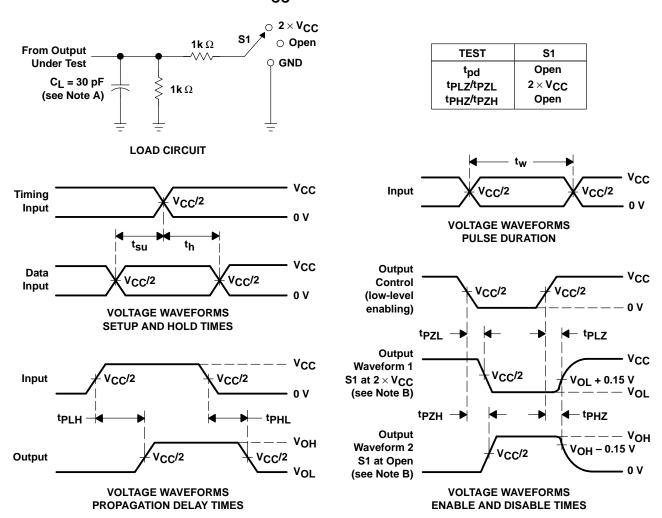
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	A or B	Υ	1.2	5.3	1	3.2		3	1.2	2.9	ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST C	ONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
				TYP	TYP	TYP		
C _{pd}	Power dissipation capacitance per gate	C _L = 0,	f = 10 MHz	24	25	26	pF	

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$

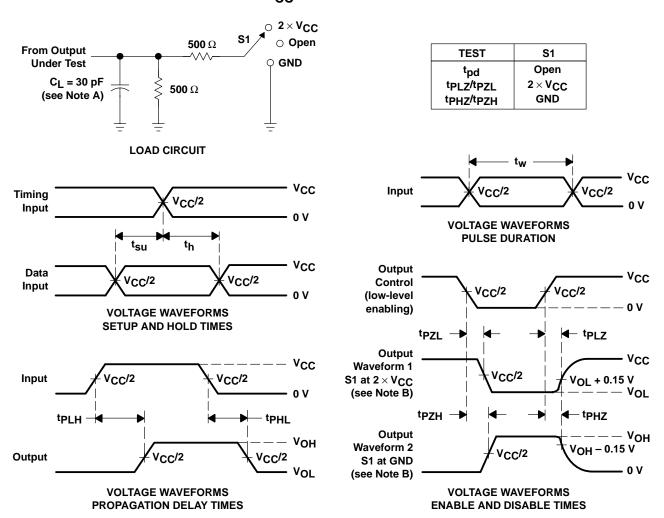


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



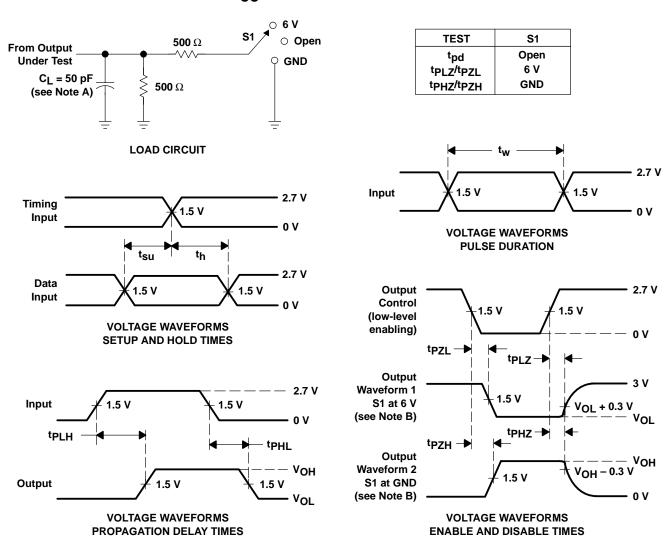
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

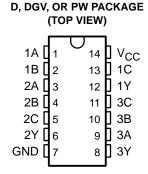
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages



description

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

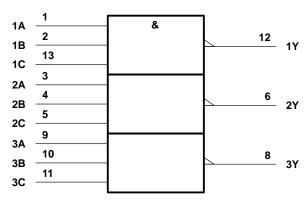
The SN74ALVC10 performs the Boolean function $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN74ALVC10 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

	INPUTS		OUTPUT
Α	В	С	Y
Н	Н	Н	L
L	X	Χ	Н
Х	L	Χ	Н
Х	X	L	Н

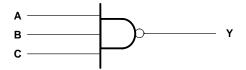
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

cas Instruments essarily include

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

• • • • • • • • • • • • • • • • • • • •		0.51/. 4.01/.
Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2) .		. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3): I	D package	127°C/W
1	DGV package	182°C/W
1	PW package	170°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH High-level input voltage VIL Low-level input voltage VI Input voltage VO Output voltage IOH High-level output current	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	VIH High-level input voltage VIL Low-level input voltage VI Input voltage VO Output voltage IOH High-level output current	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
	High level output ourrent	V _{CC} = 2.3 V		-12	mA
VO Output voltage IOH High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA	
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Low lovel output ourrent	V _{CC} = 2.3 V		12	A
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIO	NS	VCC	MIN	TYP [†]	MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$		1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Voн			2.3 V	1.7			V
	I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA		3 V	2			
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA		1.65 V			0.45	
V _{OL}	I _{OL} = 6 mA		2.3 V			0.4	V
VOL	I _{OL} = 12 mA		2.3 V			0.7	V
	IOL = 12 IIIA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
lį	V _I = V _{CC} or GND		3.6 V			±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$)	3.6 V			10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other	inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		4		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

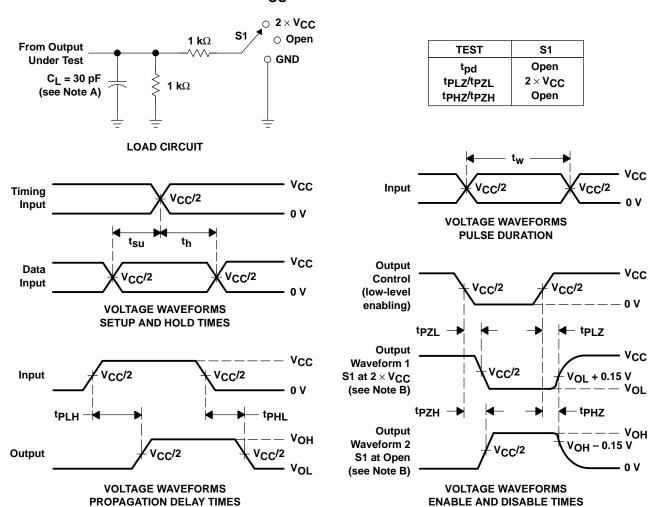
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM TO (INPUT) (OUTPU	_	V _{CC} =		V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	A, B, or C	Y	1.1	4.8	1	3		3.3	1	3	ns

operating characteristics, T_A = 25°C

Г		PARAMETER		TEST CONDITIONS		V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		FARAMETER	TEST CONDITIONS		TYP	TYP	TYP	UNIT
Ε	C _{pd}	Power dissipation capacitance per gate	$C_L = 0$,	f = 10 MHz	23	24	26	pF

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$

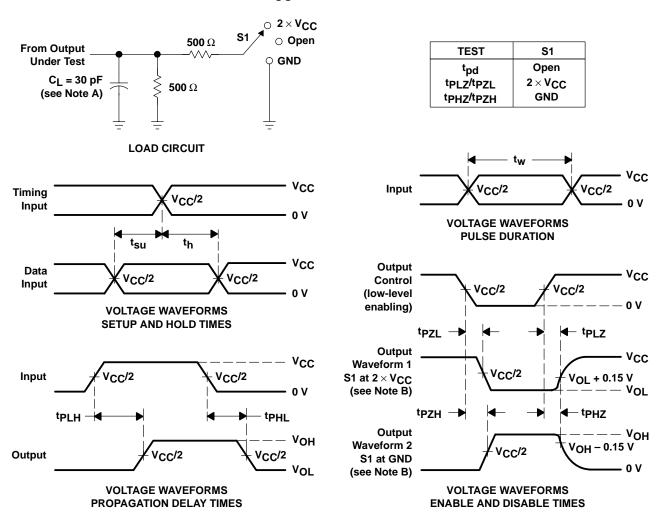


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

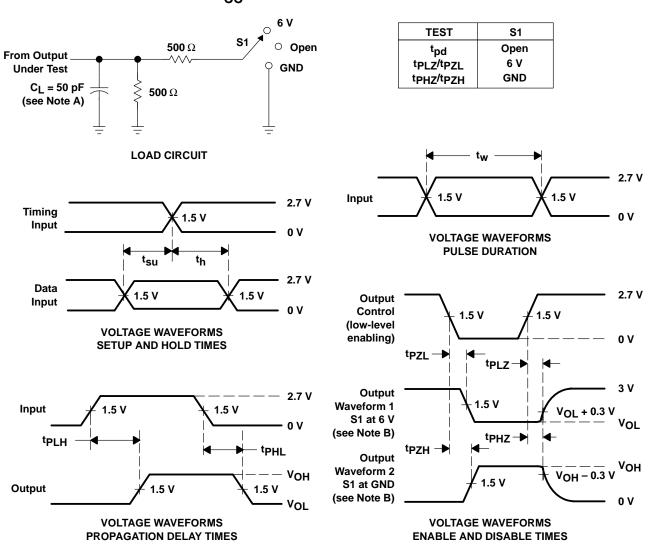


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



D, DGV, OR PW PACKAGE (TOP VIEW)

1A [

1Y [2

2Y 🛮

за Г

GND ∏7

3Y 🛮 6

2A 🛮 3

D ∨_{CC}

13 **[**] 6A

12 🛮 6Y

11 🛮 5A

10 **∏** 5Y

9 🛮 4A

8 🛮 4Y

- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **Package Options Include Plastic** Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) **Packages**

description

This hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

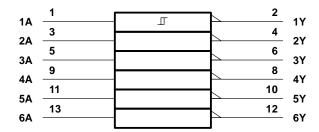
The SN74ALVC14 contains six independent inverters, and performs the Boolean function $Y = \overline{A}$.

The SN74ALVC14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)		–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)		\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	127°C/W
***	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	H High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧١	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	٧
		$V_{CC} = 1.65 \text{ V}$		-4	
la	High lovel output current	$V_{CC} = 2.3 \text{ V}$		-12	mA
·ОН	VIH High-level input voltage VIL Low-level input voltage VI Input voltage VO Output voltage IOH High-level output current	$V_{CC} = 2.7 V$		-12	IIIA
		$V_{CC} = 3 V$		-24	
		$V_{CC} = 1.65 \text{ V}$		4	
lou	Low lovel output current	$V_{CC} = 2.3 V$		12	mA
IOL	Low-level output current	$V_{CC} = 2.7 V$		12	IIIA
		$V_{CC} = 3 V$		24	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYPT MAX	UNIT
		1.65 V			
V _{T+}		2.7 V	0.8	2	
Positive-going threshold		3 V	0.8	2]
		3.6 V	0.8	2	
		1.65 V			
VT_		2.7 V	0.4	1.4	V
Negative-going threshold		3 V	0.6	1.5]
		3.6 V	0.8	1.8	
		1.65 V			
ΔVT		2.7 V	0.3	1.1	V
Hysteresis (V _{T+} – V _T _)		3 V	0.3	1.2	1 '
(-1+ -1-)		3.6 V	0.3	1.2	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2	
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		1
	$I_{OH} = -6 \text{ mA}$	2.3 V	2		
Voн		2.3 V	1.7		V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2		
		3 V	2.4		
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
	I _{OL} = 4 mA	1.65 V		0.45	
Va	I _{OL} = 6 mA	2.3 V		0.4	V
VOL	la. 42 mA	2.3 V		0.7]
	I _{OL} = 12 mA	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	
lį	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V			pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

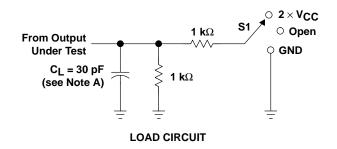
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INPUT) (OUTPUT)	TYP	MIN MAX	MIN MAX	MIN MAX		
^t pd	А	Y					ns

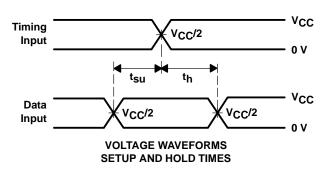
operating characteristics, T_A = 25°C

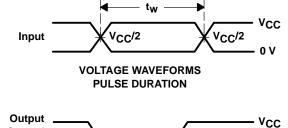
PARAMETER		TEST C	TEST CONDITIONS		V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	PARAMETER	1EST CONDITIONS		TYP	TYP	TYP	UNIT
C _{pd}	Power dissipation capacitance per inverter	$C_L = 0$,	f = 10 MHz				pF

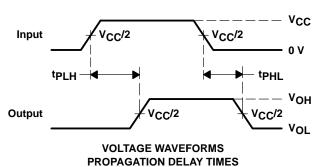
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

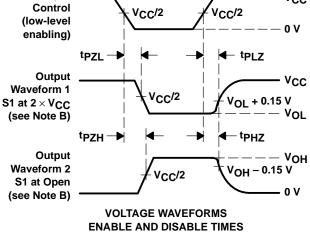


TEST	S 1
^t pd	Open
t _{PLZ} /t _{PZL}	2×V _{CC}
tPHZ/tPZH	GND







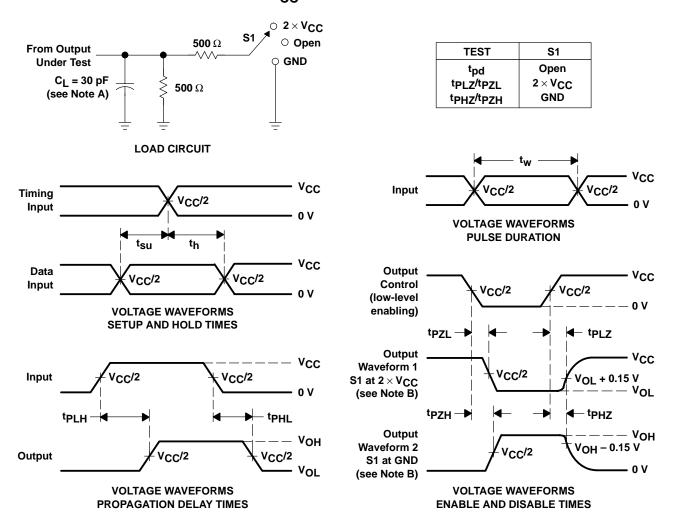


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

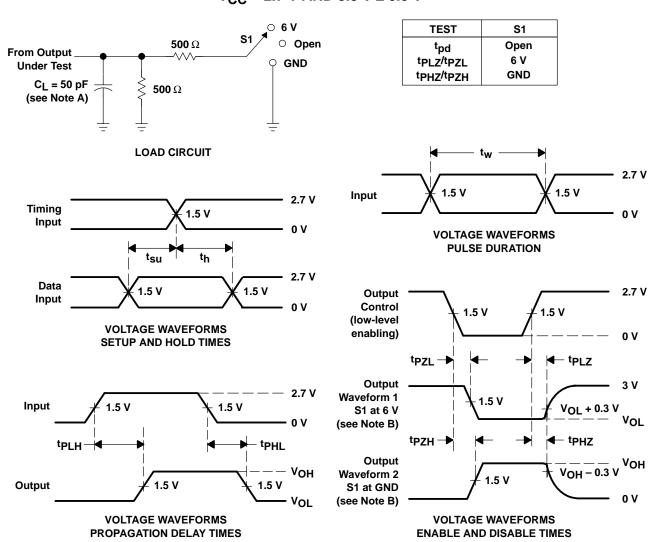


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpz and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V

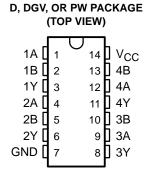


- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

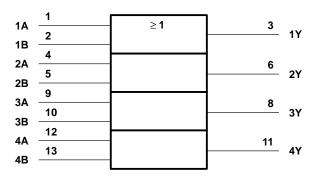
The SN74ALVC32 performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or Y = A + B in positive logic.

The SN74ALVC32 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	INPUTS OUTP					
Α	В	Y				
Н	Χ	Н				
Х	Н	Н				
L	L	L				

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		50 mA
Output clamp current, I _{OK} (V _O < 0)		−50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	: D package	127°C/W
•	DGV package	182°C/W
	PW package	170°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
ViH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ı	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
	High level output ourrent	V _{CC} = 2.3 V		-12	m Λ
ІОН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Lour lovel output ourrent	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		vcc	MIN	TYP	MAX	UNIT
	I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	I _{OH} = -6 mA		2.3 V	2			
Voн			2.3 V	1.7			V
	I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA		3 V	2			
	I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VOL	$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL	I _{OL} = 12 mA		2.3 V			0.7	V
	IOL = 12 IIIA		2.7 V			0.4	
	I _{OL} = 24 mA		3 V			0.55	
lį	$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND		3.3 V		4		pF

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

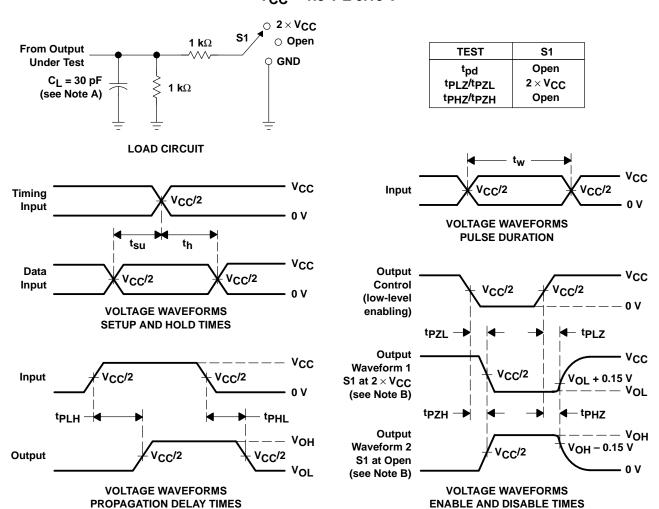
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V				V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	4.7	1	3.1		2.9	1	2.8	ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	$C_L = 0$, $f = 10 MH$	z 23	24	26	pF

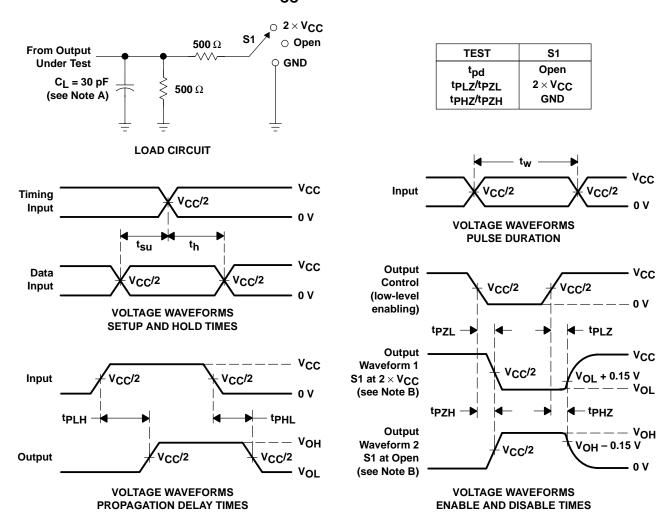
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

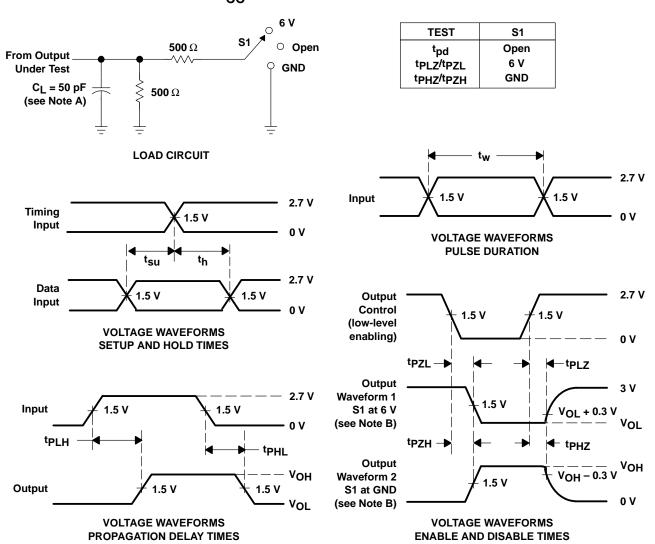


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **Package Options Include Plastic** Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) **Packages**

(TOP VIEW) 1CLR [□ v_{cc} 1D [13 2 CLR 2 1CLK [] 3 12 ¶ 2D 1PRE **[**] 4 11 2CLK 1Q [10 1 2 PRE 1Q [9 2Q 6 8 2 Q GND

D, DGV, OR PW PACKAGE

description

This dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

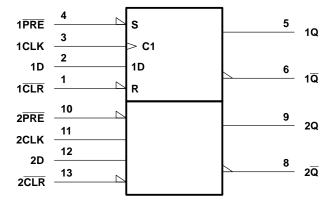
The SN74ALVC74 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Χ	L	Н
L	L	X	Χ	н†	H [†]
Н	Н	\uparrow	Н	Н	L
Н	Н	\uparrow	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

[†]This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

logic symbol†



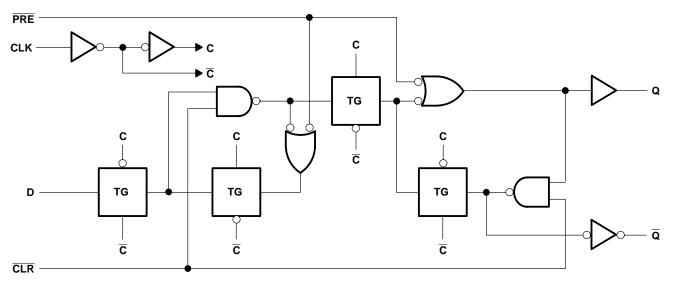
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DGV package	182°C/W
PW package	170°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
lau	High level output ourrent	$V_{CC} = 2.3 \text{ V}$		-12	
ІОН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low-level output current	V _{CC} = 2.3 V		12	m Λ
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc}	MIN	TYPT MA	X UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.2	2	
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -6 \text{ mA}$	2.3 V	2		
Voн		2.3 V	1.7		V
	I _{OH} = -12 mA	2.7 V	2.2		
		3 V	2.4		
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	1.65 V to 3.6 V		C	.2
	I _{OL} = 4 mA	1.65 V		0.	15
V	I _{OL} = 6 mA	2.3 V		C	.4 V
VOL	In. 42 mA	2.3 V		C	.7 V
	I _{OL} = 12 mA	2.7 V		C	.4
	I _{OL} = 24 mA	3 V		0.	55
lı	$V_I = V_{CC}$ or GND	3.6 V		:	:5 μA
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20 μA
∆lcc	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		7:	60 μΑ
C _i	$V_I = V_{CC}$ or GND	3.3 V			pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



SN74ALVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency										MHz
	Pulse duration	PRE or CLR low									ns
t _W	Puise duration	CLK high or low									115
	Catum time	Data before CLK↑									ns
t _{SU} Setup time	Setup time	PRE or CLR inactive									115
th	Hold time	Data after CLK↑									ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
(INPOT)	(OUTFUT)	TYP	MIN MAX	MIN MAX	MIN MAX		
f _{max}							MHz
+ .	tpd CLK Q or Q					ns	
^t pd	PRE or CLR	Q or Q					115

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST C	ONDITIONS	V _{CC} = 1.8V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	PARAMETER		TEST CONDITIONS		TYP	TYP	TYP	ONIT
	C _{pd}	Power dissipation capacitance per flip-flop	$C_{L} = 0$,	f = 10 MHz				pF

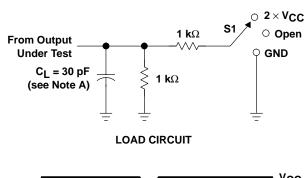


VCC

0 V

V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

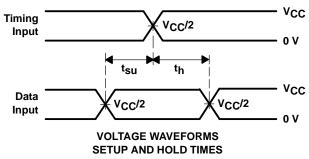


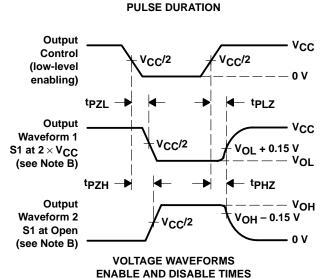
TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

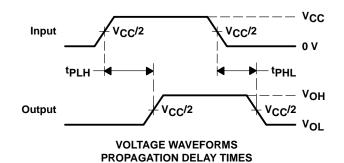
V_{CC}/2

VOLTAGE WAVEFORMS

Input







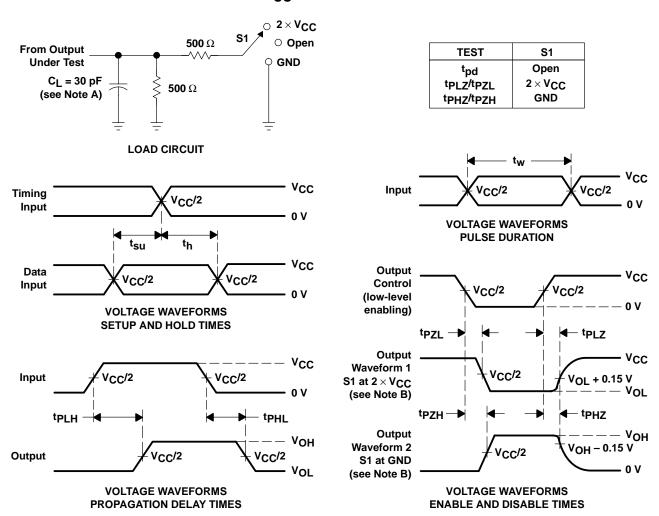
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzl and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES109E - JULY 1997 - REVISED JANUARY 1999

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

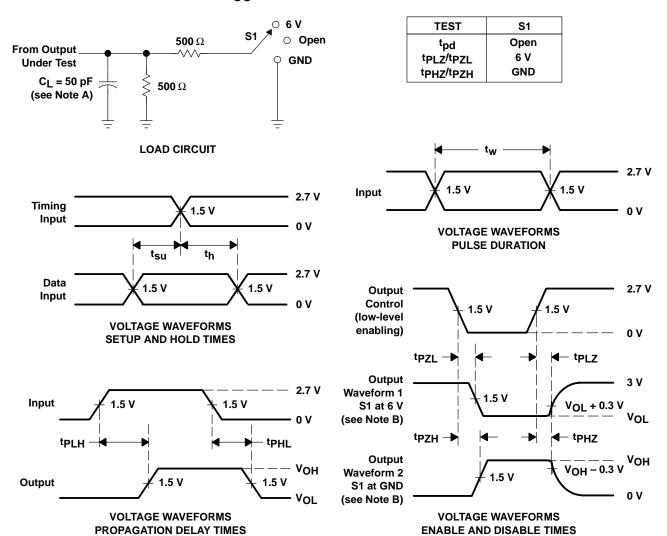


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



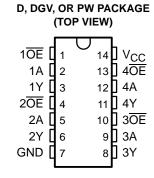
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES110D - JULY 1997 - REVISED DECEMBER 1998

- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Package Options Include Plastic** Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) **Packages**



description

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

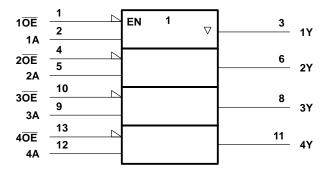
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

logic symbol[†]

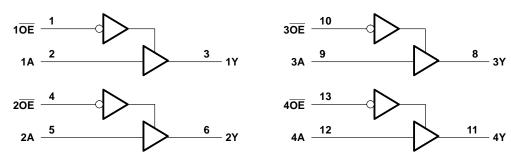


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D pa	ckage 127°C/W
DGV	package 182°C/W
PW r	package 170°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVC125 **QUADRUPLE BUS BUFFER GATE** WITH 3-STATE OUTPUTS SCES110D – JULY 1997 – REVISED DECEMBER 1998

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$				
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lou	IPak lavel autout assess t	V _{CC} = 2.3 V		-12	^	
IOH	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	m 1	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	.2			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2					
		I _{OH} = -6 mA		2.3 V	2				
Vон				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
		I _{OH} = -24 mA	3 V	2					
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45		
		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V	
VOL		lo 12 mA		2.3 V			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4			
		I _{OL} = 24 mA	3 V			0.55			
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			10	μΑ	
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
C:	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		nE.	
Ci	Data inputs	AL = ACC OLGIAD		3.3 v		3.5		pF	
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		5.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =		VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT) (OC	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	Α	Υ	1.3	5.3	1	3.2		3.1	1.1	2.8	ns
t _{en}	ŌĒ	Υ	1.4	6.4	1	4.1		4.3	1	3.5	ns
t _{dis}	ŌĒ	Y	1.8	5.9	1	3.4		4	1.4	4	ns

operating characteristics, $T_A = 25^{\circ}C$

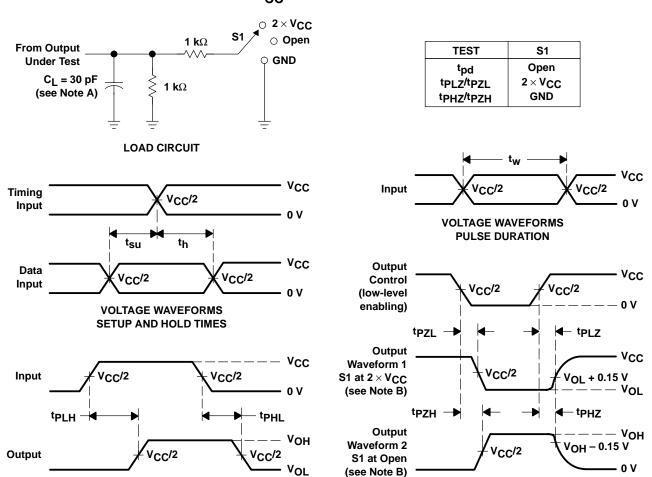
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C Power dissipation		Outputs enabled	C _L = 0,	15	17	19	pF
Cpd	capacitance per gate	Outputs disabled	f = 10 MHz	2	2	3	рг



VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

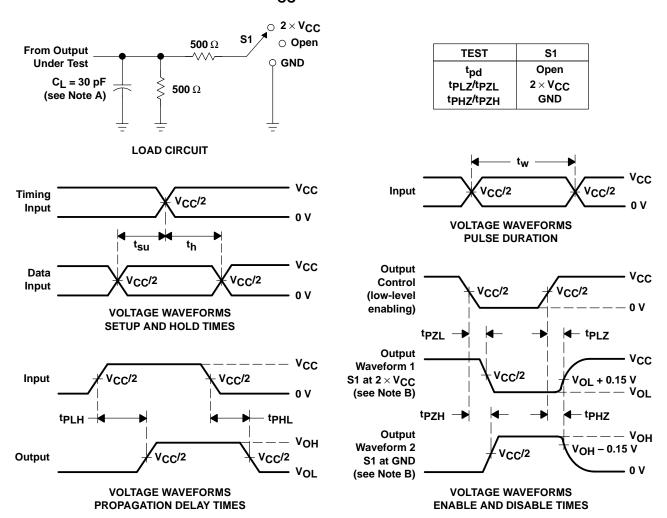
VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



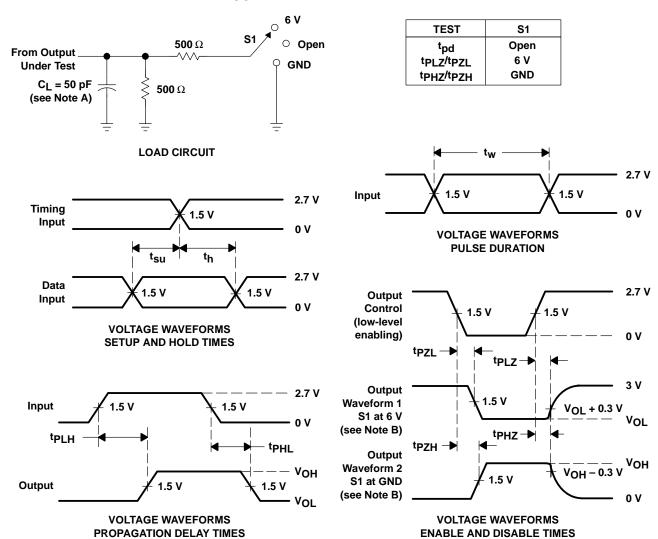
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



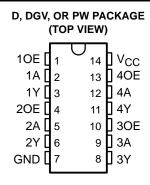
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES111E - JULY 1997 - REVISED FEBRUARY 1999

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC126 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

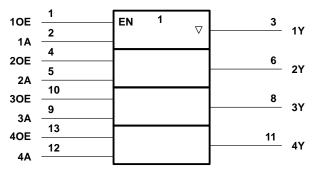
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ALVC126 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

logic symbol†

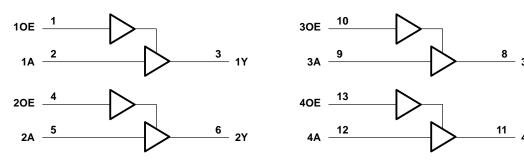


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D	package 127°C/W
DO	GV package 182°C/W
P∖	N package 170°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.65 3.6 0.65 × V _{CC} 1.7			
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
lou	LP-de land and annual	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA	
lOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA	
		V _{CC} = 3 V		24	1	
Δt/Δν	Input transition rise or fall rate			5	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SCES111E – JULY 1997 – REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CO	ONDITIONS	v _{cc}	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		I _{OH} = -4 mA		1.65 V	1.2	1.2			
		I _{OH} = -6 mA		2.3 V	2				
Vон								V	
VoL	I _{OH} = -12 mA		2.7 V	2.2					
			3 V	2.4					
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45	.45	
V		I _{OL} = 6 mA		2.3 V			0.4	V	
VOL		lo. − 12 m∆		2.3 V			0.7	v	
		I _{OL} = 12 mA		2.7 V		-	0.4		
		I _{OL} = 24 mA		3 V			0.55		
IĮ		V _I = V _{CC} or GND		3.6 V			±5	μА	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μА	
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			10	μА	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V		-	750	μА	
0.	Control inputs	V V or CND		227		3.5			
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF	
Со	Outputs	$V_O = V_{CC}$ or GND		3.3 V		5.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =		VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	1.3	5.6	1	3.4		3.4	1.1	3.1	ns
t _{en}	OE	Υ	1	5.9	1	3.8		3.8	1	3.3	ns
^t dis	OE	Y	1.8	5.6	1	3.3		4.4	1	3.7	ns

operating characteristics, T_A = 25°C

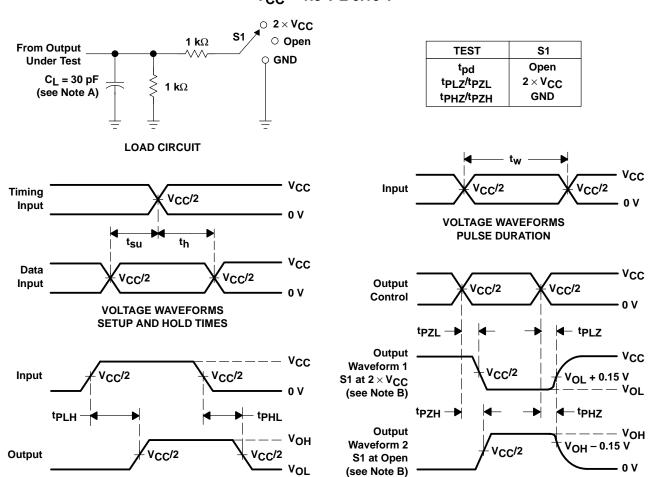
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
Power dissipation	Power dissipation	Outputs enabled	C _L = 0,	15	17	19	
Cpd	capacitance per gate	Outputs disabled	f = 10 MHz	2	2	3	pF



VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.

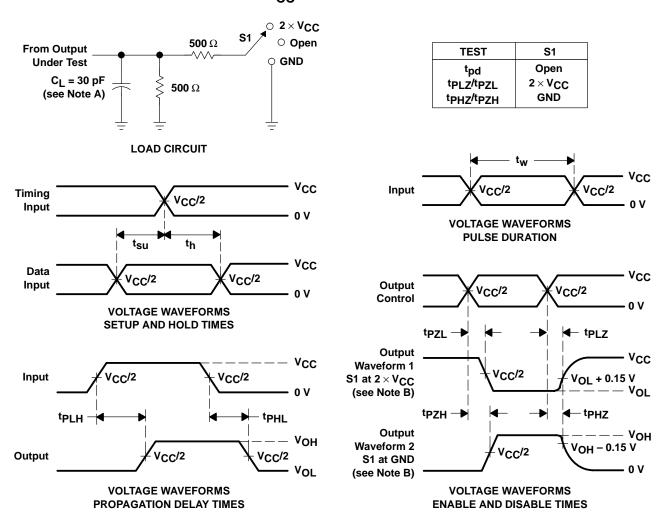
VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



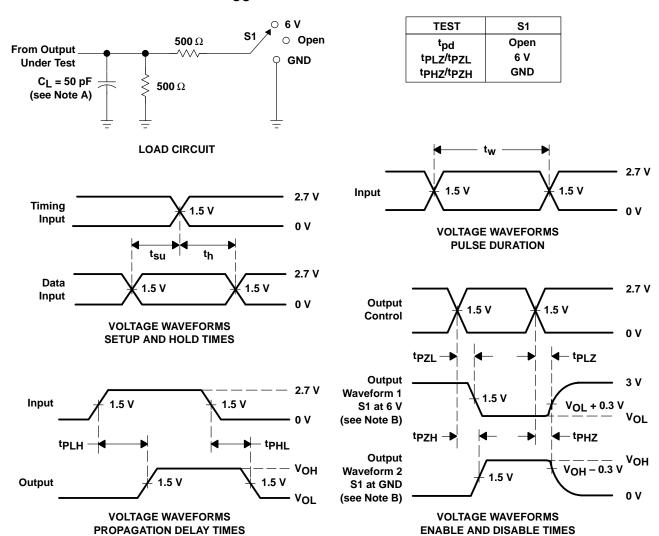
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{\mbox{\footnotesize CC}}$ = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

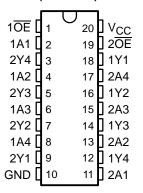
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES188 - FEBRUARY 1999

- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Package Options Include Plastic Small-Outline (DW, NS), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

DGV, DW, NS, OR PW PACKAGE (TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC244 is organized as two 4-bit line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When $\overline{\sf OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

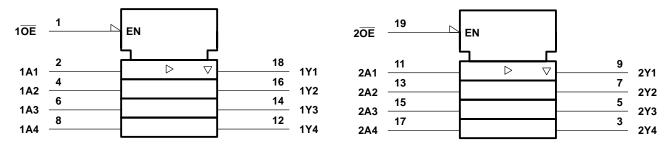
The SN74ALVC244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

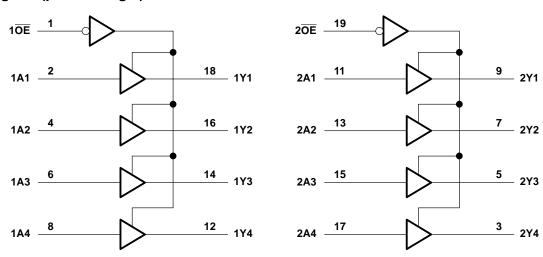
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		–0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I_{OK} ($V_O < 0$)		
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	: DGV package	146°C/W
	DW package	97°C/W
	NS package	100°C/W
	PW package	128°C/W
Storage temperature range, T _{sta}		–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
lou	High level output ourrent	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA	
		V _{CC} = 3 V		0.35 × V _{CC} 0.7 0.8 V _{CC} V _{CC} -4 -12		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12		
lOL	Low-level output current	V _{CC} = 2.7 V	12		mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			5	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$		2.3 V	2				
Vон			2.3 V	1.7			V		
$I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OL} = 100 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$	I _{OH} = -12 mA		2.7 V	2.2					
			3 V	2.4]		
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V	3.6 V		0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
\/o\	V	I _{OL} = 6 mA		2.3 V			0.4	V	
VOL		I _{OL} = 12 mA		2.3 V			0.7		
		IOL = 12 IIIA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			10	μΑ	
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
C.	Control inputs	V _I = V _{CC} or GND		3.3 V		4.5		"F	
Ci	Data inputs	AL = ACC OLGIAD		3.3 v		4.5		pF	
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

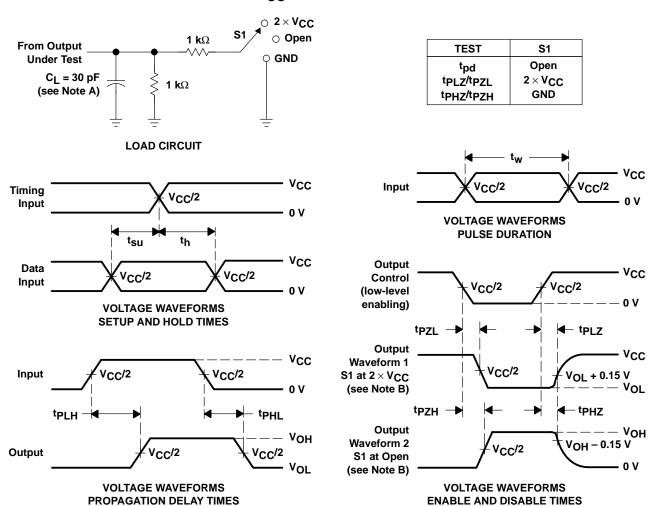
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =		VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	Α	Υ	1	4.4	1	3.1		3.1	1.1	2.8	ns
t _{en}	ŌĒ	Υ	1.8	6.9	1.5	5.4		5.3	1.5	4.5	ns
^t dis	ŌĒ	Y	1.8	5.9	1	4.1		4.4	1.7	4.2	ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			001121110110	HIF	1117	IIF	<u> </u>
C .	Power dissipation capacitance	Outputs enabled	C _L = 0,	22	23	26	pF
Cpd	per buffer/driver	Outputs disabled	f = 10 MHz	1	1	1	PΓ



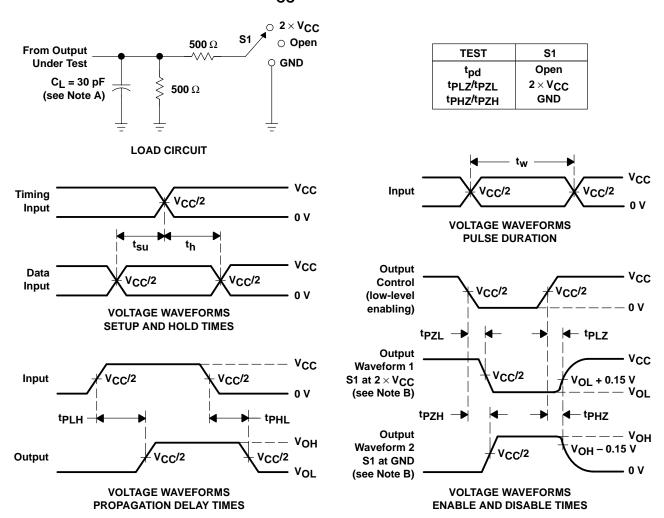
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



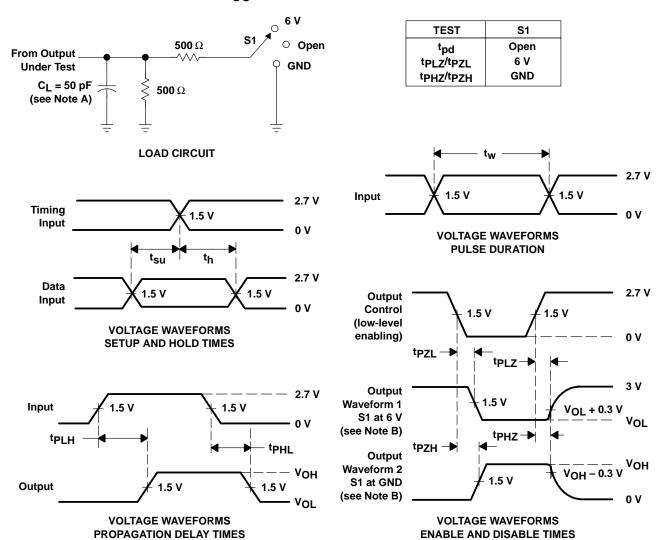
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns. $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

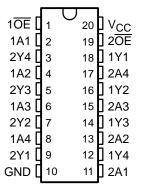
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES112C - JULY 1997 - REVISED FEBRUARY 1999

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW, NS), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

DGV, DW, NS, OR PW PACKAGE (TOP VIEW)



description

This octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

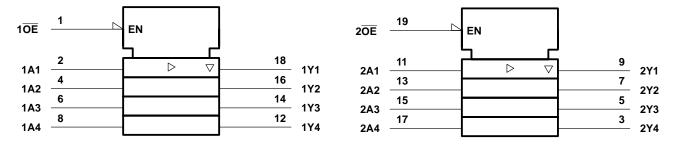
The SN74ALVCH244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

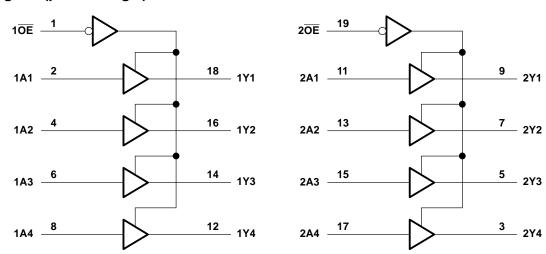
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		–0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I_{OK} ($V_O < 0$)		
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	: DGV package	146°C/W
	DW package	97°C/W
	NS package	100°C/W
	PW package	128°C/W
Storage temperature range, T _{sta}		–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
lau	High level output ourrent	V _{CC} = 2.3 V		-12	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-12	7 '''A	
		V _{CC} = 3 V		0.35×V _{CC} 0.7 0.8 V _{CC} V _{CC} -4 -12		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrant	V _{CC} = 2.3 V		12	0	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			5	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
VOН			2.3 V	1.7			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
\ \/ - :		I _{OL} = 6 mA	2.3 V			0.4	.,
VOL		L- 40 mA	2.3 V			0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
Ιį		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	§			
		V _I = 1.07 V	1.65 V	§			
		V _I = 0.7 V	2.3 V	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
` ´		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			10	μΑ
Δlcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		4.5		pF
<u> </u>	Data inputs	Al - ACC or GIAD	3.3 v		6		þι
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		8		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	§	1	3.1		3.1	1.1	2.8	ns
t _{en}	ŌĒ	Υ	§	1.5	5.4		5.3	1.5	4.5	ns
t _{dis}	ŌĒ	Y	§	1	4.1		4.4	1.7	4.2	ns

[§] This information was not available at the time of publication.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

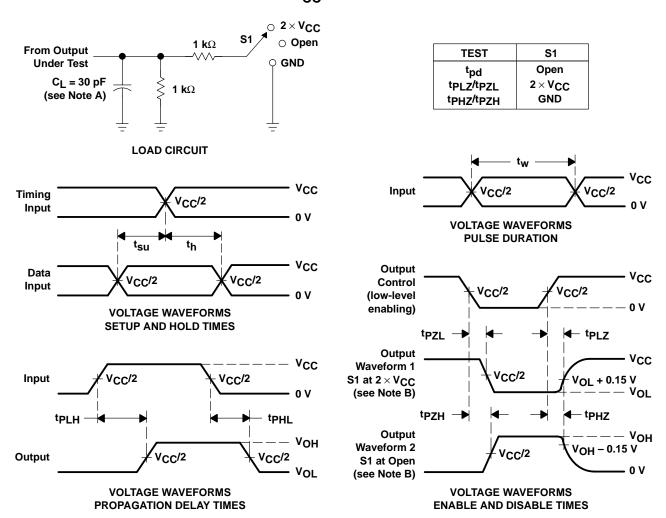
[§] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			CONDITIONS	TYP	TYP	TYP	
<u> </u>	Power dissipation capacitance	Outputs enabled	C ₁ = 0, f = 10 MHz	†	22	28	pF
C _{pd}	per buffer/driver	Outputs disabled	CL = 0, 1 = 10 MH2	†	1.5	4	þΓ

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



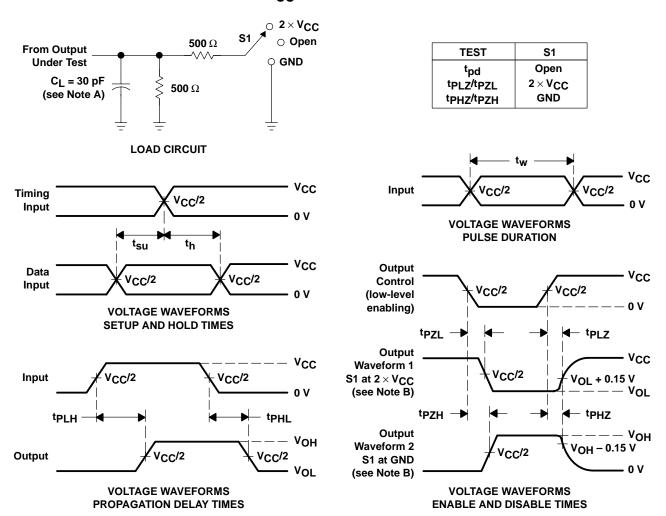
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

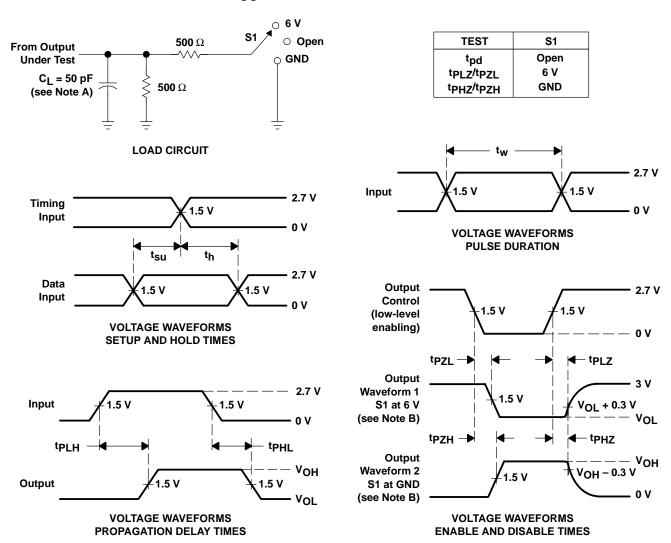


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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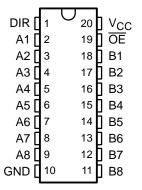
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **Package Options Include Plastic** Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

This octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

DGV, DW, OR PW PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

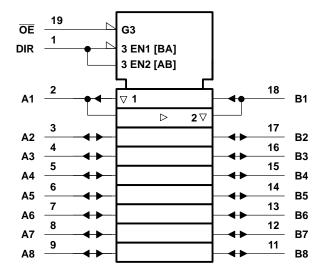
The SN74ALVC245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INP	UTS	OPERATION			
OE	DIR	OPERATION			
L	L	B data to A bus			
L	Н	A data to B bus			
Н	X	Isolation			

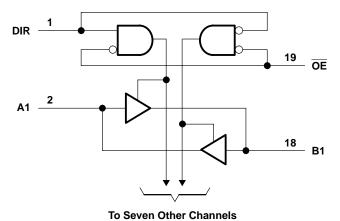
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCES271A - APRIL 1999 - REVISED MAY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGV package	
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
$V_{CC} = 1.65 \text{ V to } 1.9 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.3 \text{ V to } 2.7 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.7 \text{ V to } 3.6 \text{ V}_{CC} = 2.3 \text{ V}_{CC} = 2.$	V _{CC} = 2.7 V to 3.6 V	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
\vee_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ı	Input voltage	•	0	VCC	V
۷o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V	to 1.95 V		
		V _{CC} = 1.65 V		4	
	Lave lavel and and annual	V _{CC} = 2.3 V		12	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
\/ - ·		I _{OL} = 6 mA	2.3 V			0.4	V
VOL						0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
Тį		V _I = V _{CC} or GND	3.6 V			±5	μΑ
loz‡		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			10	μΑ
ΔlCC		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		-	750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		4.5		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		11.5		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT	
		(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	^t pd	A or B	B or A	1.5	6	1	3.5		3.6	1.3	3.4	ns
	t _{en}	ŌĒ	A or B	3.4	8.6	2	6		6.3	1.6	5.5	ns
	^t dis	ŌĒ	A or B	2.7	8	1	4.8		5.3	1.7	5.5	ns

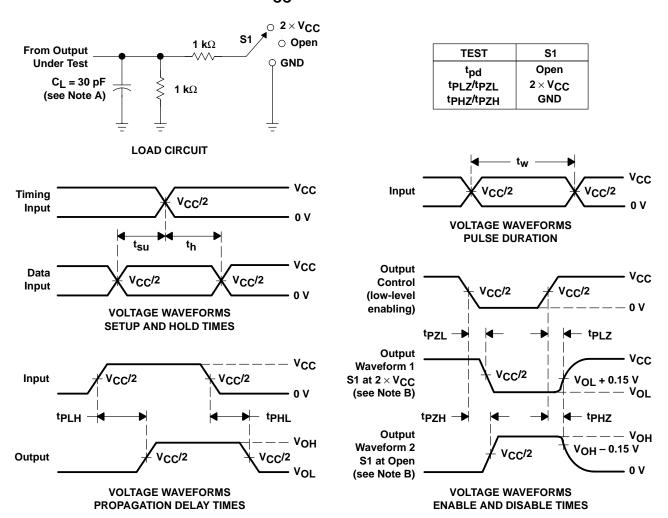
operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	VCC = 3.3 V	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation capacitance	Outputs enabled	Cı = 0. f = 10 MHz	25	27	30	PΓ
Cpd	per transceiver	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	0	0	0	рг



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V \pm 0.15 V$

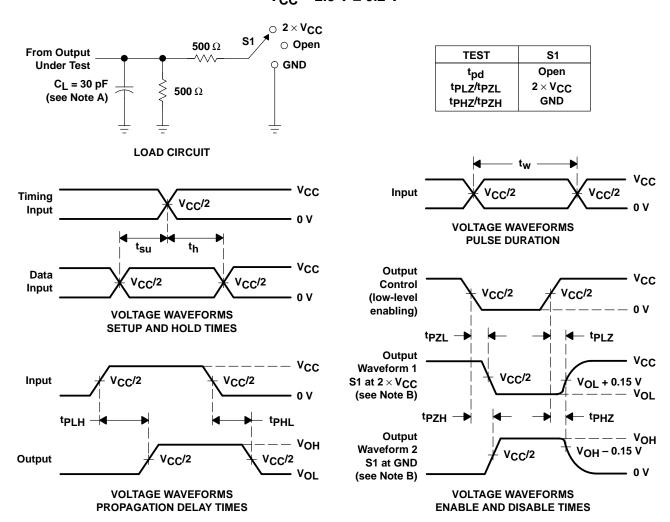


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



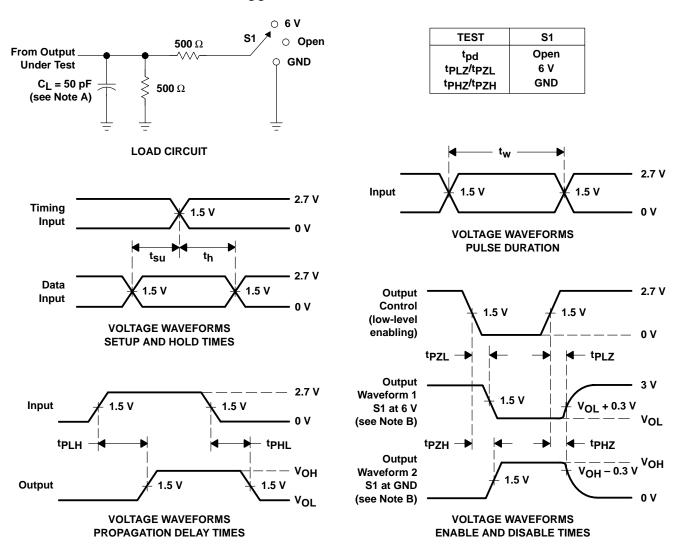
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- $\ensuremath{\mathsf{D}}.$ The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SCES119D - JULY 1997 - REVISED MAY 1999

- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Latch-Up Performance Exceeds 100 mA Per **JESD 78, Class II**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic** Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW) ի v_{cc} DIR [20 А1 П 19 \ OE A2 **∏** 3 18 B1 A3 **∏** 4 17 **∏** B2 A4 **∏** 5 16 **∏** B3 A5 **∏** 6 15 B4 A6 **∏** 7 14 **∏** B5 А7 П 8 13 **∏** B6 A8 🛮 9 12 B7 GND **1**10 11 **|** B8

DGV, DW, OR PW PACKAGE

description

This octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{\rm OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH245 is characterized for operation from -40°C to 85°C.

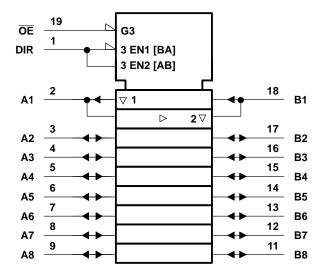
FUNCTION TABLE

INP	UTS	OPERATION		
OE	DIR	OPERATION		
L	L	B data to A bus		
L	Н	A data to B bus		
Н	X	Isolation		

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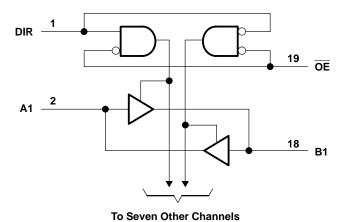


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCES119D - JULY 1997 - REVISED MAY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGV package	
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	IPak lasak satast samast	V _{CC} = 2.3 V		-12	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Lave lavel autout august	V _{CC} = 2.3 V		12	A	
lol	Low-level output current	V _{CC} = 2.7 V		12	mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
Vон		I _{OH} = -4 mA		1.65 V	1.2				
		I _{OH} = -6 mA		2.3 V	2				
				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
VOL		I _{OL} = 6 mA		2.3 V			0.4	V	
VOL		I _{OI} = 12 mA		2.3 V			0.7		
		IOL = 12 IIIA	2.7 V			0.4			
		I _{OL} = 24 mA	3 V			0.55			
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V	1.65 V	-25			μΑ		
		V _I = 0.7 V	2.3 V	45					
I _{l(hold)}		$V_{I} = 1.7 \text{ V}$ $V_{I} = 0.8 \text{ V}$ $V_{I} = 2 \text{ V}$		2.3 V	-45				
				3 V	75				
				3 V	-75				
loz§		V _I = 0 to 3.6 V [‡]		3.6 V			±500		
		$V_O = V_{CC}$ or GND,		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			10	μΑ	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4.5		pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		12		pF	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	<u>]</u>	
t _{pd}	A or B	B or A	1.5	6	1	3.5		3.6	1.3	3.4	ns	
t _{en}	ŌĒ	A or B	3.4	8.6	2	6		6.3	1.6	5.5	ns	
^t dis	ŌĒ	A or B	2.7	8	1	4.8		5.3	1.7	5.5	ns	

operating characteristics, T_A = 25°C

	PARAMETER Power dissipation capacitance per transceiver Outputs enabled Outputs disabled		TEST	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
FARAWETER		CONDITIONS	TYP	TYP	TYP	ONIT		
C .	Power dissipation capacitance	Outputs enabled	C _L = 0,	25	28	31	nE.	
Cpd	per transceiver	Outputs disabled	(40 14)	0	0	0	pF	

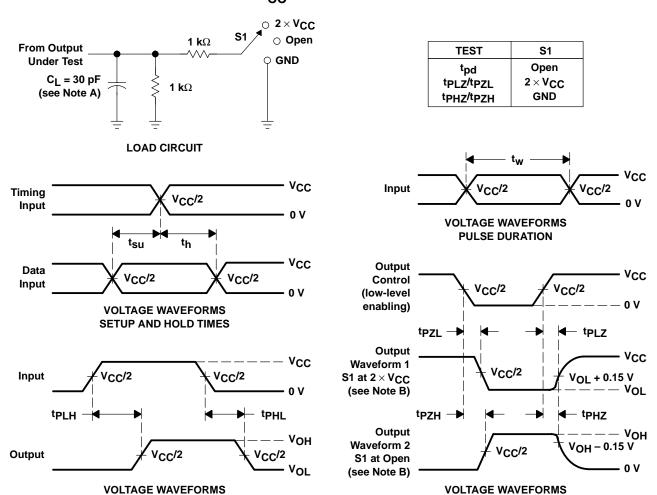


[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\ensuremath{\,\hat{}}}$ For I/O ports, the parameter IOZ includes the input leakage current.

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$



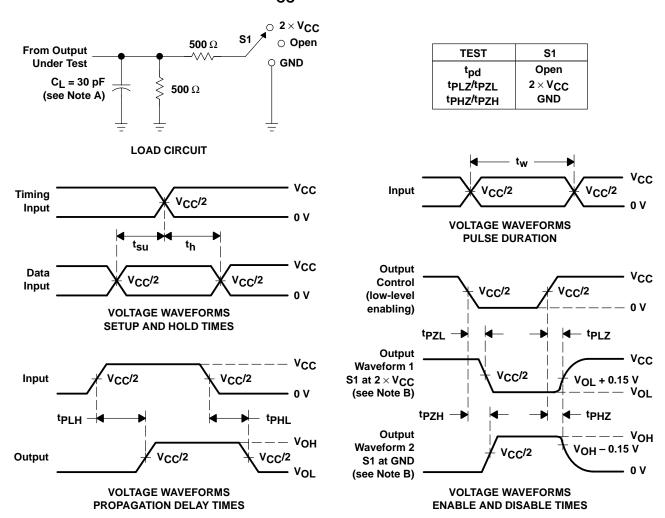
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



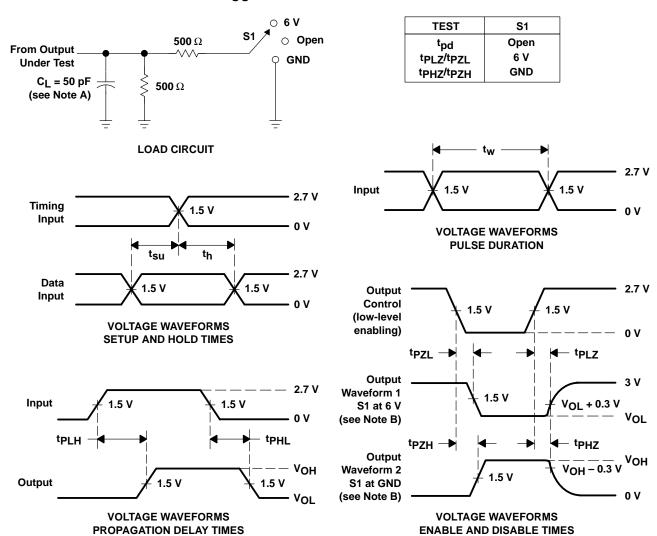
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{\mbox{\footnotesize CC}}$ = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES116D - JULY 1997 - REVISED JANUARY 1999

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW) 20 🛮 V_{CC} OE 1Q [19 1 8Q 1D 🛮 3 18 8D 2D Π 17 **[**] 7D 2Q 16 ∏ 7Q 3Q 15 \ 6Q 3D ∏ 6D 14 4D **∏** 8 13 T 5D 4Q 🛮 9 12 🛮 5Q GND II 10 11 **∏** LE

DGV, DW, OR PW PACKAGE

description

This octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH373 is characterized for operation from -40°C to 85°C.

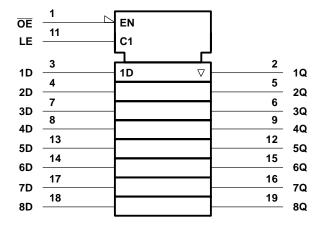
FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q_0
Н	Χ	Χ	Z

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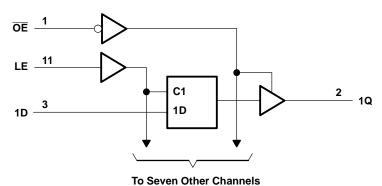


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	0.5	5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		. –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH373 **OCTAL TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCES116D – JULY 1997 – REVISED JANUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
VIН	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4	mA	
	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12		
ІОН	High-level output current	V _{CC} = 2.7 V		-12		
	V _{CC} = 3 V			-24		
		V _{CC} = 1.65 V		4		
la.	Low level output ourrent	V _{CC} = 2.3 V		12	m 1	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate			5	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	.2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон		I _{OH} = –12 mA		2.3 V	1.7			V
				2.7 V	2.2			
			3 V	2.4				
		I _{OH} = -24 mA	3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45		
Vai	Iou = 6 mA		2.3 V			0.4	.,	
VOL		lo 12 mΔ	2.3 V			0.7	V	
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V				
		V _I = 1.07 V		1.65 V				
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±425	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	VI = Voc or GND		3.3 V				n.E
Ci	Data inputs $V_I = V_{CC}$ or GND			3.3 v	0.0 v			pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		v _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	!
t _W	Pulse duration, LE high									ns
t _{su}	Setup time, data before LE↓									ns
th	Hold time, data after LE↓									ns

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

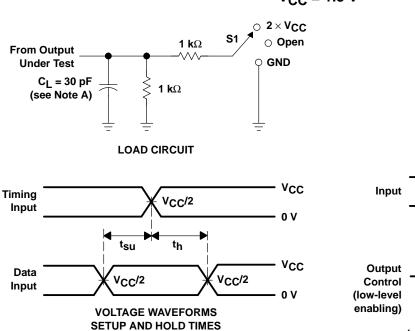
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

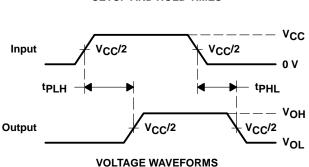
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INFOT)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN MAX	
4 .	D	0					no
^t pd	LE	Q					ns
^t en	ŌĒ	Q					ns
^t dis	ŌĒ	Q					ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		CONDITIONS	TYP	TYP	TYP		
C .	Power dissipation capacitance	Outputs enabled	C _L = 0,				pF
Cpd	per latch	Outputs disabled	f = 10 MHz				рг

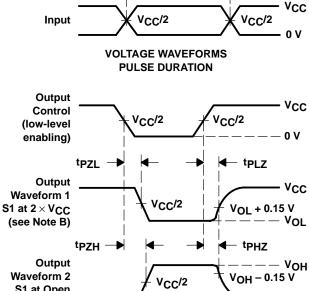
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





PROPAGATION DELAY TIMES

TEST S1 Open tpd $\textbf{2} \times \textbf{V}_{\textbf{CC}}$ tPLZ/tPZL **GND** tPHZ/tPZH



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- 0 V

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

S1 at Open

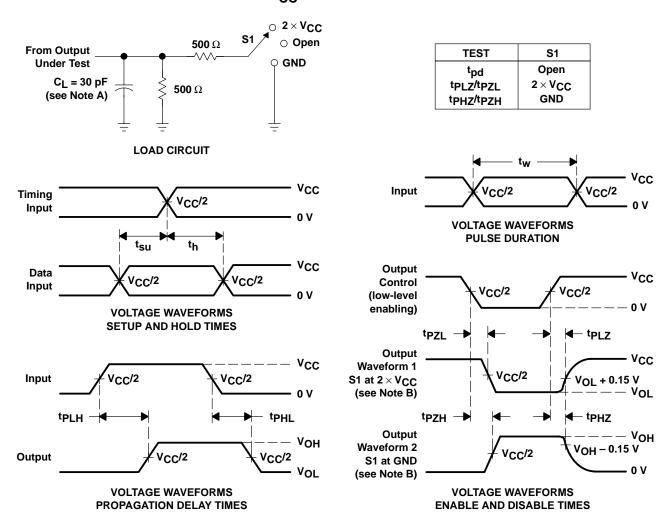
(see Note B)

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



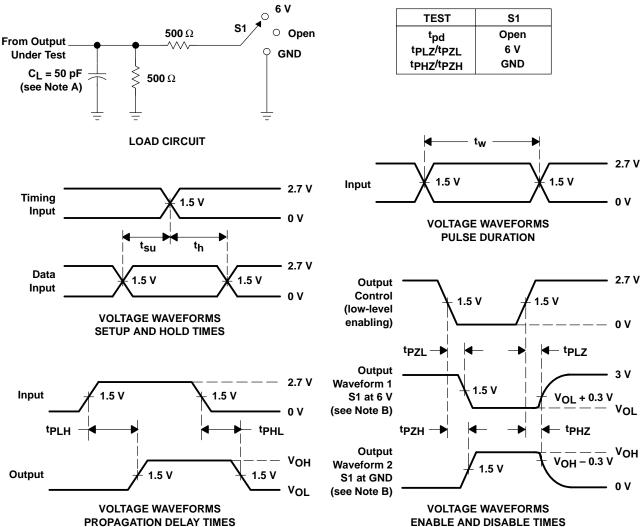
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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SN74ALVCH374 OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES118D - JULY 1997 - REVISED JANUARY 1999

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

DGV, DW, OR PW PACKAGE (TOP VIEW) 1 V_{CC} OE 1Q [19 8Q 1D 🛮 3 18 NBD 2D Π Π 7D 17 2Q 16 ∏ 7Q 3Q 15 ∏ 6Q 3D ∏ 6D 14 4D ∏ 8 13 **∏** 5D 4Q 🛛 9 12 🛮 5Q GND II 10 11 CLK

description

This octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

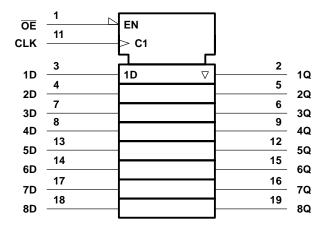
	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	Х	Х	Z

EPIC is a trademark of Texas Instruments Incorporated.



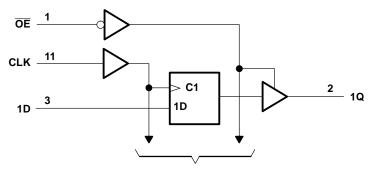
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	0.5	5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T _{stg}		. –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH374 OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCES118D – JULY 1997 – REVISED JANUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lau	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
lai	Low-level output current	V _{CC} = 2.3 V		12	mA	
lOL	Low-level output current	V _{CC} = 2.7 V		12		
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate			5	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0	2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA	3 V	2				
		I _{OL} = 100 μA					0.2	
		I _{OL} = 4 mA	1.65 V			0.45		
1/		I _{OL} = 6 mA	2.3 V			0.4		
VOL			2.3 V			0.7	V	
		I _{OL} = 12 mA		2.7 V		-	0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V				
		V _I = 1.07 V	1.65 V					
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
,		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±425	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			20	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs Data inputs	V _I = V _{CC} or GND		3.3 V				pF
Co	 	VO = VCC or GND		3.3 V				pF
	Control inputs Data inputs Outputs		Other Imputs at ACC of GND				750	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		v _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency									MHz
t _W	Pulse duration, CLK high or low									ns
t _{su}	Setup time, data before CLK↑									ns
th	Hold time, data after CLK↑									ns



PRODUCT PREVIEW

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH374 OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCES118D – JULY 1997 – REVISED JANUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

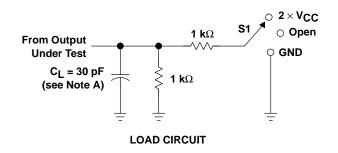
PARAMETER	FROM (INPUT)	TO V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(1141-01)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN MAX	
f _{max}							MHz
^t pd	CLK	Q					ns
^t en	ŌĒ	Q					ns
^t dis	ŌĒ	Q					ns

operating characteristics, T_A = 25°C

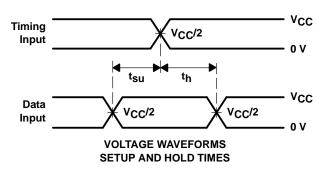
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 TYP	UNIT	
	Power dissipation capacitance	Outputs enabled	C _L = 0,				pF
C _{pd}	per flip-flop	Outputs disabled	f = 10 MHz				ρi

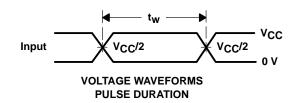


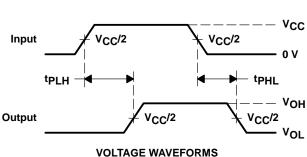
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



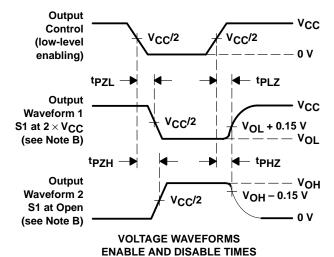
TEST	S 1
t _{pd}	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND







PROPAGATION DELAY TIMES



NOTES: A. C_L includes probe and jig capacitance.

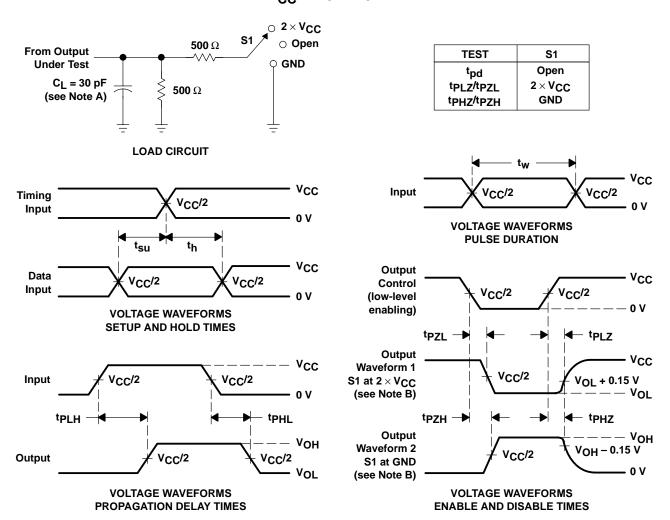
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

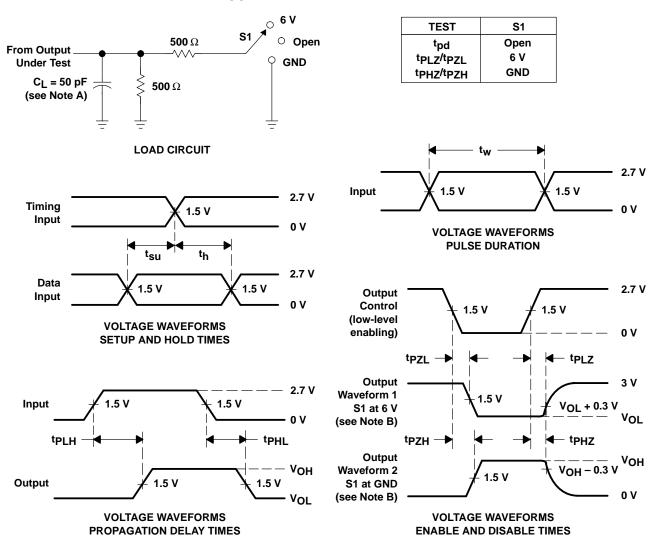


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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SN74ALVCH16652	16-Bit Bus Transceiver and Register With 3-State Outputs	3–251
SN74ALVCH16721	3.3-V 20-Bit Flip-Flop With 3-State Outputs	
SN74ALVCH16820	3.3-V 10-Bit Flip-Flop With Dual Outputs and 3-State Outputs	
SN74ALVCH16821	3.3-V 20-Bit Bus-Interface Flip-Flop With 3-State Outputs	
SN74ALVCH16823	18-Bit Bus-Interface Flip-Flop With 3-State Outputs	
SN74ALVCH16825	18-Bit Buffer/Driver With 3-State Outputs	
SN74ALVCH16827	20-Bit Buffer/Driver With 3-State Outputs	3–307
SN74ALVCH16828	20-Bit Buffer/Driver With 3-State Outputs	3–315
SN74ALVCH16830	1-Bit to 2-Bit Address Driver With 3-State Outputs	
SN74ALVCH16831	1-to-4 Address Register/Driver With 3-State Outputs	3–331
SN74ALVCH16832	1-to-4 Address Register/Driver With 3-State Outputs	
SN74ALVC16834	18-Bit Universal Bus Driver With 3-State Outputs	
SN74ALVCH16834	18-Bit Universal Bus Driver With 3-State Outputs	3–357
SN74ALVC16835	18-Bit Universal Bus Driver With 3-State Outputs	3–367
SN74ALVCH16835	18-Bit Universal Bus Driver With 3-State Outputs	3–377
SN74ALVCH16836	20-Bit Universal Bus Driver With 3-State Outputs	3–387
SN74ALVCH16841	20-Bit Bus-Interface D-Type Latch With 3-State Outputs	
SN74ALVCH16843	18-Bit Bus-Interface D-Type Latch With 3-State Outputs	
SN74ALVCH16863	18-Bit Transceiver With 3-State Outputs	
SN74ALVCH16901	18-Bit Universal Bus Transceiver With Parity Generators/Checkers	
SN74ALVCH16952	16-Bit Registered Transceiver With 3-State Outputs	3–435
SN74ALVCH32501	36-Bit Universal Bus Transceiver With 3-State Outputs	3-445

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

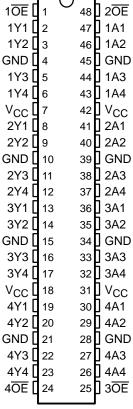
description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

DGG OR DL PACKAGE (TOP VIEW) 10E 1 48 20E



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

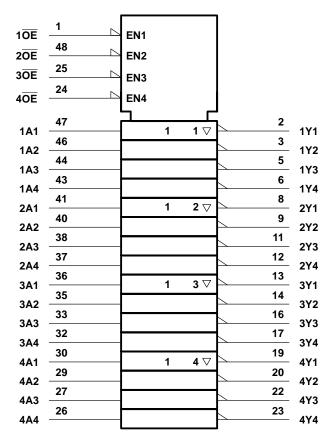
The SN74ALVCH16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	Н
Н	Χ	Z

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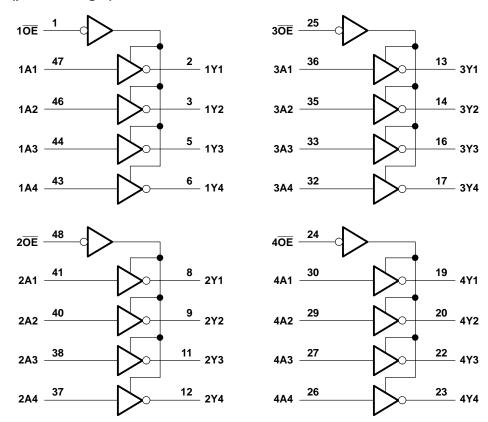
logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
1	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ЮН	High-level output current	$V_{CC} = 2.7 V$		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low-level output current	V _{CC} = 2.3 V		12		
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
			3 V	2.4				
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
V _{OL}		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	.,
		I _{OL} = 12 mA		2.3 V			0.7	V
	2.7 V					0.4		
		I _{OL} = 24 mA	3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	Control inputs Data inputs	V _I = V _{CC} or GND		3.3 V		3 6		pF
Со	Outputs	V _O = V _{CC} or GND		3.3 V		7		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Υ	§	1	5.3		5.3	1	3.9	ns
t _{en}	ŌĒ	Υ	§	1	6.4		6.1	1	5	ns
t _{dis}	ŌĒ	Υ	§	1	5.4		4.8	1	4.4	ns

[§] This information was not available at the time of publication.



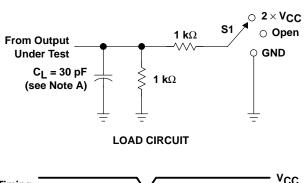
[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

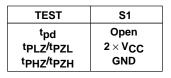
operating characteristics, $T_A = 25^{\circ}C$

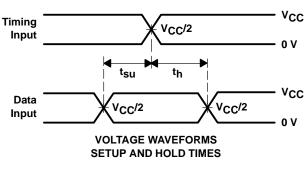
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAMETER		TEST CONDITIONS	TYP	TYP	TYP	UNIT
<u> </u>	Power dissipation	Outputs enabled	C _L = 50 pF, f = 10 MHz	†	16	19	ρF
Cpd	capacitance	Outputs disabled		†	4	5	рг

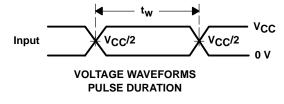
[†] This information was not available at the time of publication.

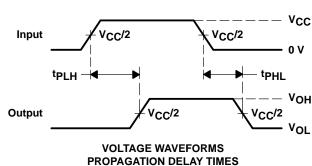
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

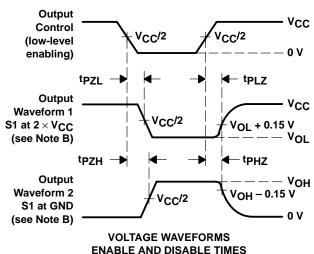












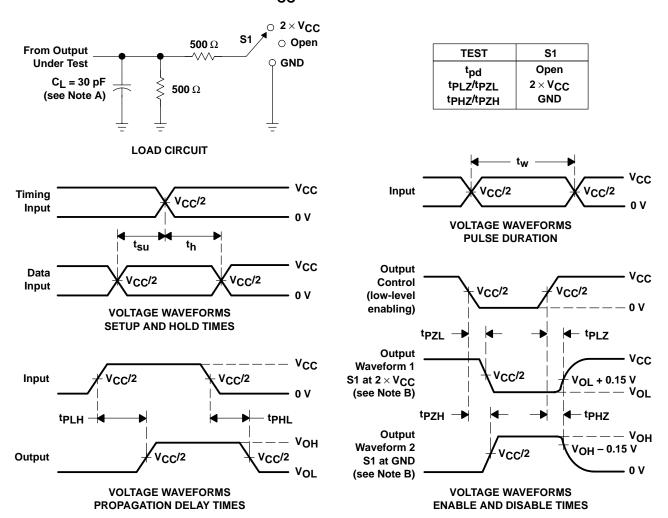
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f\leq$ 2 ns, $t_f\leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

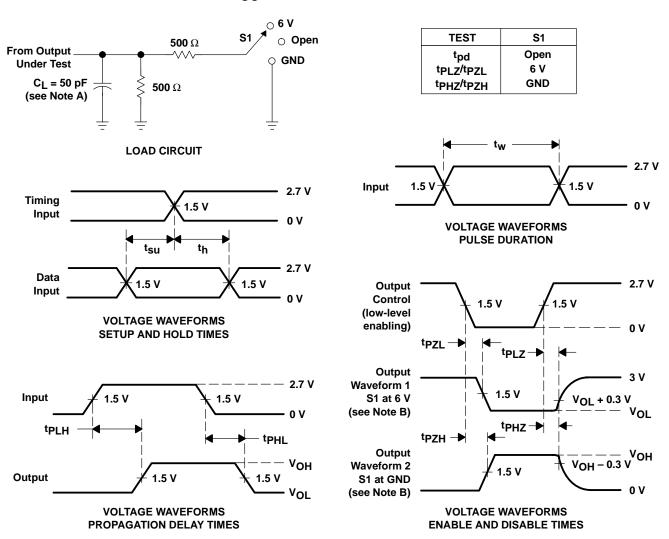


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC16244A is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true symmetrical active-low outputs and output-enable (OE) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC16244A is characterized for operation from -40°C to 85°C.

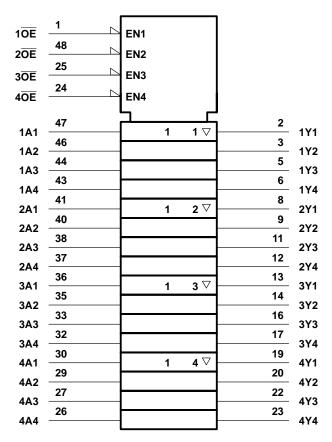
FUNCTION TABLE (each 4-bit buffer)

INPUTS		OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

DGG OR DL PACKAGE (TOP VIEW)

		$\overline{}$		
1 0E [1	O	48	2 0E
1Y1 [2		47] 1A1
	3		46] 1A2
GND [4		45	GND
1Y3 [5		44] 1A3
1Y4 [_] 1A4
	7		42] v _{cc}
2Y1 [8		41	2A1
-	9		40	2A2
-	10		39	GND
	11		38	2A3
-	12			2A4
-	13			3A1
-	14			3A2
GND [15] GND
_	16			3A3
-	17		32	3A4
	18			□ v _{cc}
	19] 4A1
	20			4A2
	21] GND
	22			4A3
	23		26	4 <u>A4</u>
4 OE [24		25	3 <u>OE</u>
	$\overline{}$			I

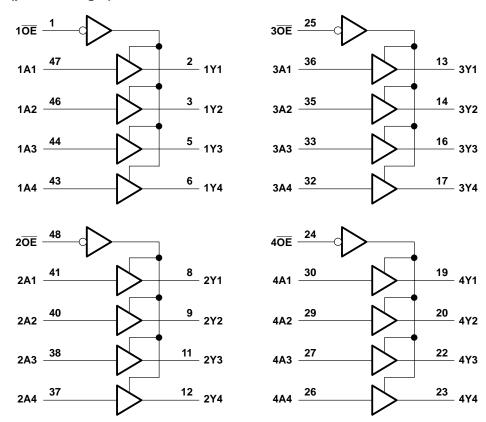
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	_	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	mA
1	High-level output current	V _{CC} = 2.3 V		-12	
ЮН		$V_{CC} = 2.7 \text{ V}$		-12	
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Lour lovel output outront	V _{CC} = 2.3 V		12	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDI	VCC	MIN	TYP	MAX	UNIT		
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2					
		I _{OH} = -6 mA	2.3 V	2					
∨он				2.3 V	1.7			V	
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2				
			3 V	2.4					
		I _{OH} = -24 mA	3 V	2					
		$I_{OL} = 100 \mu A$	1.65 V to 3.6 V			0.2			
		I _{OL} = 4 mA	1.65 V			0.45			
\/		I _{OL} = 6 mA	2.3 V			0.4	V		
VOL		I _{OL} = 12 mA		2.3 V			0.7	.7 °	
		IOF = 15 IIIA	2.7 V			0.4			
		I _{OL} = 24 mA	3 V			0.55			
П		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ		
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND, $I_O = V_{CC}$	= 0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V, Oth	er inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	Vi – Voo or CND		3.3 V		3		n.E	
Ci	Data inputs	$V_I = V_{CC}$ or GND		3.3 V	6		pF		
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(001101)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	А	Y	‡	1	3.7		3.6	1	3	ns
^t en	ŌĒ	Y	‡	1	5.7		5.4	1	4.4	ns
^t dis	ŌĒ	Y	‡	1	5.2		4.6	1	4.1	ns

[‡]This information was not available at the time of publication.

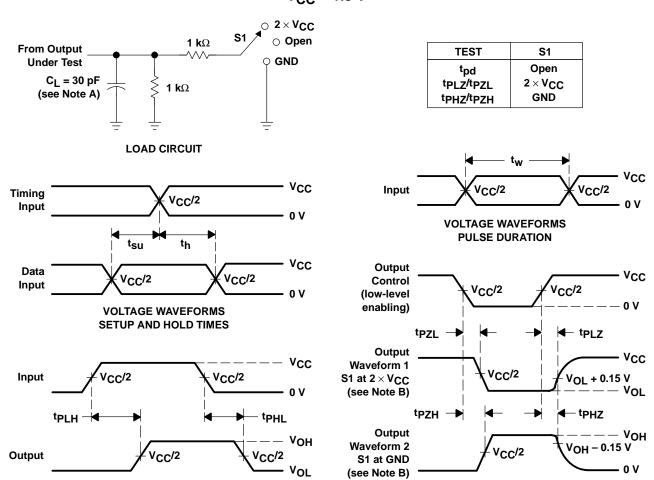
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC}		V _{CC} = 3.3 V	UNIT		
	FARAWIETER		TEST CONDITIONS	TYP	TYP	TYP	ONII	
	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	‡	16	19	PΓ	
C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	‡	4	5	рг	

[‡] This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

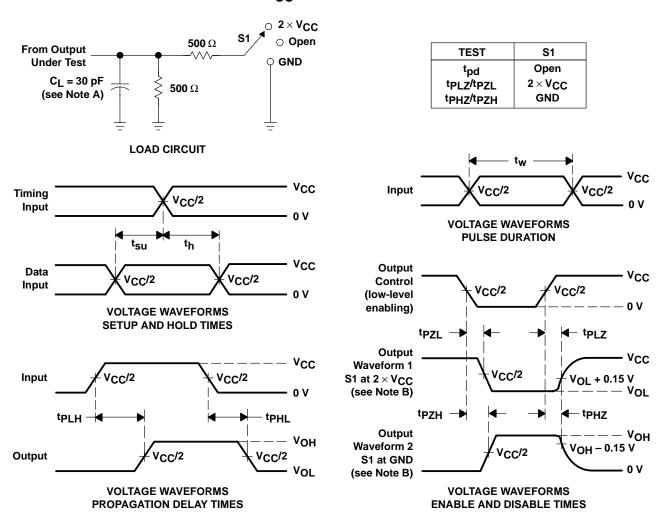
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

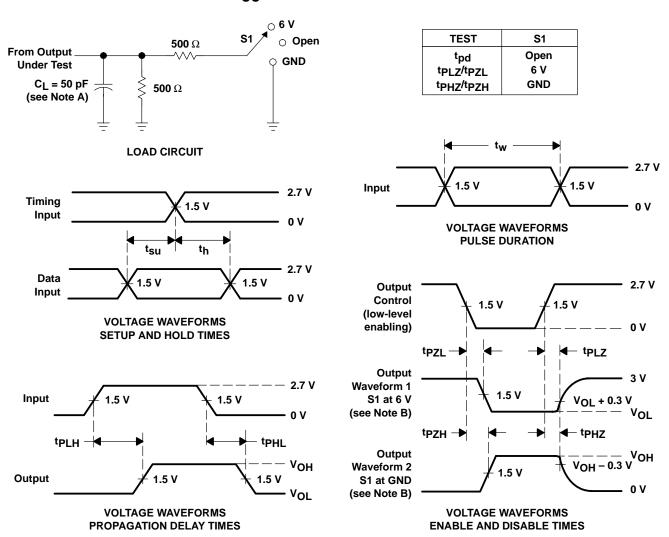


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (OE) inputs.

1OE 48 20E 1Y1 2 47 1 1A1 1Y2 ∏ 3 46 1 1A2 GND 4 45 GND 1Y3 🛮 5 44**∏** 1A3 1Y4 6 43 1A4 42 VCC V_{CC} 2Y1 🛮 8 41 2A1 2Y2 9 40 2A2 39 GND GND 10 2Y3 🛭 11 38 II 2A3 2Y4 12 37 2A4 3Y1 13 36 3A1 3Y2 114 35 3A2 GND ∏ 15 34 ∏ GND 3Y3 16 33 3A3 3Ү4 П 17 32 3A4 V_{CC} 🛚 18 31 V_{CC} 4Y1 119 30 4A1

29 🛮 4A2

28 GND 27 4A3

26 4A4 25 30E

4Y2 20

GND 21

4Y3 22

4Y4 **∏** 23

4OE **∏** 24

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

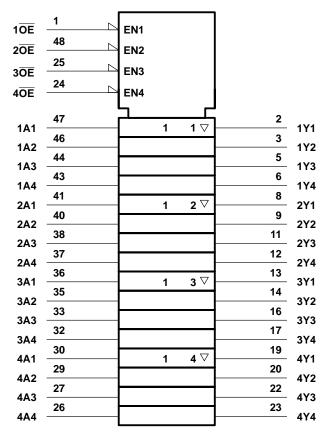
The SN74ALVCH16244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

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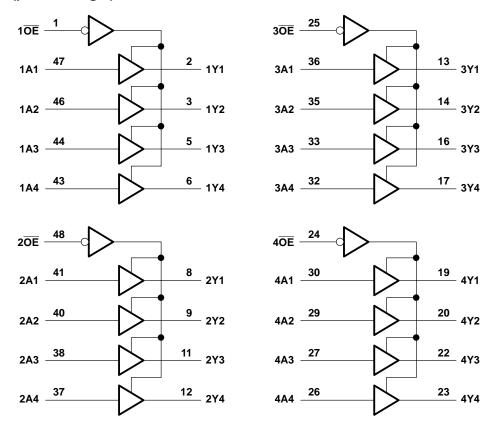
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, IOK (VO < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	: DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High-level output current	V _{CC} = 2.3 V		-12	mA
ЮН		$V_{CC} = 2.7 \text{ V}$	-12		IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low-level output current	V _{CC} = 2.3 V	12		mA
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	IIIA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT		
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	VCC-0	.2				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2					
	$I_{OH} = -6 \text{ mA}$	2.3 V	2					
Voн		2.3 V	1.7			V		
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2					
		3 V	2.4					
	$I_{OH} = -24 \text{ mA}$	3 V	2					
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2			
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45			
Va.	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V		
VOL	la. 42 mA	2.3 V			0.7	V		
	I _{OL} = 12 mA	2.7 V			0.4			
	$I_{OL} = 24 \text{ mA}$	3 V			0.55			
IJ	V _I = V _{CC} or GND	3.6 V			±5	μΑ		
	V _I = 0.58 V	1.65 V	25					
	V _I = 1.07 V	1.65 V	-25					
	V _I = 0.7 V	2.3 V	45					
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45			μΑ		
,	V _I = 0.8 V	3 V	75					
	V _I = 2 V	3 V	-75					
	$V_{\parallel} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500			
I _{OZ}	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ		
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ		
ΔI _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ		
Control inputs	Vi – Voo er CND	3.3 V		3		n.E		
C _i Data inputs	$V_I = V_{CC}$ or GND	3.3 V	6			pF		
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
	^t pd	А	Y	§	1	3.7		3.6	1	3	ns
	^t en	ŌĒ	Υ	§	1	5.7		5.4	1	4.4	ns
Г	^t dis	ŌĒ	Υ	§	1	5.2		4.6	1	4.1	ns

[§] This information was not available at the time of publication.



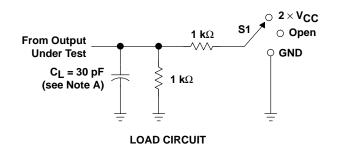
[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

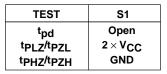
operating characteristics, $T_A = 25^{\circ}C$

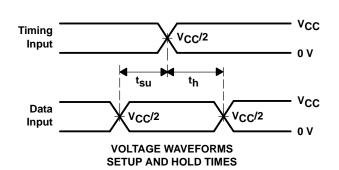
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
	· .	Power dissipation	Outputs enabled	C. FO. T. 1 10 MILE	†	16	19	ρF
Ľ	Ppd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	5	рг

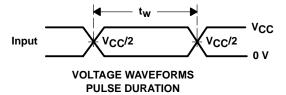
[†] This information was not available at the time of publication.

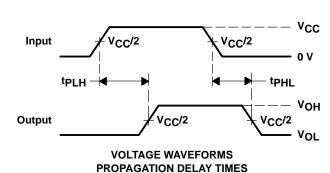
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

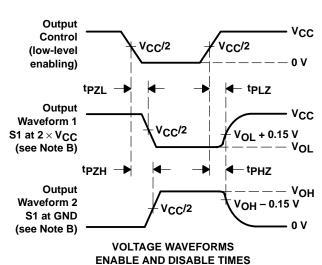










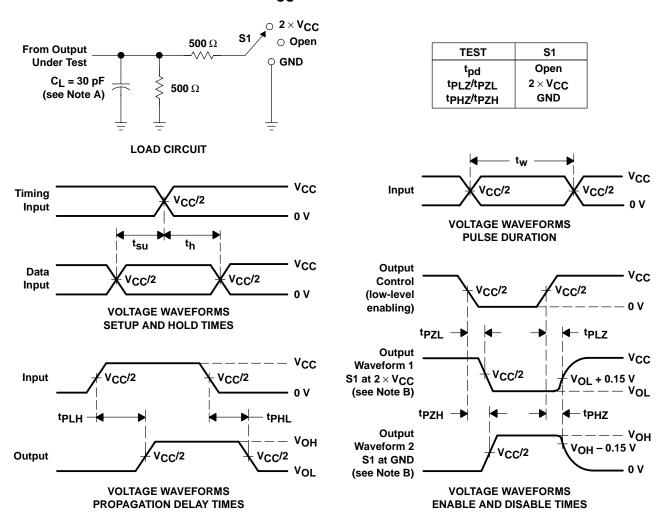


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f\leq$ 2 ns, $t_f\leq$ 2 ns,
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



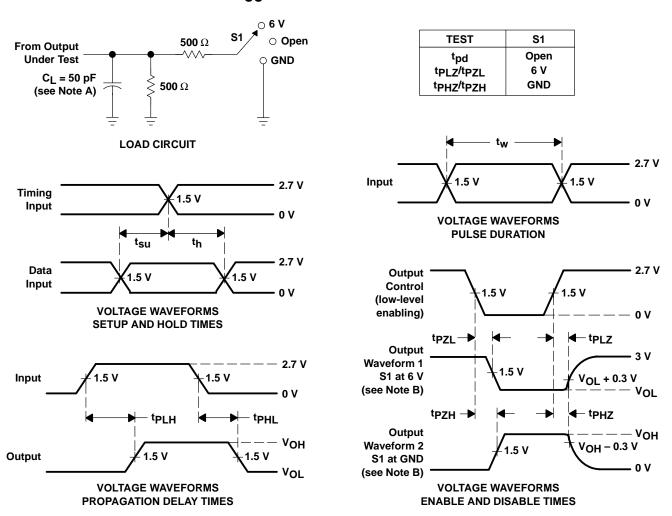
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_f≤2 ns, t_f≤2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzI and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16245 is designed asvnchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data

transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION
OE	DIR	OFERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

48 1 1 OE 1DIR L 47 🛮 1A1 1B1 📙 2 1B2 **∏** 3 46 1 1A2 GND L 4 45 GND 1B3 🛮 5 44 🛮 1A3 1B4 🛮 6 43 1 1A4 42 V_{CC} V_{CC} 4 7 41 🛮 1A5 1B5 🛮 8 1B6 🛮 9 40 1 1A6 GND 10 39 GND 1B7 ∏ 11 38 🛮 1A7 1B8 🛮 12 37 L 1A8 2B1 13 36 2A1 2B2 1 14 35 2A2 GND II 15 34 II GND 2B3 16 33 2A3 2B4 🛮 17 32 D 2A4 V_{CC} Ц 18 31 V_{CC} 2B5 [] 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 🛮 22

2B8 🛮 23

2DIR 🛮 24

27 2A7

26 2A8

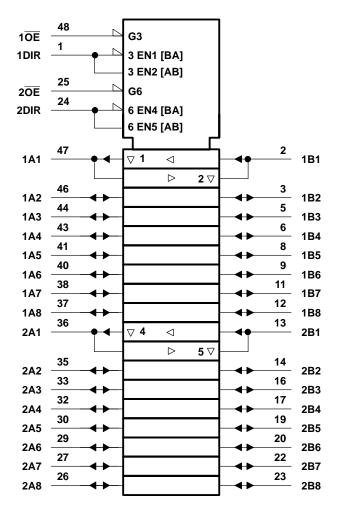
25 20E

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

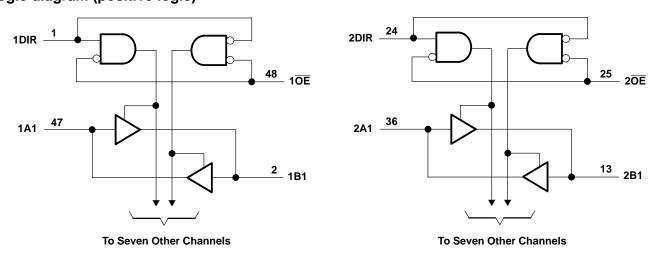
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCES015F - JULY 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output-voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	Lligh lovel output ourrest	V _{CC} = 2.3 V		-12	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Lave lavel autout august	V _{CC} = 2.3 V		12	A	
lol	Low-level output current	V _{CC} = 2.7 V	12		mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$		2.3 V	2				
Vон				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
\ \/~.		I _{OL} = 6 mA		2.3 V			0.4	V	
VOL		In. 12 mA		2.3 V			0.7	V	
	I _{OL} = 12 mA			2.7 V			0.4	1	
		I _{OL} = 24 mA	3 V			0.55			
II		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		V _I = 0.7 V		2.3 V	45				
I _{I(hold)}		V _I = 1.7 V		2.3 V	-4 5			μΑ	
` ´		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V		-	±500		
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
(INF		(IIVFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
Г	^t pd	A or B	B or A	¶	1	3.7		3.6	1	3	ns
	t _{en}	ŌE	A or B	¶	1	5.7		5.4	1	4.4	ns
Γ	^t dis	ŌĒ	A or B	¶	1	5.2		4.6	1	4.1	ns

This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

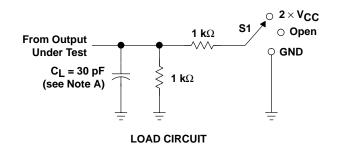
[§] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, T_A = 25° C

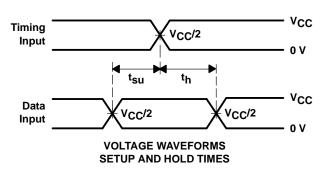
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
PARAMETER			TEST CONDITIONS	TYP	TYP	TYP	ONIT	
	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	22	29	nE.	
C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	5	pF	

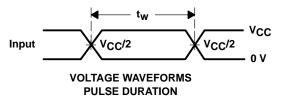
[†] This information was not available at the time of publication.

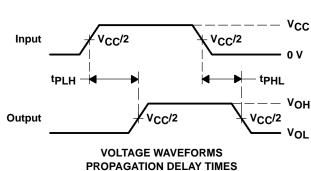
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

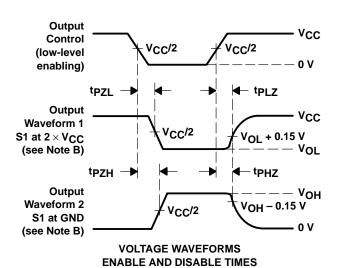










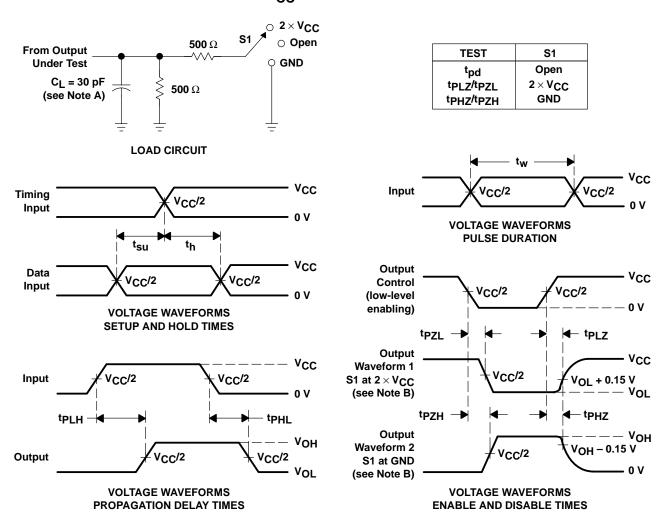


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f\leq$ 2 ns, $t_f\leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

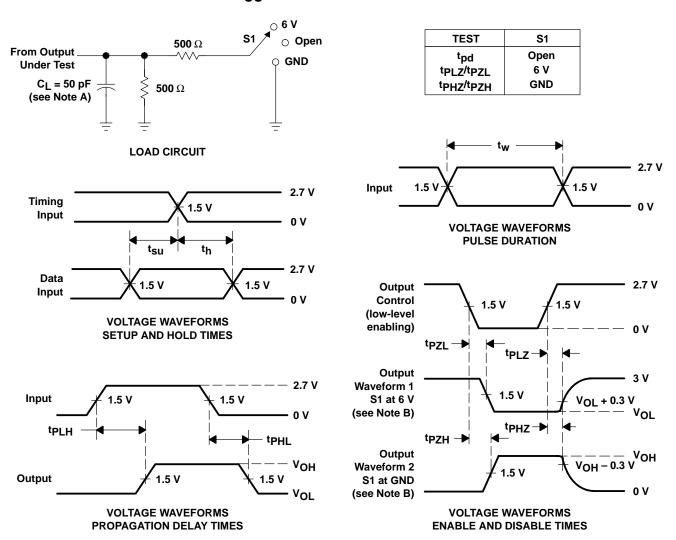


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

SCES046E - JULY 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit multiplexed D-type latch is designed for 1.65-V to 3.6-V_{CC} operation.

The SN74ALVCH16260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

OEA 56 OE2B LE1B [] 2 55 **∏** LEA2B 2B3 🛮 3 54 2B4 GND Π₄ 53 **∏** GND 2B2 **∏**5 52 **1** 2B5 2B1 **6** 51 2B6 V_{CC} 🛮 7 50 V_{CC} A1 🛮 8 49 2B7 A2 🛮 9 48 **∏** 2B8 A3 **∏** 10 47 **∏** 2B9 GND 11 46 GND A4 🛮 12 45 **∏**2B10 A5 ∏ 13 44 **∏** 2B11 A6 🛮 14 43 **1**2B12 A7 🛮 15 42 **1** 1B12 A8 🛮 16 41 **1** 1B11 A9 🛮 17 40 **1** 1B10 GND ∏18 39 **∏** GND A10 **1**19 38 **∏** 1B9 A11 20 37 🛮 1B8 A12 Π 21 36 **∏** 1B7 35 🛮 V_{CC} V_{CC} 422 1B1 **2**3 34 🛮 1B6 1B2 **1**24 33 **□** 1B5 GND ∏25 32 | GND 1B3 26 31 **1** 1B4 30 🛮 LEA1B LE2B **1**27 SEL [] 28 29 OE1B

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16260 is characterized for operation from -40°C to 85°C.

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Function Tables

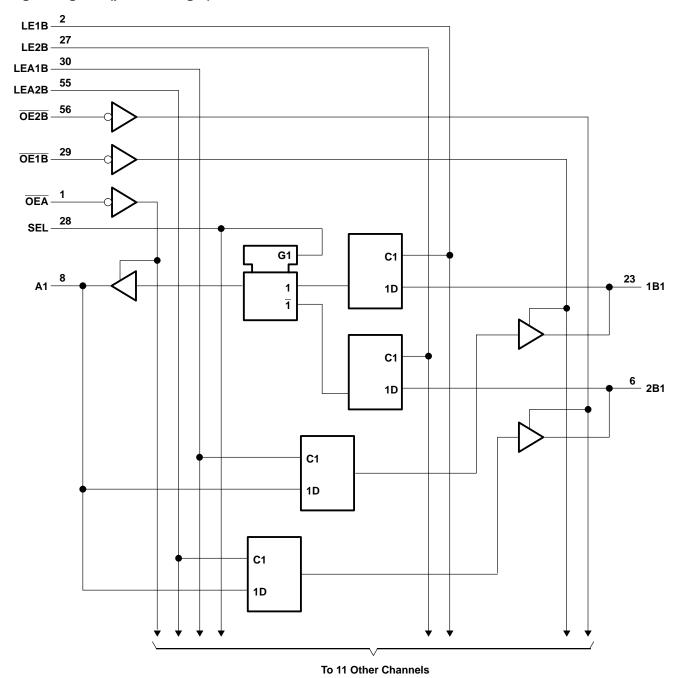
B TO A $(\overline{OEB} = H)$

	INPUTS							
1B	2B	SEL	LE1B	LE2B	OEA	Α		
Н	Х	Н	Н	Х	L	Н		
L	Χ	Н	Н	X	L	L		
Х	Χ	Н	L	X	L	A ₀		
Х	Н	L	X	Н	L	Н		
Х	L	L	X	Н	L	L		
Х	Χ	L	X	L	L	A ₀		
Х	Χ	Χ	Χ	Χ	Н	Z		

A TO B ($\overline{OEA} = H$)

		INPUTS			OUTI	PUTS
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	Н	Н	L	L	L	L
Н	Н	L	L	L	Н	2B ₀
L	Н	L	L	L	L	2B ₀
Н	L	Н	L	L	1B ₀	Н
L	L	Н	L	L	1B ₀	L
Х	L	L	L	L	1B ₀	2B ₀
Х	X	Χ	Н	Н	Z	Z
Х	Χ	Χ	L	Н	Active	Z
Х	Χ	X	Н	L	Z	Active
Х	X	Χ	L	L	Active	Active

logic diagram (positive logic)





SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		V _{CC} = 2.7 V to 3.6 V	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
1	I Park Javas Laudaud august d	V _{CC} = 2.3 V		-12	A	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Law laws and autom to a support	V _{CC} = 2.3 V		12	١.	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
	V _{CC} = 3 V			24	<u>l </u>	
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	VCC-0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V			0.45	
Vol	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V
VOL	I _{OL} = 12 mA	2.3 V			0.7	V
	IOL = 12 IIIA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
Ц	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i Control inputs	V _I = V _{CC} or GND	3.3 V		3.5		pF
C _{io} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		9		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	¶		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B	¶		1.4		1.1		1.1		ns
th	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B	¶		1.6		1.9		1.5		ns

This information was not available at the time of publication.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B	B or A	†	1	5.4		5.1	1.2	4.3	
^t pd	LE	A or B	†	1	5.6		5.2	1	4.4	ns
	SEL	Α	†	1	6.9		6.6	1.1	5.6	
t _{en}	ŌE	A or B	†	1	6.7		6.4	1	5.4	ns
^t dis	ŌĒ	A or B	†	1	5.7		5	1.3	4.6	ns

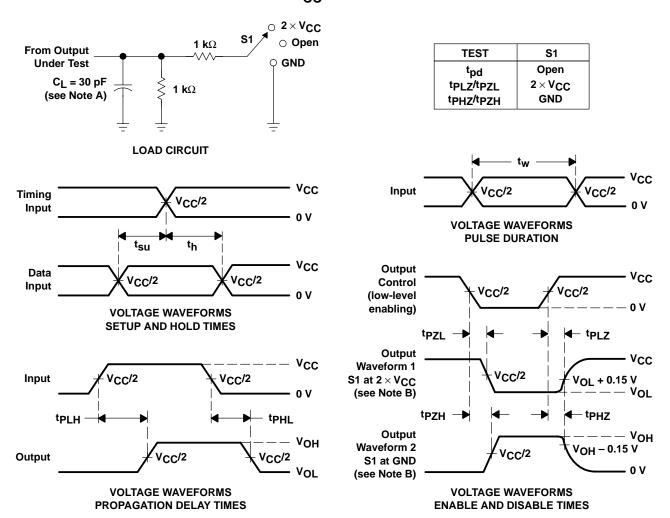
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	VCC = 3.3 V	UNIT
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	CINIT	
	Power dissipation	All outputs enabled	Cı = 50 pF. f = 10 MHz	†	37	41	pF
C _{pd}	capacitance	All outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	7	pr

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

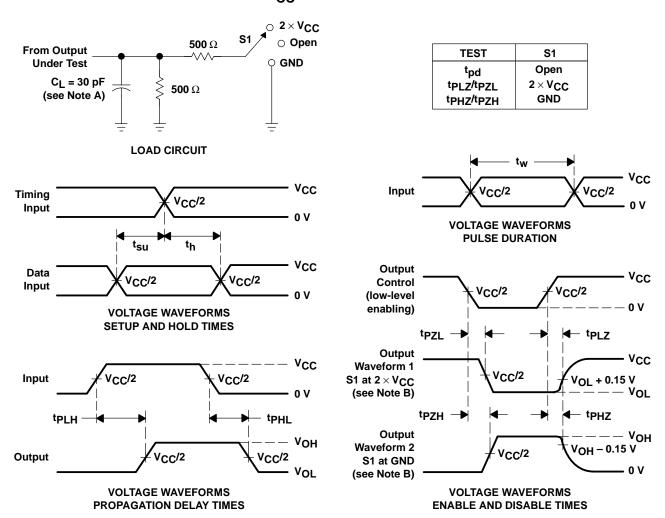


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES046E - JULY 1995 - REVISED FEBRUARY 1999

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

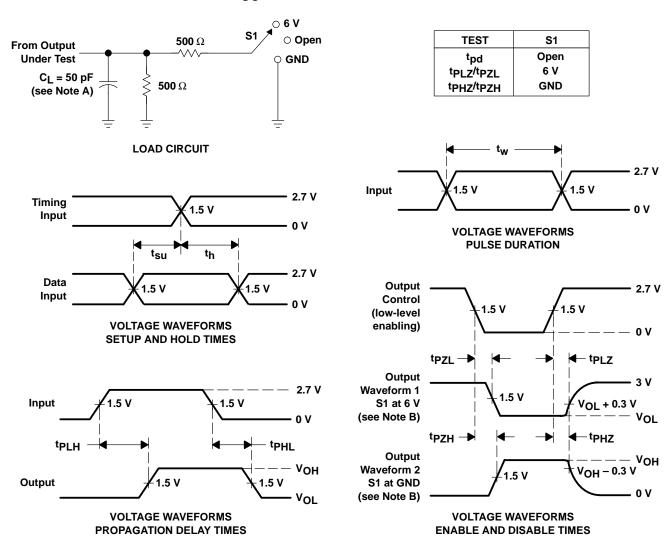


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES019H - JULY 1995 - REVISED FEBRUARY1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

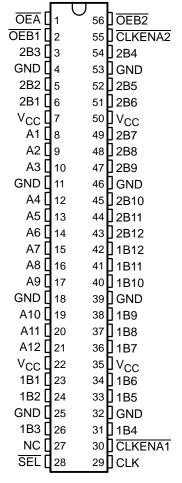
description

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage

DGG OR DL PACKAGE (TOP VIEW)



NC - No internal connection

register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, OEB2).

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16269 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

Function Tables

OUTPUT ENABLE

	INPUTS	OUTPUTS			
CLK	OEA	OEB	Α	1B, 2B	
1	Н	Н	Z	Z	
1	Н	L	Z	Active	
1	L	Н	Active	Z	
1	L	L	Active	Active	

A-TO-B STORAGE ($\overline{OEB} = L$)

	INPUTS			OUTI	PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Χ	Χ	1B ₀ †	2B ₀ †
L	Χ	\uparrow	L	L	Х
L	Χ	\uparrow	Н	Н	Х
Х	L	\uparrow	L	Х	L
Х	L	\uparrow	Н	Х	Н

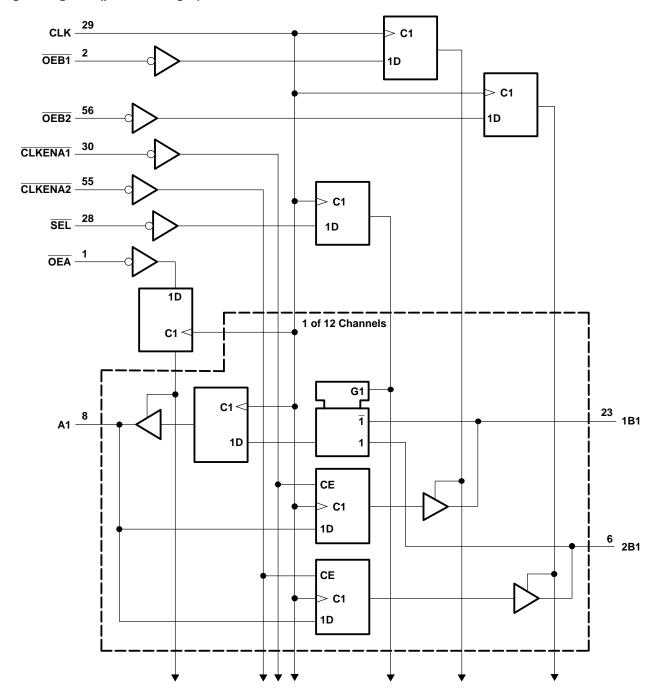
[†]Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

	INPL	JTS		OUTPUT
CLK	SEL	2B	Α	
Х	Н	Х	Х	A ₀ †
Х	L	Χ	X	A ₀ † A ₀ †
1	Н	L	Χ	L
1	Н	Н	Χ	Н
1	L	Χ	L	L
1	L	Χ	Н	Н

[†] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High level output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Lavidaval autout avenue	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDIT	IONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24 \text{ mA}$		3 V	2			
		$I_{OL} = 100 \mu A$		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
Vai		I _{OL} = 6 mA		2.3 V			0.4	V
VOL		lo 12 mA		2.3 V			0.7	V
		$I_{OL} = 12 \text{ mA}$		2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55		
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		$V_{I} = 0.58 \text{ V}$		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		$V_{I} = 0.7 V$		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	0	3.6 V			40	μΑ
∆lcc		One input at V _{CC} – 0.6 V, Other	r inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		9		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency			†		135		135		135	MHz
t _W	Pulse duration	on, CLK high or low	†		3.3		3.3		3.3		ns
	A data before CLK↑	†		2		2		1.7			
	Setup time	B data before CLK↑	†		2.2		2.1		1.8		
t _{su}		SEL before CLK↑	†		1.6		1.6		1.3		ns
		CLKENA1 or CLKENA2 before CLK↑	†		1		1.2		0.9		
		OE before CLK↑	†		1.5		1.6		1.3		
		A data after CLK↑	†		0.7		0.6		0.6		
		B data after CLK↑	†		0.7		0.6		0.6		
th	Hold time	SEL after CLK↑	†		1.1		0.7		0.7		ns
		CLKENA1 or CLKENA2 after CLK↑	t		1		8.0		1.1		
		OE after CLK↑	†		0.8		0.8		0.8		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER FROM		TO (OUTPUT)	v _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		135		135		135		MHz
	CLK	В		†	1	8.2		7.3	1	6.2	no
^t pd	CLK	А		†	1	6.4		5.8	1	5	ns
4	OL K	В		†	1	7.9		6.7	1	6.1	no
^t en	CLK	А		†	1	7.6		6.2	1	5.9	ns
4	CLIK	В		†	1	8.1		6.9	1	6.1	no
^t dis	CLK	А		†	1	7.5		6.8	1	5.6	ns

[†] This information was not available at the time of publication.

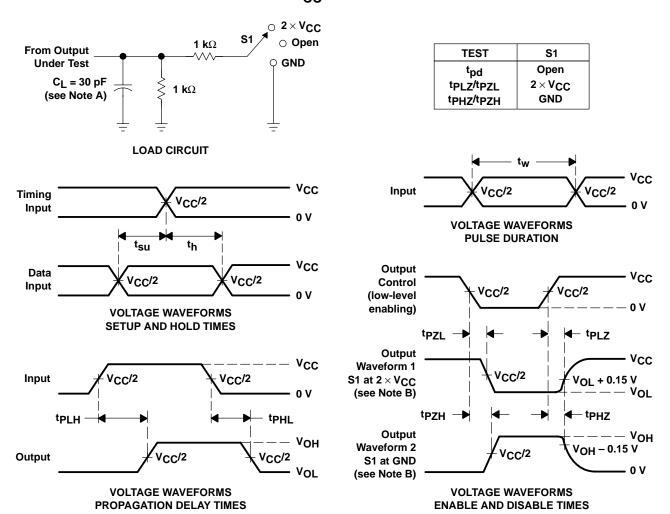
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C .	Power dissipation	All outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	87	120	5E
Cpd	capacitance per exchanger	All outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	80.5	118	pF

[†] This information was not available at the time of publication.



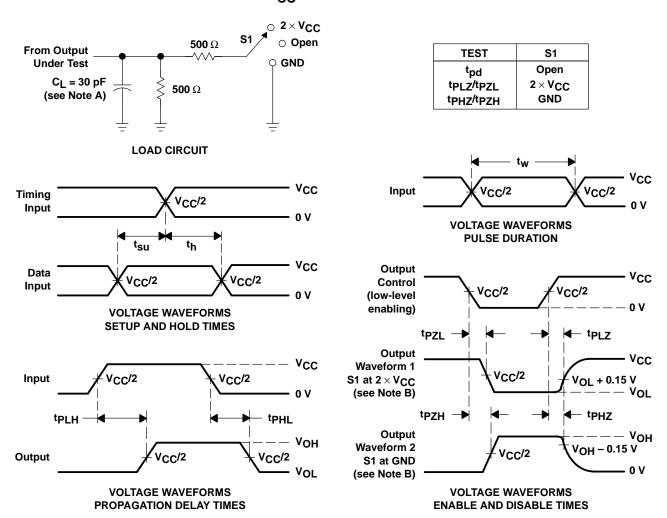
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

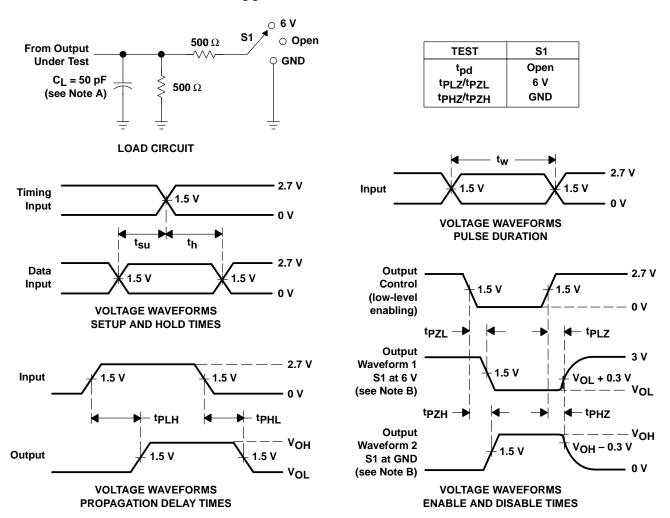


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

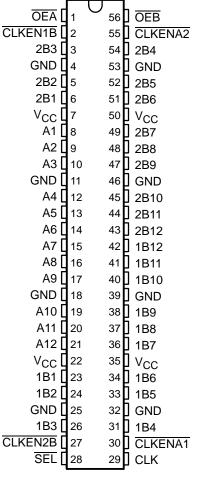
description

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate CLKEN inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path.

DGG OR DL PACKAGE (TOP VIEW)



Proper control of the CLKENA inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). The control terminals are registered to synchronize the bus-direction changes with CLK.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is characterized for operation from -40°C to 85°C.

ts TEXAS

Function Tables

OUTPUT ENABLE

	INPUTS	OUTPUTS		
CLK	OEA	OEB	Α	1B, 2B
1	Н	Н	Z	Z
1	Н	L	Z	Active
1	L	Н	Active	Z
1	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

	INPUTS					
CLKENA1	CLKENA2	CLK	Α	1B	2B	
L	Н	Χ	Χ	1B ₀ †	2B ₀ †	
L	Н	Χ	Χ	1B ₀ †	2B ₀ †	
L	L	\uparrow	L	L‡	L	
L	L	\uparrow	Н	н‡	Н	
Н	L	\uparrow	L	1B ₀ †	L	
Н	L	\uparrow	Н	1B ₀ †	Н	
Н	Н	Χ	Χ	1B ₀ †	2B ₀ †	

[†]Output level before the indicated steady-state input conditions were established

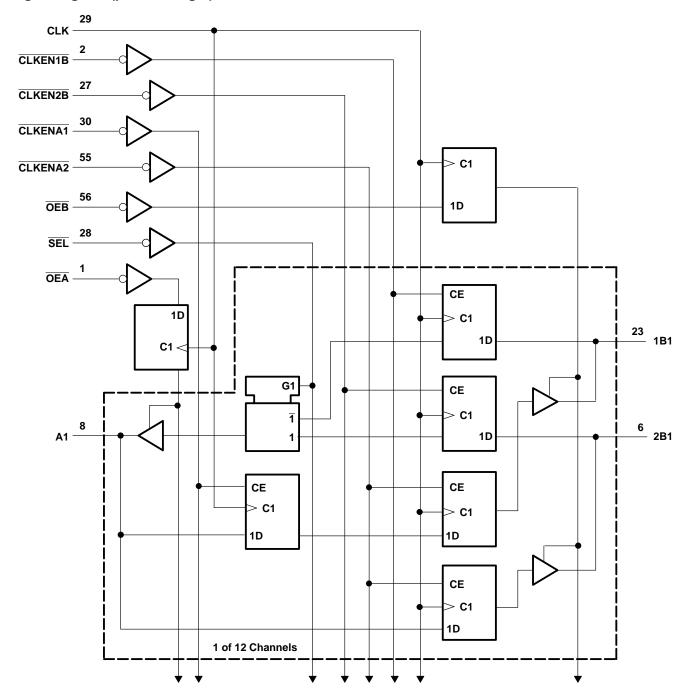
B-TO-A STORAGE ($\overline{OEA} = L$)

	ОИТРИТ					
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
Н	Х	Χ	Н	Χ	Х	A ₀ †
Х	Н	Χ	L	Χ	Χ	A ₀ †
L	Χ	\uparrow	Н	L	X	L
L	Χ	\uparrow	Н	Н	Χ	Н
Х	L	\uparrow	L	Χ	L	L
Х	L	\uparrow	L	X	Н	н

[†]Output level before the indicated steady-state input conditions were established

[‡]Two CLK edges are needed to propagate data.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	-0.5 V to V_{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to $V_{\mbox{\footnotesize CC}}$ + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{sta}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
۷o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
1	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Low lovel output ourrent	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24 \text{ mA}$		3 V	2			
		$I_{OL} = 100 \mu A$		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		loι – 12 mΛ		2.3 V			0.7	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC			Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF
C _{io}	A or B ports	VO = VCC or GND		3.3 V		9		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock freque	ency		†		150		150		150	MHz
t _W	Pulse durati	on, CLK high or low	†		3.3		3.3		3.3		ns
		A data before CLK↑	†		4.1		3.8		3.1		
	Setup time	B data before CLK↑	†		0.9		1.2		0.9		
t _{su}		CLKENA1 or CLKENA2 before CLK↑	†		3.5		3.2		2.7		ns
		CLKEN1B or CLKEN2B before CLK↑	†		3.4		3		2.6		
		OE data before CLK↑	†		4.4		3.9		3.2		
		A data after CLK↑	†		0		0		0.2		
		B data after CLK↑	†		1.4		1		1.7		
th	Hold time	CLKENA1 or CLKENA2 after CLK↑	†		0		0.1		0.3		ns
		CLKEN1B or CLKEN2B after CLK↑	t		0		0		0.6		
		OE after CLK↑	†		0		0		0.1		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		J ,									
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	0116	В		†	1.5	5.9		5.8	1.1	5.1	
t _{pd}	CLK	А		†	1.2	5.4		5.4	1	4.7	ns
·	SEL	А		†	1.4	6.2		6.4	1	5.5	
t _{en}	CLK	A or B		†	1.5	7		6.8	1	6	ns
t _{dis}	CLK	A or B		†	1.9	7.2		6.5	1.1	5.8	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

ſ	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC}		V _{CC} = 3.3 V	UNIT	
			TEOT GONDITIONS	TYP	TYP	TYP	ONT	
Γ	С .	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	87	120	pF
	C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	80.5	118	рΓ

[†] This information was not available at the time of publication.

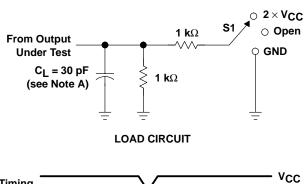


VCC

0 V

V_{CC}/2

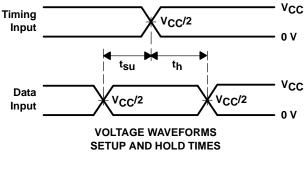
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

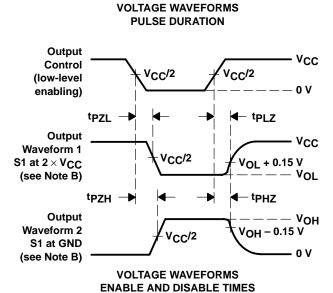


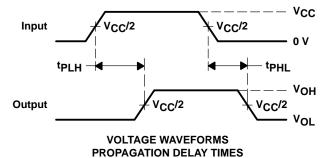
TEST	S 1
tpd	Open
tpLZ/tpZL	2 × V _{CC}
tpHZ/tpZH	GND

V_{CC}/2

Input



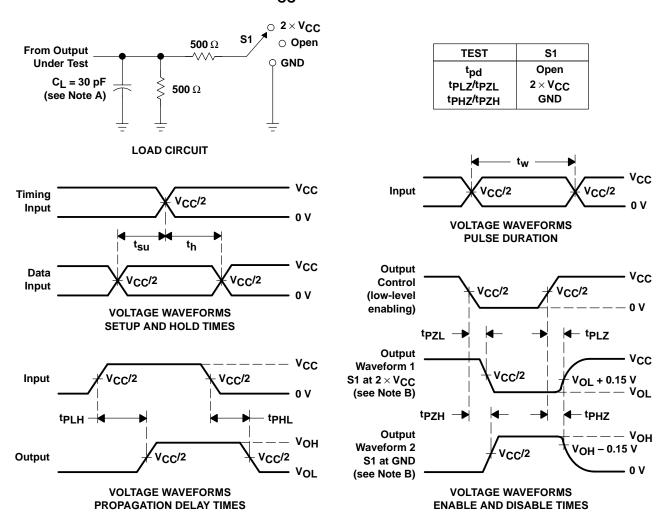




- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzl and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

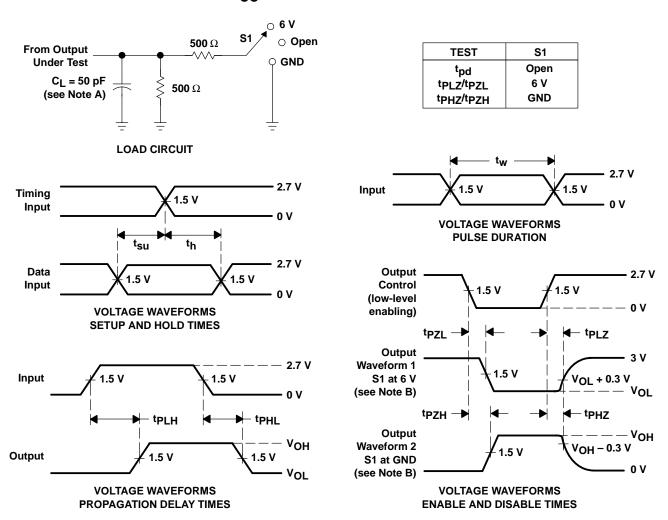


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES017E - JULY 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

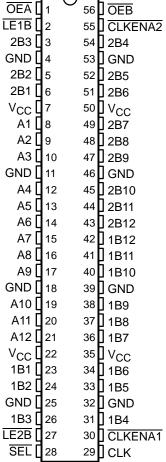
description

This 12-bit to 24-bit bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16271 is intended for applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

DGG OR DL PACKAGE (TOP VIEW)



Transparent latches in the B-to-A path allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{\text{LE}}$) inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$).

To ensure the high-impedance state during power up or power down, the output enables should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16271 is characterized for operation from -40°C to 85°C.

TEXAS
INSTRUMENTS

Function Tables

OUTPUT ENABLE

INP	UTS	OUTPUTS			
OEA	OEB	Α	1B, 2B		
Н	Н	Z	Z		
Н	L	Z	Active		
L	Н	Active	Z		
L	L	Active	Active		

A-TO-B STORAGE ($\overline{OEB} = L$)

	OUTPUTS				
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Χ	Χ	1B ₀ †	2B ₀ †
L	Χ	\uparrow	L	L	Х
L	Χ	\uparrow	Н	Н	Х
Х	L	\uparrow	L	Х	L
Х	L	\uparrow	Н	A ₀	Н

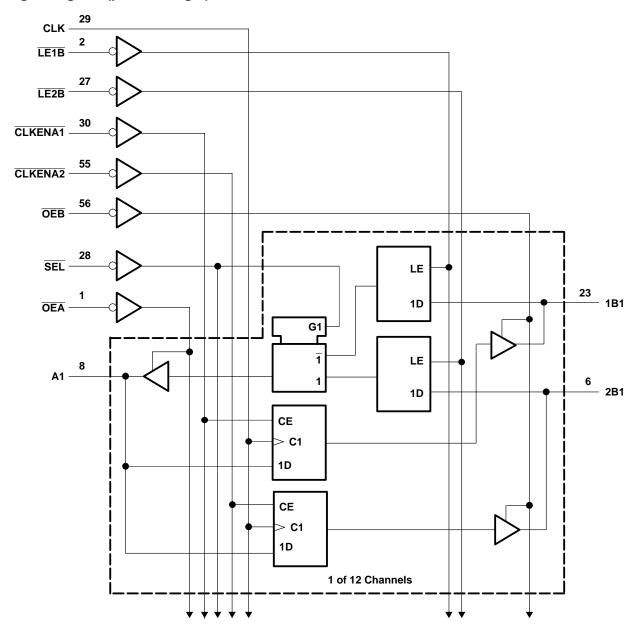
B-TO-A STORAGE ($\overline{OEA} = L$)

	INPU	OUTPUT		
LE	SEL	1B	2B	Α
Н	Х	Х	Х	A ₀ †
Н	Χ	Χ	Χ	A ₀ † A ₀ †
L	Н	L	Χ	L
L	Н	Н	X	Н
L	L	Χ	L	L
L	L	Χ	Н	Н

[†] Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	Vcc	V
۷o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
l .	Lligh lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-12	A
ІОН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
١	Law lavel output ourrent	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
Тд	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
Vol	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	\/
VOL	lo 12 mA	2.3 V			0.7	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔlCC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
C _i Control inputs	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF
C _{iO} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		9		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			¶		130		130		130	MHz
t _W	Pulse duration, CLK high	or low	¶		3.3		3.3		3.3		ns
		A before CLK↑	¶		2.6		2.1		1.7		
t _{su}	Setup time	B before LE	¶		1.7		1.5		1.3		ns
		CLKEN before CLK↑	¶		1.6		1.3		1		
		A after CLK↑	¶		0.6		0.6		0.7		
t _h	Hold time	B after LE	¶		0.9		0.9		1.1		ns
		CLKEN after CLK↑	¶		1		0.9		0.9		

This information was not available at the time of publication.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES017E - JULY 1995 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		130		130		130		MHz
	CLK	В		†	1	6.2		5	1	4.3	
	В			†	1	5.3		4.7	1.4	4	
^t pd	LE	Α		†	1	6		5.9	1.4	4.8	ns
	SEL			†	1.1	6.4		6.2	1.3	5.2	
^t en	OEB or OEA	B or A		†	1	6		6.1	1	5.1	ns
^t dis	OEB or OEA	B or A		†	1.4	5.4		4.6	1.7	4.2	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAIV	IETEK		TEST CONDITIONS	TYP	TYP TYP		UNIT
		Power dissipation A to B Outputs enabled Outputs disabled	Outputs enabled		†	92	105	
	Power dissipation		0 0 5 40 M I =	†	61	76		
Cpd	C _{pd} capacitance	D to A	Outputs enabled	$C_L = 0$, $f = 10 MHz$	†	39	43	pF
		B to A	Outputs disabled		†	11	13	

[†] This information was not available at the time of publication.



TEST

tpd

tPLZ/tPZL

tPHZ/tPZH

V_{CC}/2

VOLTAGE WAVEFORMS

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S1

Open

2×V_{CC}

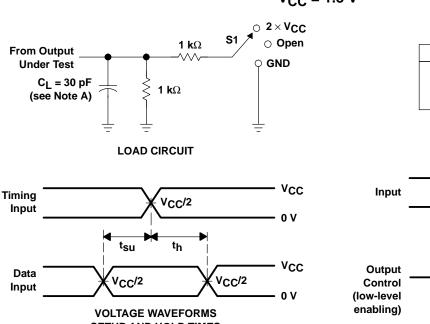
GND

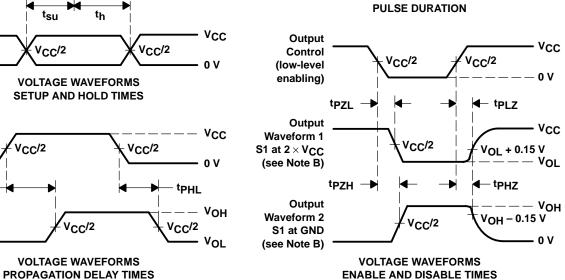
VCC

0 V

V_{CC}/2

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





NOTES: A. C_L includes probe and jig capacitance.

V_{CC}/2

Input

Output

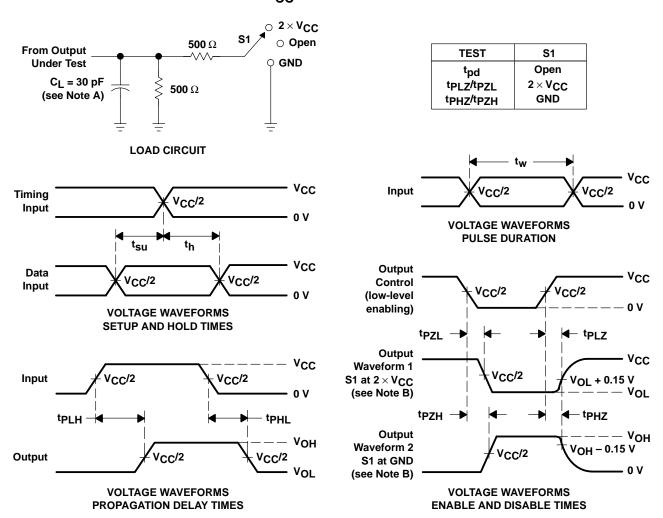
^tPLH

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpz and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



NOTES: A. C_L includes probe and jig capacitance.

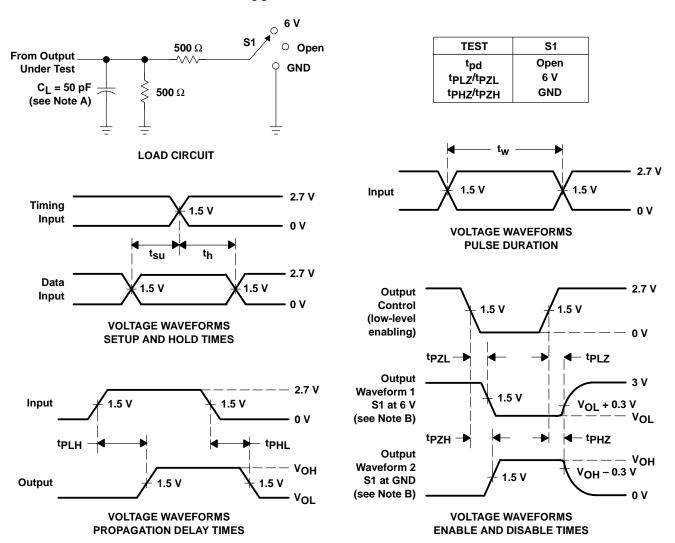
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

SCES057C - OCTOBER 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

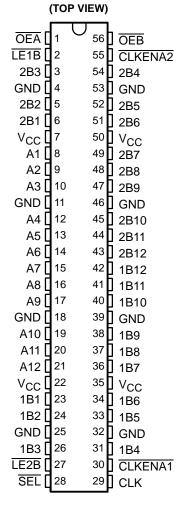
description

This 12-bit to 24-bit bus exchanger is designed for 1.65-V to 3.3-V V_{CC} operation.

The SN74ALVCH16272 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, when the CLKENA inputs are low. A two-stage pipeline is provided in each of the A-to-1B and A-to-2B paths to serve as a shallow write buffer.

Transparent latches are provided in the B-to-A path to allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16272 is characterized for operation from -40°C to 85°C.

Function Tables

OUTPUT ENABLE

INP	UTS	OUTPUTS			
OEA	OEB	Α	1B, 2B		
Н	Н	Z	Z		
Н	L	Z	Active		
L	Н	Active	Z		
L	L	Active	Active		

A-TO-B STORAGE (OEB = L)

	OUTI	PUTS			
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	Χ	\uparrow	L	L‡	X
L	Χ	\uparrow	Н	H‡	Х
Х	L	\uparrow	L	Х	L
Х	L	\uparrow	Н	A ₀	Н

[†]Output level before the indicated steady-state input conditions were established

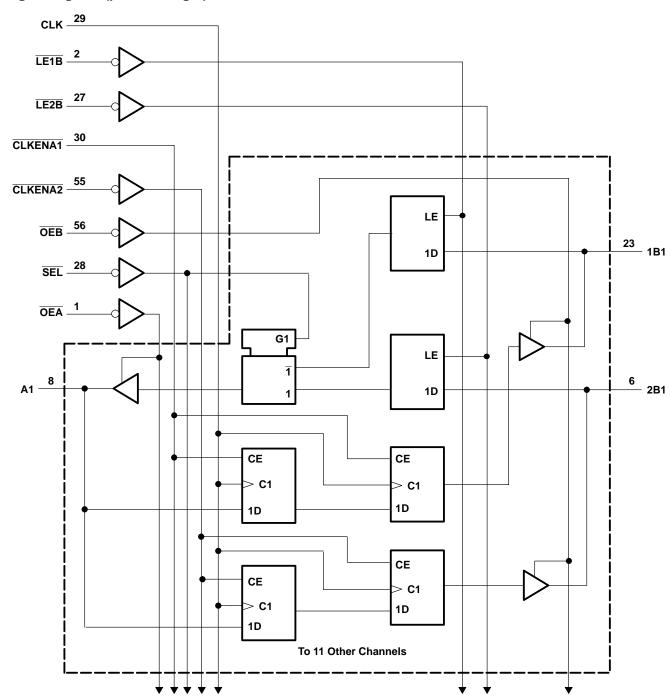
B-TO-A STORAGE (OEA = L)

		•						
	INPUTS							
LE	SEL	1B	2B	Α				
Н	Х	Χ	Х	A ₀ †				
Н	X	Χ	X	А _О † А _О †				
L	Н	L	X	L				
L	Н	Н	X	Н				
L	L	Χ	L	L				
L	L	Χ	Н	Н				

[†] Output level before the indicated steady-state input conditions were established

[‡]Two CLK edges are needed to propagate data.

logic diagram (positive logic)





SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES057C - OCTOBER 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{Stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
\vee_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ı	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
	High lovel output ourrent	$V_{CC} = 2.3 V$		-12	mA
ІОН	High-level output current	$V_{CC} = 2.7 V$		-12	IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Lour lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYPT MAX	UNIT	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7		V	
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V		0.2		
	$I_{OL} = 4 \text{ mA}$	1.65 V		0.45		
Vol	$I_{OL} = 6 \text{ mA}$	2.3 V		0.4	V	
VOL	lo 12 mA	2.3 V		0.7	V	
	I _{OL} = 12 mA	2.7 V		0.4		
	$I_{OL} = 24 \text{ mA}$	3 V		0.55		
II	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ	
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45		μΑ	
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500		
loz§	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ	
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ	
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	μΑ	
C _i Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF	
Cio A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency										MHz
t _W	Pulse duration, CLK high or low										ns
		A before CLK↑									
t _{su}	Setup time	B before LE									ns
		CLKEN before CLK↑									
	A after CLK↑										
t _h	Hold time	B after LE									ns
		CLKEN after CLK↑									

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\$}$ For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES057C - OCTOBER 1995 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM	FROM TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
	CLK	В									
	В										
^t pd	LE	Α									ns
	SEL										
t _{en}	OEB or OEA	B or A									ns
^t dis	OEB or OEA	B or A									ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	A to D		Outputs enabled					
	Power dissipation	capacitance Outputs enabled C _L = 0, f = 10 MI		C. O f 10 MHz				pF
C _{pd}	oupaonarioc			$C_{L} = 0, I = 10 \text{ M/Hz}$				ρг
	B to A		Outputs disabled					

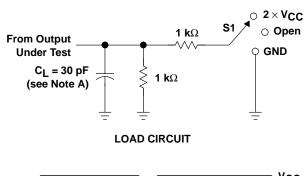


VCC

0 V

V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

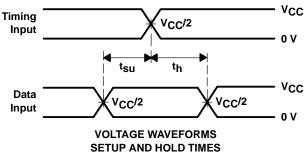


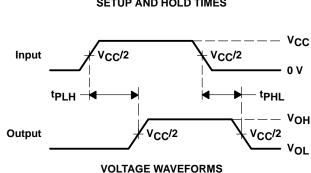
TEST	S 1
t _{pd} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 × V _{CC} GND

V_{CC}/2

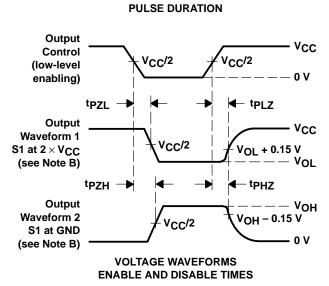
VOLTAGE WAVEFORMS

Input





PROPAGATION DELAY TIMES

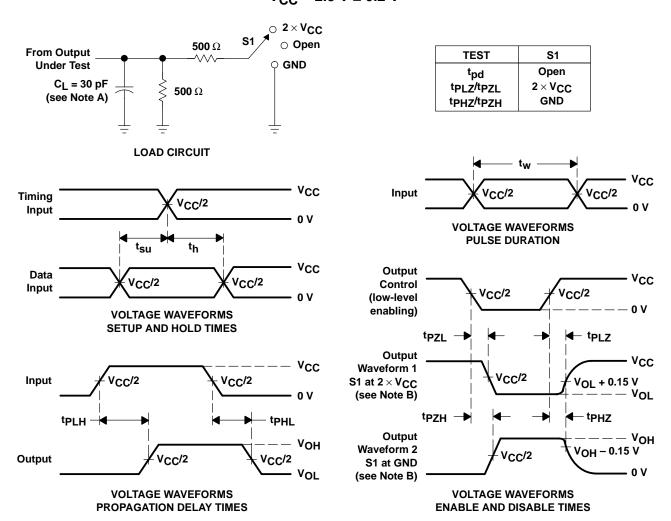


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

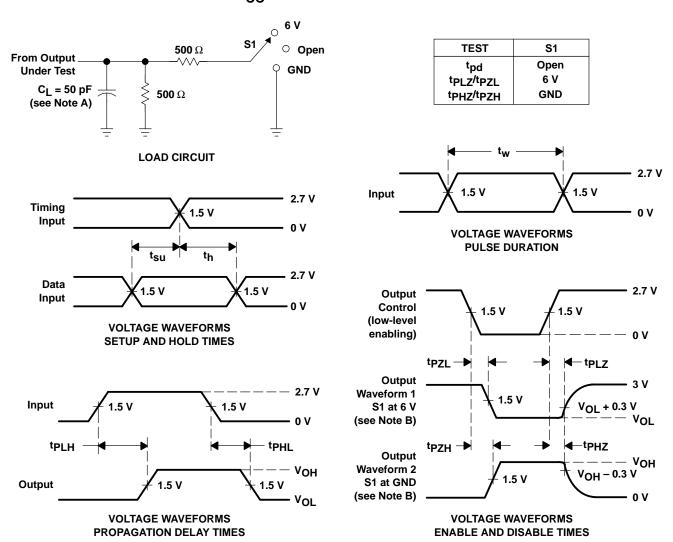


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveform

SN74ALVCH16280 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPU

DBB PACKAGE

(TOP VIEW)

SCES033A - JULY 1995 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Packaged in Thin Shrink Small-Outline **Package**

description

This 16-bit to 32-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation. This device is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the A and B ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, SEL selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, and a single storage register in the 2B path. Data flow is controlled by the active-low output enable (\overline{OE}) and the direction-control (DIR) input. DIR is registered to synchronize the bus direction changes with the clock.

Two mask bits are provided for both data bytes. The D outputs are controlled by the active-low OE.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16280 is characterized for operation from -40°C to 85°C.

	<u>`</u>		_	1
V_{CC}	1	\cup	80]v _{cc}
GND	2			GND
2B7	3			1B8
1B7	4		77	
2B6	5		76	1B9
GND	6		75	GND
1B6	7		74	2B9
2B5	8		73] 1B10
1B5	9		72	2B10
V_{CC}	10		71] v _{cc}
2B4	11		70] 1B11
1B4	12		69	2B11
2B3	13		68] 1B12
1B3	14		67	2B12
GND	15		66	GND
2B2	16		65] 1B13
1B2	17		64	2B13
2B1	18		63] 1B14
1B1	19		62	2B14
V_{CC}	20		61	Vcc
GND	21		60	GND
2D2	22		59	
1D2	23		58	2B15
2D1	24		57] 1B16
1D1	25		56	2B16
V_{CC}	26		55	Vcc
C1	27			A16
C2	28		53	A15
A1	29		52	A14
GND	30		51	GND
A2	31		50	A13
А3	32		49	A12
A4	33		48	A11
V_{CC}	34		47	Vcc
A5	35		46	A10
A6	36		45] A9
A7	37		44	8A [
GND	38		43] GND
CLK	39		42	OE
SEL	40		41	DIR
	_			•

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Function Tables

OUTPUT ENABLE

	INPUTS		OUTPUTS		
CLK	OE	DIR	Α	1B, 2B	1D, 2D
1	Н	Х	Z	Z	Z
1	L	Н	Z	Active	Active
↑	L	L	Active	Z	Active

A-TO-B STORAGE (OE = L, DIR = H)

	INPUTS	OUTI	PUTS	
SEL	CLK	Α	1B	2B
Н	Х	Х	1B ₀ †	2B ₀ †
L	\uparrow	L	L‡	L
L	\uparrow	Н	н‡	Н

[†]Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE $(\overline{OE} = L, DIR = L)$

	INP	OUTPUT		
CLK	SEL	1B	2B	Α
1	Н	Χ	L	L§
1	Н	Χ	Н	н§
1	L	L	X	L
1	L	Н	X	Н

[§] Two clock edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

C-TO-D STORAGE (OE = L)

	INPUTS	OUTI	PUTS	
SEL	CLK	Α	1B	2B
Н	Х	Х	1D ₀ †	2D ₀ †
L	\uparrow	L	L‡	L
L	\uparrow	Н	н‡	Н

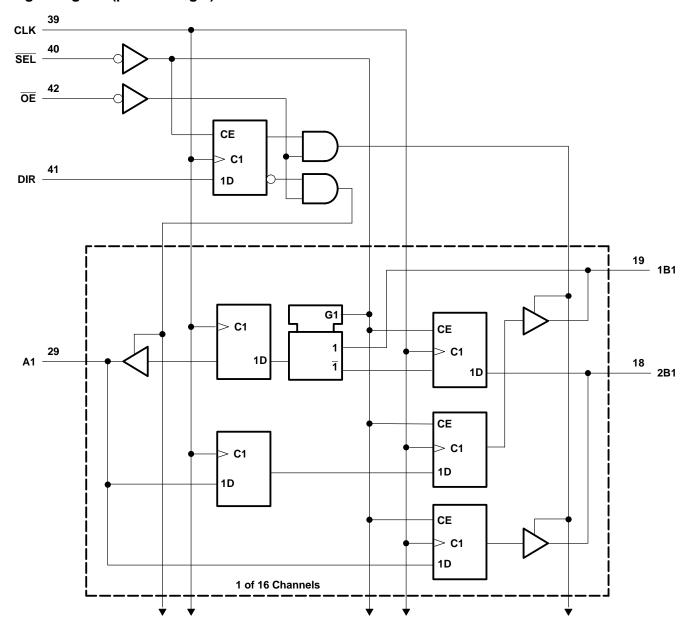
[†]Output level before the indicated steady-state input conditions were established



[‡] Two CLK edges are needed to propagate the data.

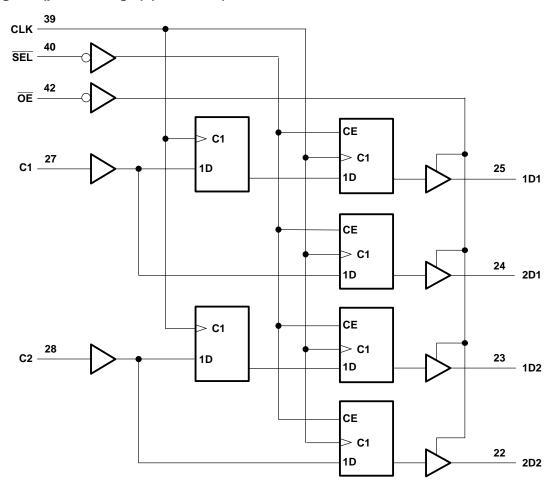
[‡] Two CLK edges are needed to propagate the data.

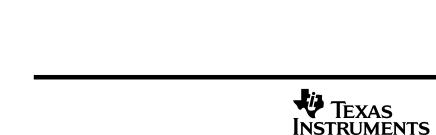
logic diagram (positive logic)



PRODUCT PREVIEW

logic diagram (positive logic) (mask bits)





SN74ALVCH16280 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
\vee_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lou	High level output ourrant	$V_{CC} = 2.3 \text{ V}$		-12	mA	
IOH	righ-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA	
	High-level input voltage $ \begin{array}{c} V_{CC} = 1.65 \ V \ to \ 1.9t \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 1.65 \ V \ to \ 1.9t \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 2.3 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.3 \ V \\ V_{CC} = 2.7 \ V \\ V_{CC} = 3 \ V \\ V_{CC} = 2.7 \ V \\ V_{CC} $	V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA	
	je zow iovorodiput odnom	V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	
T _A	Operating free-air temperature				35	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN74ALVCH16280 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	V _{CC} -0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
1/		I _{OL} = 6 mA	2.3 V			0.4	V
VOL		10.00	2.3 V		-	0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
lį		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V [‡]	3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μА
Δlcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V				pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\colored}$ For I/O ports, the parameter IOZ includes the input leakage current.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency										MHz
t _W	Pulse duration, CLK high	or low									ns
	t _{SU} Setup time	A data before CLK↑									- ns
		B data before CLK↑									
^ι su		DIR before CLK↑									
		SEL before CLK↑									
		A data after CLK↑									
	l lald than a	B data after CLK↑									ns
^t h	Hold time	DIR after CLK↑									
		SEL after CLK↑									

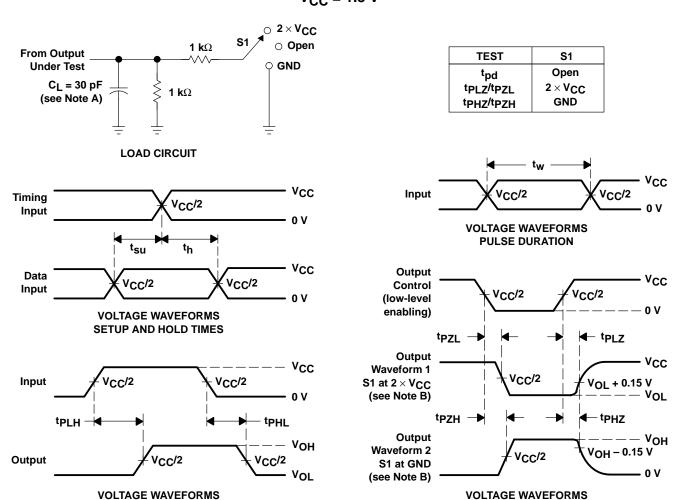
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TO V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
t _{od} CLK	Α									ns	
^t pd	CLK	В									115
		Α									ns
t _{en}	ŌĒ	В									
4	ŌĒ	Α									no
^t dis	OE	В									ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	LIMIT
	FARAIVIETER		TEST CONDITIONS	TYP	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC} = 3.3 V UN TYP TYP TYP pf	UNIT	
			Cı = 0. f = 10 MHz				s.E
Cpd	Power dissipation capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$				рΓ

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

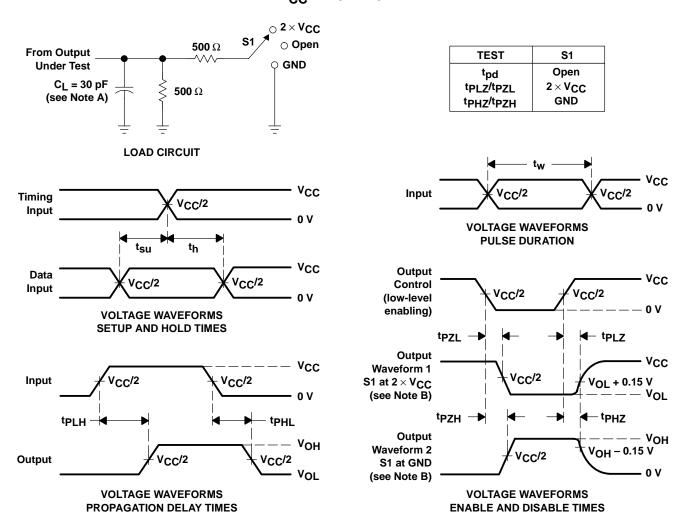
Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



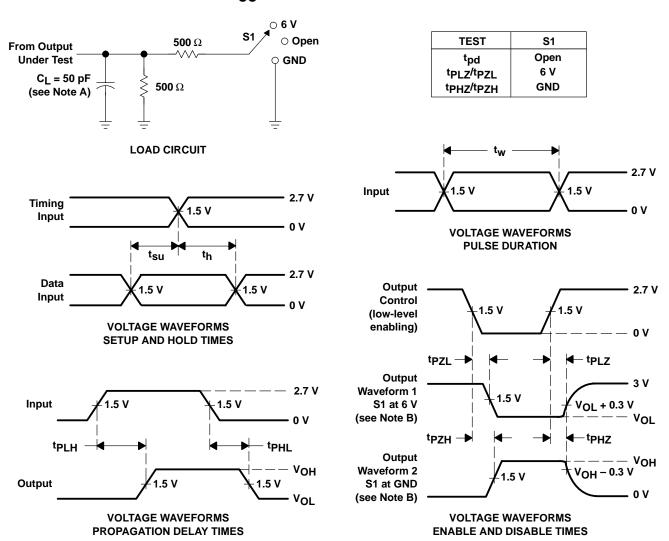
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SCES036C - JULY 1995 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown**
- Packaged in Thin Very Small-Outline **Package**

description

The SN74ALVCH16282 is an 18-bit to 36-bit registered bus exchanger designed for 1.65-V to 3.6-V V_{CC} operation.

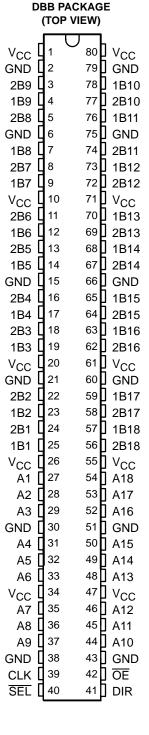
This part is intended for use in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select (SEL) input selects 1B or 2B data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable (\overline{OE}) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16282 is characterized for operation from -40°C to 85°C.



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Function Tables

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

INPUTS			OUTPUTS		
SEL	CLK	Α	1B	2B	
Н	Х	Х	1B ₀ †	2B ₀ †	
L	\uparrow	L	L‡	Х	
L	\uparrow	Н	н‡	Х	

[†]Output level before indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

	INPL	OUTPUT		
CLK	SEL	1B	2B	Α
1	Н	Χ	L	L§
↑	Н	Χ	Н	н§
↑	L	L	X	L
↑	L	Н	X	н

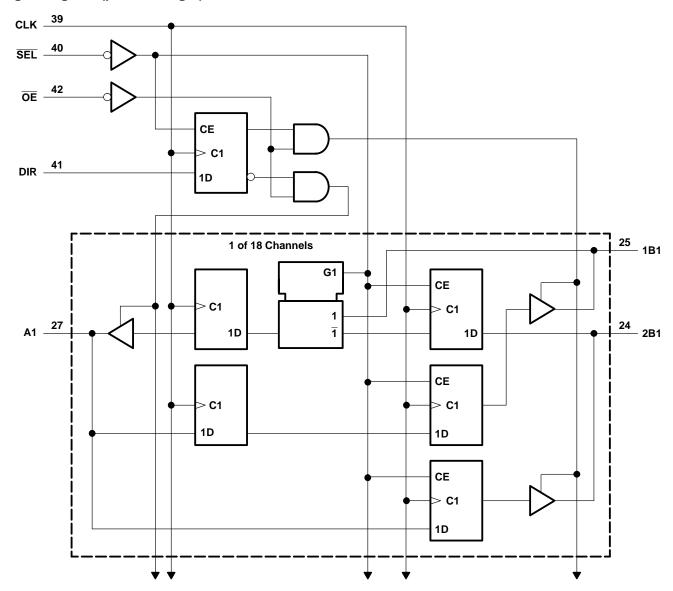
[§] Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

	INPUTS			OUTPUTS			
CLK	OE	DIR	Α	1B, 2B			
1	Н	Х	Z	Z			
1	L	L	Z	Active			
↑	L	Н	Active	Z			

[‡] Two CLK edges are needed to propagate the data.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.65 3.6 V 0.65 × V _{CC} 1.7 2	$0.35 \times V_{CC}$	
\vee_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
$V_{CC} = 2.7 \text{ V}$ $V_{I} \qquad \text{Input voltage}$ $V_{O} \qquad \text{Output voltage}$	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
la	High lovel output ourront	V _{CC} = 2.3 V		-12	mA
ЮН	High-level output current	V _{CC} = 2.7 V		-12	IIIA
		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-24		
		V _{CC} = 1.65 V		4	
10.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
IOL	Low-level output current	V _{CC} = 2.7 V		12	
	OL Low-level output current	V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP† I	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24 \text{ mA}$		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	1/
VOL		loι – 12 mΔ		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		1.65 V to 3.6 V V _{CC} -0.2 1.65 V 1.2 2.3 V 2 2.3 V 2 2.7 V 2.2 3 V 2.4 3 V 2 1.65 V to 3.6 V 0.45 2.3 V 0.4 2.3 V 0.4 2.3 V 0.7 2.7 V 0.4 3 V 0.55 3.6 V ±5 μΑ 1.65 V 2.3 V 45 2.3 V 45 2.3 V 45 2.3 V 45 3 V 75 3 V 75 3 V 75 3 C 3.6 V ±500 3.6 V ±500 3.6 V 40 μΑ				
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V		:	±500	
I _{OZ} §		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	ock Clock frequency			†		150		150		150	MHz
t _W	Pulse duration, CLK high or low		†		3.3		3.3		3.3		ns
	Setup time	A data before CLK↑	†		2.4		2.3		2		ns
t _{su}		B data before CLK↑	†		2.2		2.2		1.8		
		DIR before CLK↑	†		2.2		2.1		1.7		
		SEL before CLK↑	†		2		2		1.8		
^t h	Hold time	A data after CLK↑	†		0.5		0.5		0.7		ns
		B data after CLK↑	†		0.5		0.5		0.6		
		DIR after CLK↑	†		0.5		0.5		0.5		
		SEL after CLK↑	†		0.7		0.7		0.8		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	CLK	А		†	1	6.1		5.5	1.4	5	ns
^t pd		В		†	1.2	6.3		5.7	1.6	5.3	115
+	ŌĒ	Α		†	1.3	6.9		6.3	1.2	5.7	nc
^t en		В		†	2.3	8.7		8.1	2.3	7.4	ns
+	ŌĒ	А		†	1.5	7		5.6	1.8	5.7	20
^t dis		В		†	2.1	7.9		6.4	2.3	6.4	ns

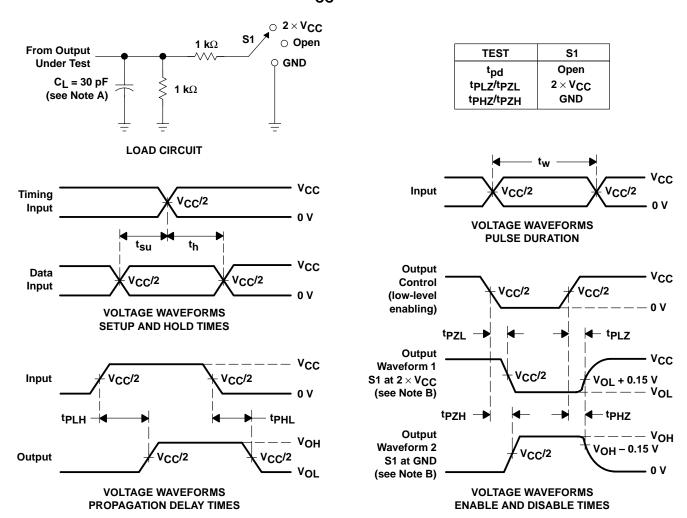
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAMETER		TEST CONDITIONS	TYP	TYP	TYP TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	Cı = 0. f = 10 MHz	†	282	310	pF
		Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	208	228	þг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

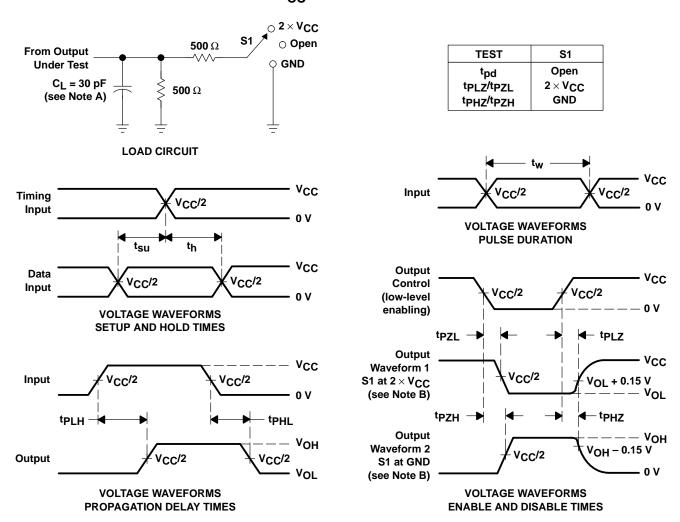


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



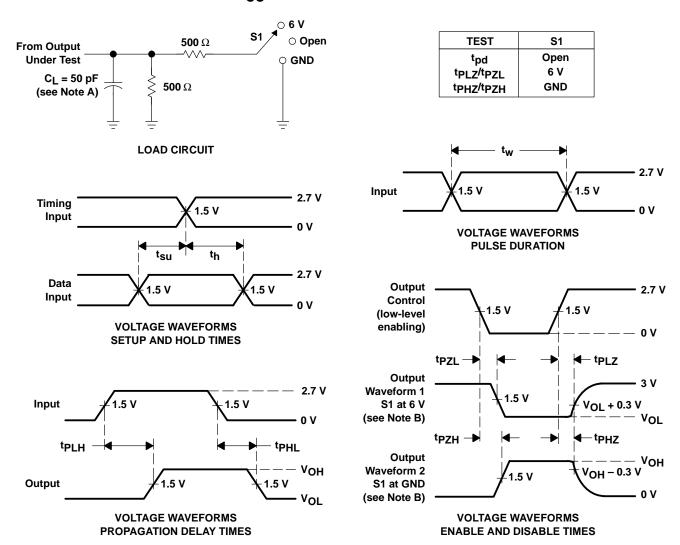
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

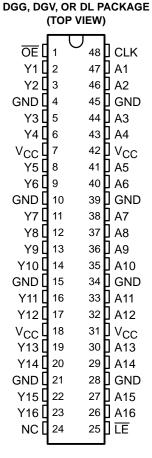
Figure 3. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Ideal for Use in PC100 Register DIMM
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.



NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

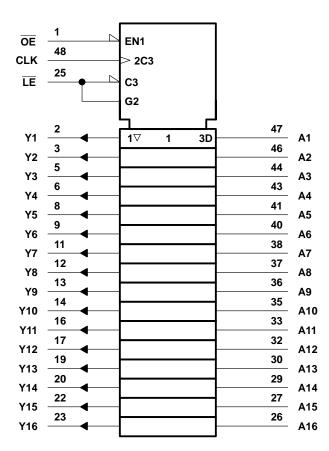
The SN74ALVC16334 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INF	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Χ	Z
L	L	Χ	L	L
L	L	X	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

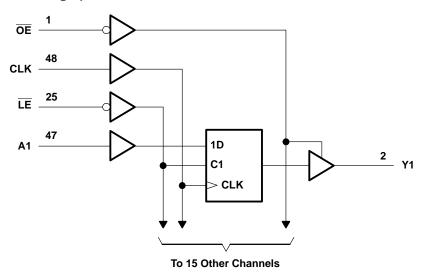
logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
$V_{IL} \text{Low-level input voltage} \qquad \begin{array}{c} V_{CC} = 1.65 \text{ V to } 1.95 \text{ V} \\ \hline V_{CC} = 2.3 \text{ V to } 2.7 \text{ V} \\ \hline V_{CC} = 2.7 \text{ V to } 3.6 \text{ V} \\ \hline \end{array}$		$0.35 \times V_{CC}$				
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
1	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ЮН	nigh-level output current	$V_{CC} = 2.7 V$		-12	IIIA	
		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-24			
		V _{CC} = 1.65 V		4		
la.	Low-level output current	V _{CC} = 2.3 V		12	mA	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	IIIA	
		V _{CC} = 3 V		24]	
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER	TEST CO	ONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
	Voн	I _{OH} = -6 mA	OH = -6 mA						
Vон								V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
VOH $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OL} = 100 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 6 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	I _{OH} = -24 mA		3 V	2					
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45			
\/oı	V _{OL}	I _{OL} = 6 mA		2.3 V			0.4	V	
VOL		loι = 12 mΛ		2.3 V			0.7		
		IOL = 12 IIIA		2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55			
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V	5			pF	
	Data inputs	AL = ACC OLGIAD		3.3 v		5.5		PΓ	
Со	Outputs	$V_O = V_{CC}$ or GND	·	3.3 V		7.5	·	pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	CC = 1.8 V VCC = 2.5 V ± 0.2 V		2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	Dulas duration	Ise duration		‡		3.3		3.3		3.3		ns
t _W	Puise duration			‡		3.3		3.3		3.3		115
		Data before CLK↑		‡		1.4		1.7		1.5		
t _{su}	Setup time		CLK high	‡		1.2		1.6		1.3		ns
		Data before LE ↑	CLK low	‡		1.4		1.5		1.2		
		Data after CLK↑		‡		0.9		0.9		0.9		
th	Hold time	Data after <u>LE</u> ↑	CLK high or low	‡		1.1	·	1.1		1.1		ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	3.7		3.6	1.1	3.3	
t _{pd}	LE	Y		†	1	4.8		5	1.3	4.4	ns
'	CLK			†	1	4.4		4.5	1	4.1	
t _{en}	ŌĒ	Y		†	1	5.4		5.4	1.1	4.6	ns
^t dis	ŌĒ	Y		†	1	4.1		4.5	1.7	4.4	ns

[†]This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	UNIT	
	(INFOT)	(001F01)	MIN	MAX	
	А	Y	1.2	3.2	ns
^t pd	CLK	Υ	1.1	4	ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
	PARAIVIETER		1E31 CONDITIONS	TYP	TYP	TYP	ONII	
<u> </u>	Power dissipation	Outputs enabled	$C_1 = 0$, $f = 10 \text{ MHz}$	†	31	36	nE.	
Cpd	capacitance	Outputs disabled	C[= 0,	†	7	11	pF	

[†] This information was not available at the time of publication.

S1

Open

2×VCC

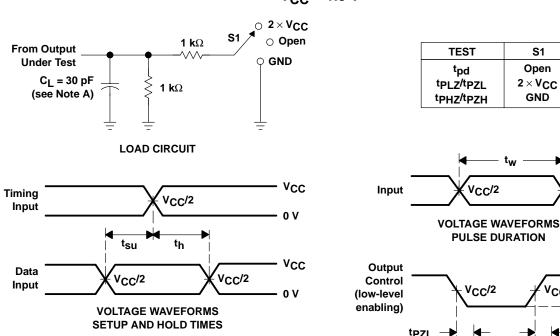
GND

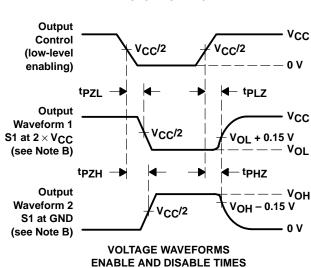
VCC

0 V

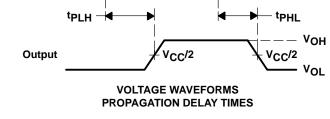
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





V_{CC}/2



NOTES: A. C_L includes probe and jig capacitance.

V_{CC}/2

Input

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

VCC

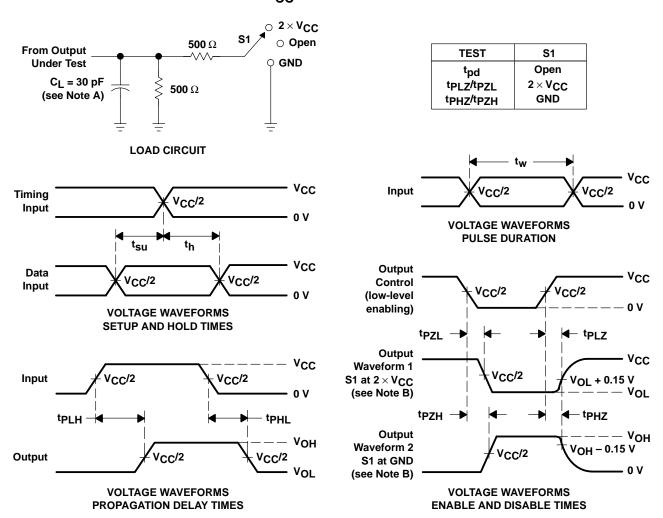
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.

V_{CC}/2

- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



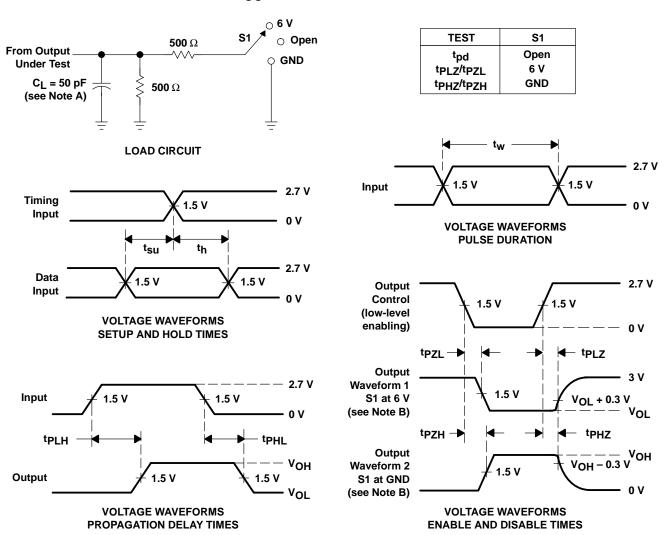
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

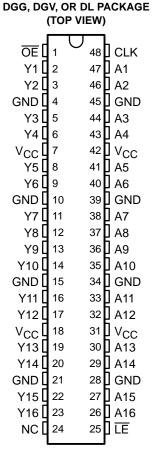
SCES090H - OCTOBER 1996 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.



NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

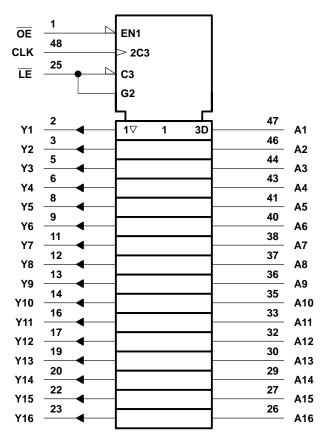
The SN74ALVCH16334 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Х	Z
L	L	Χ	L	L
L	L	X	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

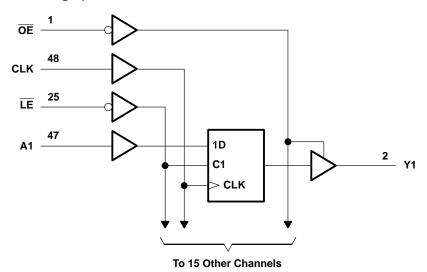
logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DC	GG package 89°C/W
DC	GV package 93°C/W
DL	_ package
Storage temperature range, T _{stg}	—65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
$V_{IL} \text{Low-level input voltage} \qquad \begin{array}{c} V_{CC} = 1.65 \text{ V to } 1.95 \text{ V} \\ \hline V_{CC} = 2.3 \text{ V to } 2.7 \text{ V} \\ \hline V_{CC} = 2.7 \text{ V to } 3.6 \text{ V} \\ \hline \end{array}$		$0.35 \times V_{CC}$				
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
1	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ЮН	nigh-level output current	$V_{CC} = 2.7 V$		-12	IIIA	
		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-24			
		V _{CC} = 1.65 V		4		
la.	Low-level output current	V _{CC} = 2.3 V		12	mA	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	IIIA	
		V _{CC} = 3 V		24]	
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST Co	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$	2.3 V	2					
Vон				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45		
Vai		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	W	
VOL	lo. – 12 mA		2.3 V			0.7	V		
		I_{OL} = 12 mA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			10.2 0.45 0.4 0.7 0.4 0.55 ±5 10 40 750		
lį		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		V _I = 0.7 V		2.3 V	45				
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ	
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V	1.2 2 1.7 2.2 2.4 2 6 V 0.2 0.45 0.4 0.7 0.4 0.55 ±5 μA 25 -25 45 -45 -45 75 -75 ±500 ±10 μA 40 μA				
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
С	ontrol inputs	Vi – Voe er CND		0.01/		5.5		nE	
C _i D	ata inputs	$V_I = V_{CC}$ or GND		3.3 V		6		þΓ	
C _o O	utputs	$V_O = V_{CC}$ or GND		3.3 V		8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				†		150		150		150	MHz
t Dulas duration		Pulse duration		†		3.3		3.3		3.3		ns
t _W	Puise duration	CLK high or low		†		3.3		3.3		3.3		115
		Data before CLK↑		†		1.4		1.7		1.5		
t _{su}	Setup time	Data before LF↑	CLK high	†		1.2		1.6		1.3		ns
			CLK low	†		1.4		1.5		1.2		
		Data after CLK↑		†		0.9		0.8		0.9		
th	Hold time	Data after LE ↑	CLK high or low	t		1.2		1.1		1.1		ns

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(1147-01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	3.7		3.6	1.1	3.3	
t _{pd}	LE	Y		†	1	4.8		5	1.3	4.4	ns
·	CLK			†	1	4.4		4.5	1	4.1	
^t en	ŌĒ	Y		†	1	5.4		5.4	1.1	4.6	ns
^t dis	ŌĒ	Y		†	1	4.1		4.5	1.7	4.4	ns

[†] This information was not available at the time of publication.

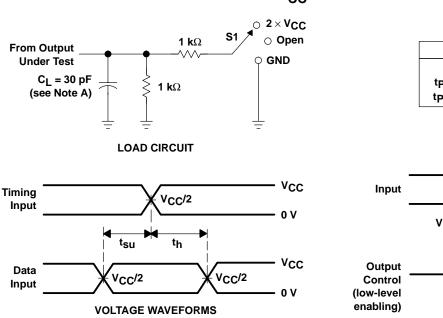
operating characteristics, T_A = 25°C

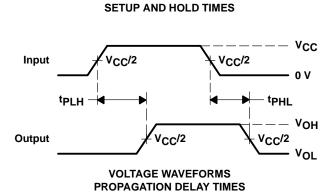
	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
	FARAMETER	1E31 CONDITIONS	TYP	TYP	TYP	ONIT		
<u> </u>	Power dissipation	Outputs enabled	$C_1 = 0$, $f = 10 \text{ MHz}$	†	32	37	pF	
Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	7	11	рг	

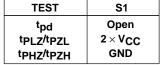
[†] This information was not available at the time of publication.

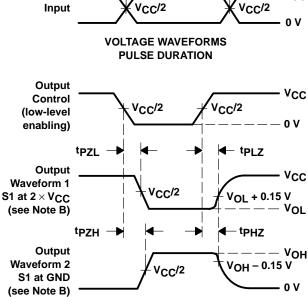
VCC

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V









VOLTAGE WAVEFORMS

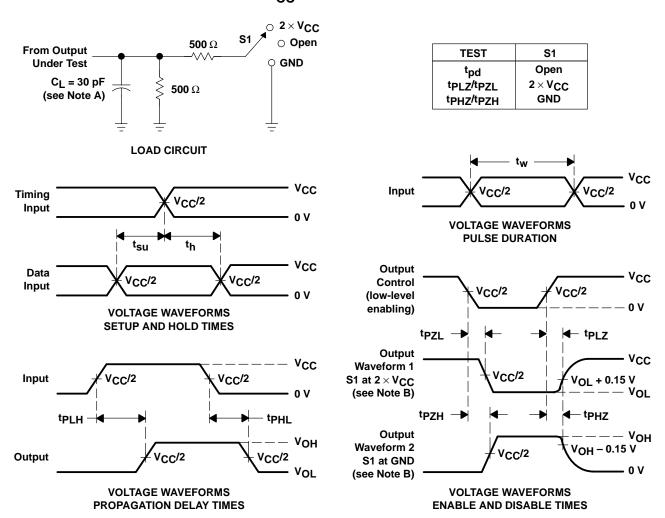
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



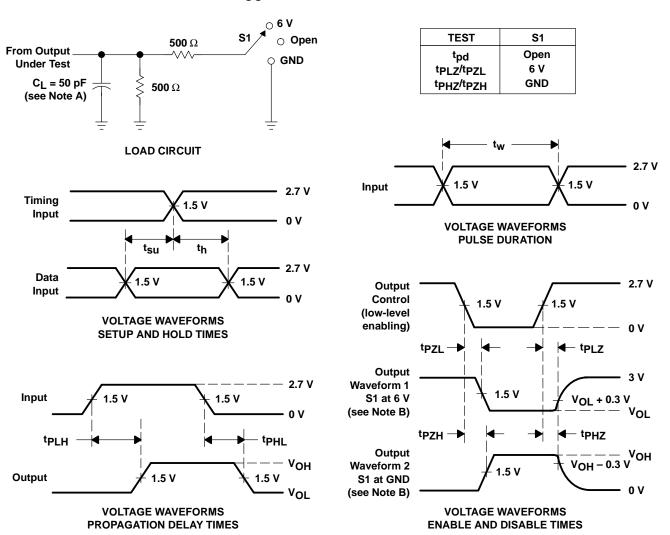
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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- Member of the Texas Instruments Widebus ™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 1-bit to 4-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16344 is used in applications in which four separate memory locations must be addressed by a single address.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16344 is characterized for operation from –40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

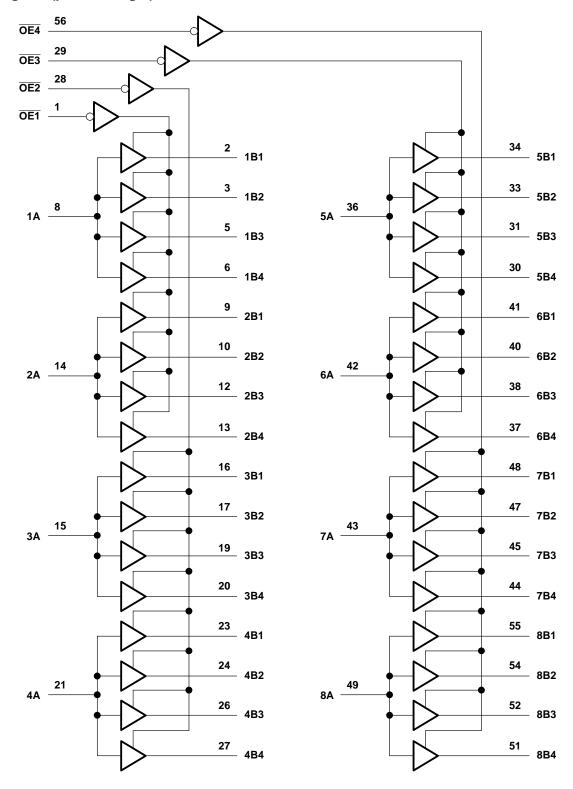
		Т		1
OE1	1	O	56	OE4
1B1	2		55]8B1
1B2	3		54]8B2
GND	4		53	GND
1B3	5		52	8B3
1B4	6		51] 8B4
V _{CC}	7		50	Vcc
1A			49]8A
2B1	9		48] 7B1
2B2	10		47	7B2
GND	11		46	GND
2B3	12		45] 7B3
2B4	13		44] 7B4
2A	14		43]7A
ЗА	15		42	6A
3B1	16			6B1
3B2	17		40]6B2
GND	18		39	GND
3B3	_		38] 6B3
3B4	20		37]6B4
4A	21		36]5A
V _{CC}	22		35] v _{cc}
4B1	23		34]5B1
4B2	24		33]5B2
GND	25		32	GND
4B3	26		31]5B3
4B4	27		30]5B4
OE2	28		29	OE3

FUNCTION TABLE

INPU	JTS	OUTPUT			
OE	Α	Bn			
L	Н	Н			
L	L	L			
Н	Н	Z			

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logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$		
Output clamp current, IOK (VO < 0)		
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND .		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stq}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	High lavel autout august	V _{CC} = 2.3 V		-12	mA	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Law lavel output ourrent	V _{CC} = 2.3 V		12	l . I	
loL	Low-level output current	V _{CC} = 2.7 V	12		mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT			
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2					
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2						
		$I_{OH} = -6 \text{ mA}$	2.3 V	2						
Vон			2.3 V	1.7			V			
		I _{OH} = -12 mA	2.7 V	2.2						
			3 V	2.4						
		I _{OH} = -24 mA	3 V	2						
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2				
		I _{OL} = 4 mA	1.65 V			0.45				
Voi		I _{OL} = 6 mA	2.3 V			0.4	, <u>,</u>			
VOL		lo 12 mA	2.3 V			0.7	V			
		I _{OL} = 12 mA	2.7 V			0.4				
		I _{OL} = 24 mA	3 V			0.55				
IĮ		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ			
		V _I = 0.58 V	1.65 V	25						
		V _I = 1.07 V	1.65 V	-25						
		V _I = 0.7 V	2.3 V	45						
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ			
` ´		V _I = 0.8 V	3 V	75						
		V _I = 2 V	3 V	-75						
		V _I = 0 to 3.6 V [‡]	3.6 V			±500				
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ			
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ			
ΔlCC		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ			
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		2.5		pF			
	Data inputs Outputs		3.3 V		3.5		pF			
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		4		þг			

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	А	В	§	1	4.6		4.6	1.4	4	ns
t _{en}	ŌE	В	§	1	6.2		6.2	1.2	5.1	ns
^t dis	ŌĒ	В	§	1	5.1		4.4	1.2	4	ns
t _{sk(o)} ¶									0.35	ns
t _{sk(o)} #									0.5	ns

[§] This information was not available at the time of publication.

[#] Skew between outputs of all banks and same package (A1 through A8 tied together).



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

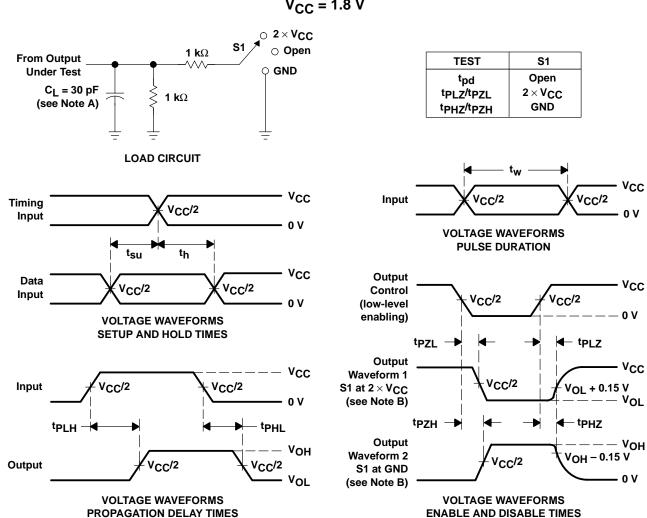
 $[\]P$ Skew between outputs of same bank and same package (same transition).

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
	FARAMETER	1E31 CONDITIONS	TYP	TYP	TYP	ONIT		
<u> </u>	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	68	84	pF	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	11	14	PF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



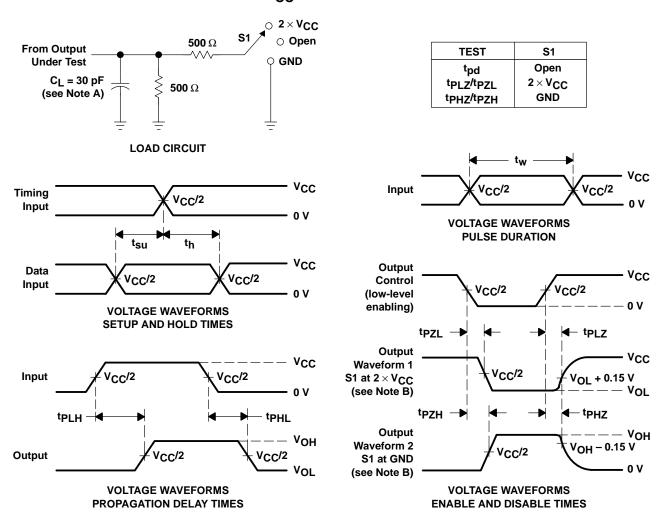
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

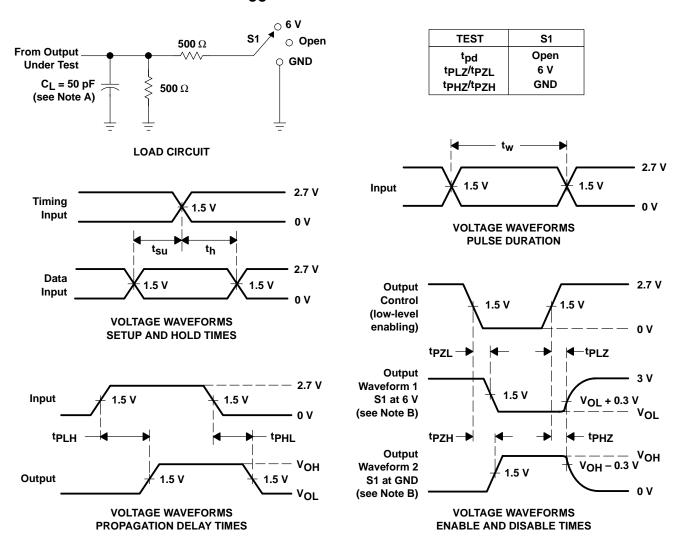


- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES020C - JULY 1995 - REVISED FEBRUARY 1999

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process 	1 0E
 ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	1Q2
Latch-Up Performance Exceeds 250 mA Per JESD 17	1Q4
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1Q5
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	1Q7
description	2Q2 [14 35] 2D2 GND [15 34] GND 2Q3 [16 33] 2D3
This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V _{CC} operation.	2Q4 [17 32] 2D4 V _{CC}
The SN74ALVCH16373 is particularly suitable for implementing buffer registers, I/O ports,	2Q5
bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched	2Q7 [22 27] 2D7 2Q8 [23 26] 2D8 2OE [24 25] 2LE

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16373 is characterized for operation from -40°C to 85°C.

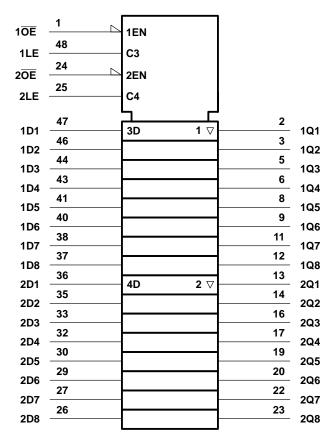
TEXAS INSTRUMENTS

at the levels set up at the D inputs.

FUNCTION TABLE (each 8-bit section)

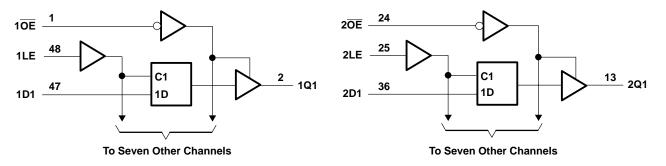
	INPUTS	OUTPUT			
OE	LE	Q			
L	Н	Н	Н		
L	Н	L	L		
L	L	Χ	Q_0		
Н	Χ	Χ	Z		

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES020C - JULY 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage			VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lau	OH High-level output current	V _{CC} = 2.3 V		-12	mA	
IOH		V _{CC} = 2.7 V		-12	IIIA	
		V _{CC} = 3 V		-24		
	DL Low-level output current	V _{CC} = 1.65 V		4		
loi		V _{CC} = 2.3 V		12	mA	
lOL		V _{CC} = 2.7 V		12	IIIA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature	-	-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004. SCES020C - JULY 1995 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT				
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2						
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2							
		$I_{OH} = -6 \text{ mA}$	2.3 V	2							
Vон			2.3 V	1.7			V				
		I _{OH} = -12 mA	2.7 V	2.2							
			3 V	2.4							
		I _{OH} = -24 mA	3 V	2							
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2					
		I _{OL} = 4 mA	1.65 V			0.45					
\/		I _{OL} = 6 mA	2.3 V			0.4	٧				
VOL		L- 40 mA	2.3 V			0.7					
		I _{OL} = 12 mA	2.7 V			0.4					
		I _{OL} = 24 mA	3 V			0.55					
IĮ		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ				
		V _I = 0.58 V	1.65 V	25							
		V _I = 1.07 V	1.65 V	-25			μΑ				
		V _I = 0.7 V	2.3 V	45							
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45							
` ´		V _I = 0.8 V	3 V	75							
		V _I = 2 V	3 V	-75							
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500					
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ				
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$		3.6 V			40	μΑ				
Δlcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ				
Ci	Control inputs Data inputs	V _I = V _{CC} or GND	3.3 V		3 6		pF				
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF				

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	§		1		1		1.1		ns
th	Hold time, data after LE↓	§		1.5	·	1.7		1.4		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM	FROM TO (INPUT)		V _{CC} = ± 0.2	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	†	1	4.5		4.3	1.1	3.6	20
^t pd	LE		†	1	4.9		4.6	1	3.9	ns
t _{en}	ŌĒ	Q	†	1	6		5.7	1	4.7	ns
t _{dis}	ŌĒ	Q	†	1.2	5.1		4.5	1.4	4.1	ns

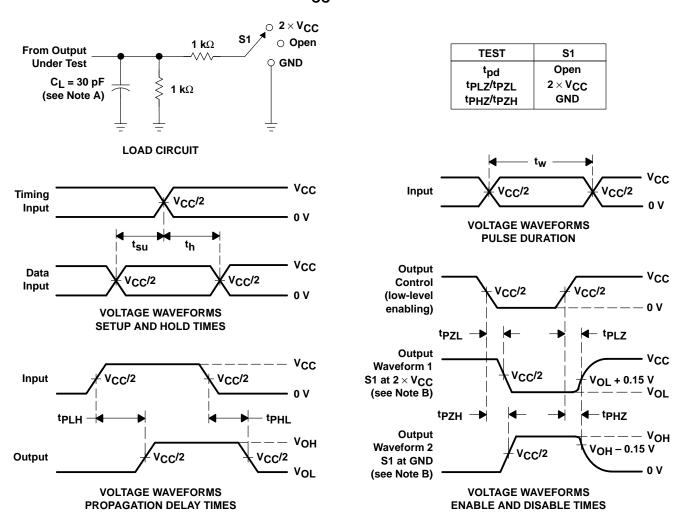
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	Power dissipation capacitance	Outputs enabled	C. 50 pF f 10 MU	†	19	22	pF
C _{pd}		Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	5	рг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

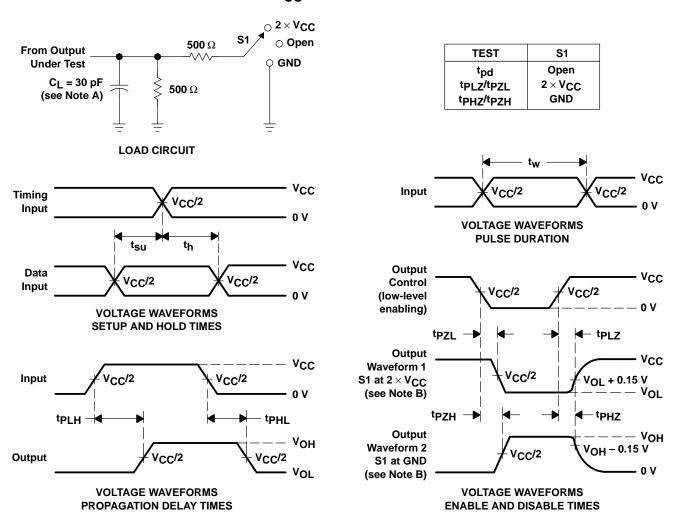


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

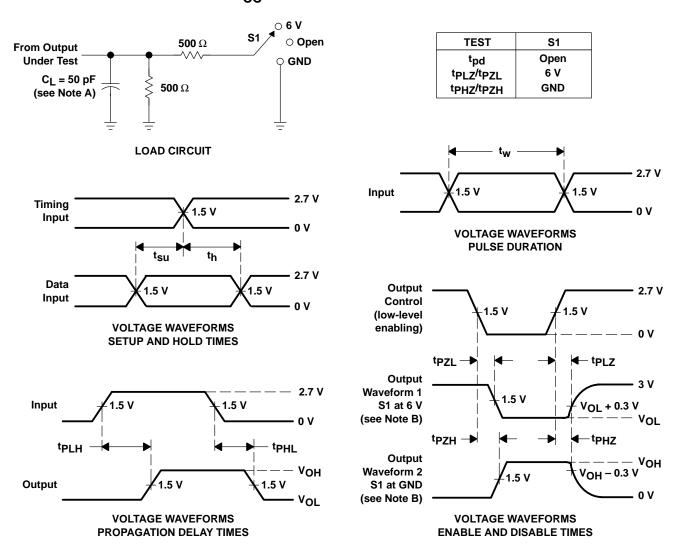


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

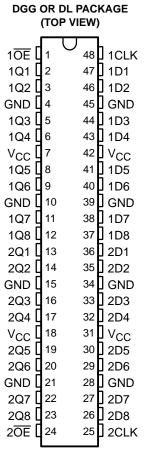
SCES021D - JULY 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs. \overline{OE} can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.



OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16374 is characterized for operation from -40°C to 85°C.

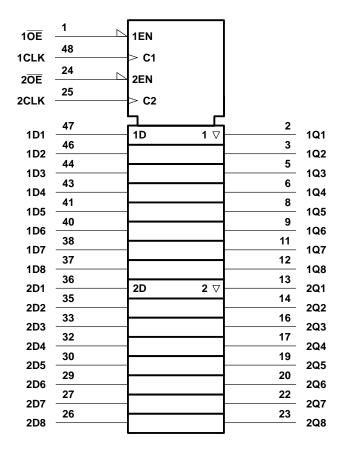
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FUNCTION TABLE (each flip-flop)

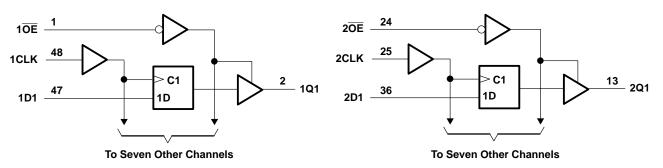
	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q ₀
Н	X	Χ	Z

logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021D - JULY 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
nput voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
nput clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, IOK (VO < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	
Package thermal impedance, θ_{JA} (see Note 3): DGG package	e 89°C/W
DL package	94°C/W
Storage temperature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
VIН	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lau	High level autout august	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	V _{CC} = 2.7 V		-12	IIIA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021D - JULY 1995 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2				
Vон	VOH			2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\/ - ·		I _{OL} = 6 mA		2.3 V			0.4	
VOL		I. 40 mA		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V		-	0.4	
		I _{OL} = 24 mA	I _{OL} = 24 mA				0.55	
l _l		V _I = V _{CC} or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V		-	40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs			221/		3		~ F
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF
Со	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MIN MAX		MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		2.1		2.2		1.9		ns
th	Hold time, data after CLK↑	§		0.6	·	0.5		0.5	·	ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	5.3		4.9	1	4.2	ns
t _{en}	ŌĒ	Q		†	1	6.2		5.9	1	4.8	ns
^t dis	ŌĒ	Q		†	1	5.3		4.7	1.2	4.3	ns

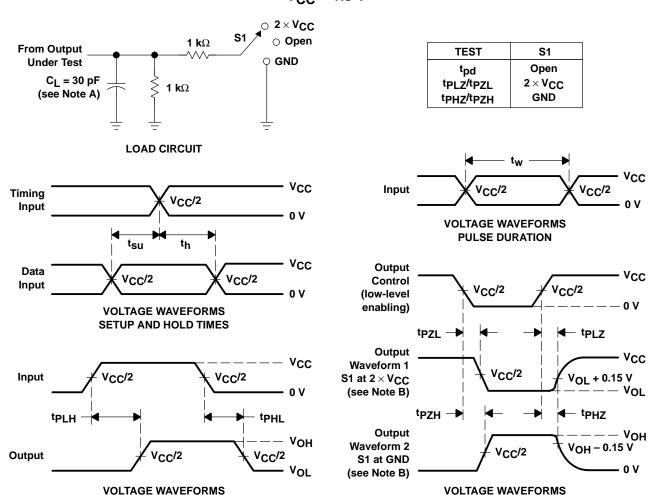
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
PARAMETER		1E31 CONDITIONS	TYP	TYP	TYP	UNIT		
	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	31	30	۰۲	
C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	16	18	pF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

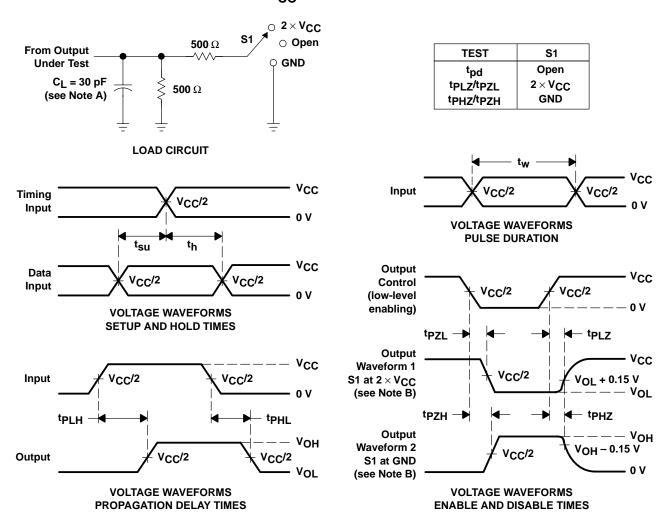
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

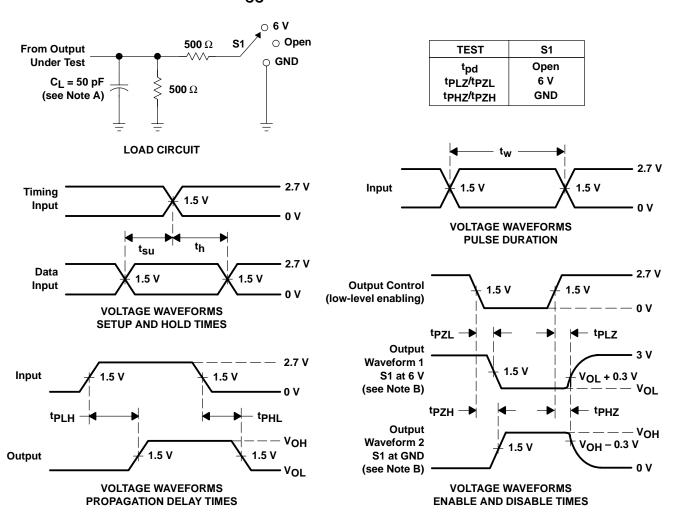


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2 ns. $t_{f} \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpZL and tpZH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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- **Member of the Texas Instruments** Widebus+™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBE** ™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0-SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

The data-flow control logic is designed to allow glitch-free data transmission.

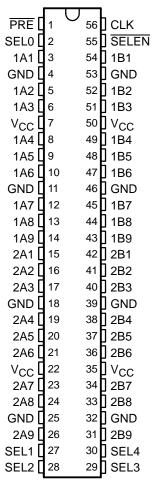
When preset (PRE) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both PRE and SELEN must be low and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down, $\overline{\mathsf{PRE}}$ should be tied to V_CC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16409 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)



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Function Tables

	INPUTS	OUTPUT
CLK	SEND PORT	RECEIVE PORT
Х	Х	_{В0} †
Х	L	L
Х	Н	Н
1	L	L
1	Н	Н
Н	X	в ₀ †
L	X	_{B0} †

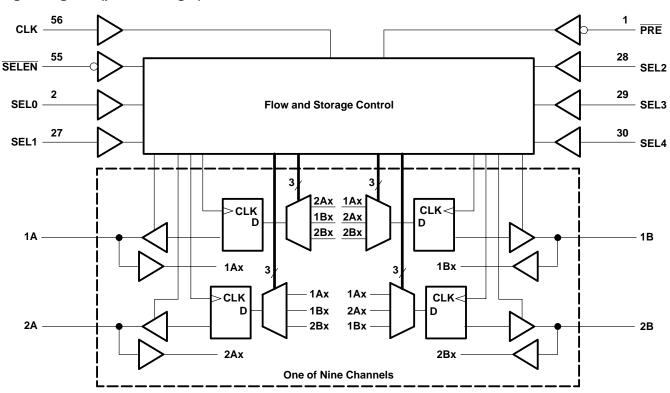
[†] Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

INPUTS								
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
Н	Х	Х	Х	Х	Х	Х	Х	All outputs disabled
L	Н	\uparrow	Х	X	X	X	Х	No change
L	L	1	0	0	0	0	0	None, all I/Os off
L	L	\uparrow	0	0	0	0	1	Not used
L	L	1	0	0	0	1	0	Not used
L	L	\uparrow	0	0	0	1	1	Not used
L	L	1	0	0	1	0	0	Not used
L	L	\uparrow	0	0	1	0	1	Not used
L	L	1	0	0	1	1	0	Not used
L	L	\uparrow	0	0	1	1	1	Not used
L	L	1	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	\uparrow	0	1	0	0	1	2A to 1A
L	L	1	0	1	0	1	0	2B to 1B
L	L	\uparrow	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	\uparrow	0	1	1	0	1	1A to 2A
L	L	1	0	1	1	1	0	1B to 2B
L	L	\uparrow	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	\uparrow	1	0	0	0	1	1A to 1B
L	L	1	1	0	0	1	0	2A to 2B
L	L	\uparrow	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	\uparrow	1	0	1	0	1	1B to 1A
L	L	1	1	0	1	1	0	2B to 2A
L	L	1	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	1	1	1	0	0	1	1B to 2A
L	L	1	1	1	0	1	0	2B to 1A
L	L	1	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	1	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	1	1	1	1	0	1	1A to 2B
L	L	1	1	1	1	1	0	2A to 1B
L	L	\uparrow	1	1	1	1	1	1A to 2B and 2A to 1B



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES022E - JULY 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
lau	High lavel autout august	$V_{CC} = 2.3 \text{ V}$		-12	mA	
IOH	High-level output current	$V_{CC} = 2.7 V$		-12		
		V _{CC} = 3 V	-24			
		V _{CC} = 1.65 V		4		
la.	Low-level output current	V _{CC} = 2.3 V		12		
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER	TEST Co	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
			3 V	2.4				
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\/a.		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V	
VOL	VOL	lo 12 mΛ	2.3 V			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
l _{OZ} §		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
^I CC		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\ensuremath{\$}}\mbox{ For I/O ports, the parameter I}_{\mbox{\ensuremath{OZ}}}\mbox{\ensuremath{$}}\mbox{includes the input leakage current.}$

SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			†		120		120		120	MHz
t _W	Pulse duration, CLK high	or low	†		4.2		4.2		3		ns
		A or B before CLK↑	†		1.9		1.9		1.4		
١.		SEL before CLK↑	†		5.1		4.2		3.5		ns
tsu	Setup time	SELEN before CLK↑	†		2.5		2.5		1.8		
		PRE before CLK↑	†		1		1		0.7		
		A or B after CLK↑	†		0.8		0.8		1		
th	Hold time	SEL after CLK↑	†		0		0		0		ns
		SELEN after CLK↑	†		0.5		0.5		0.8		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

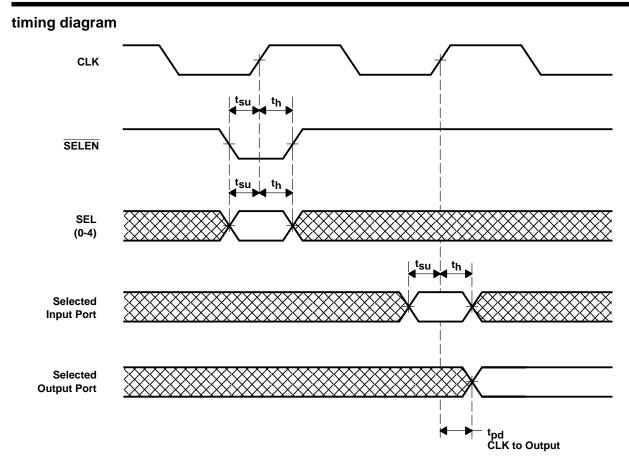
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		120		120		MHz
^t pd	CLK	A or B		†	1.5	6		5.7	1.5	5.1	ns
^t en	CLK	A or B		†	2.4	6.9		6.3	2	5.7	ns
4	CLK	A or B		†	2.3	7.1		6	2	5.7	no
^t dis	PRE	AUIB		†	2.8	7.5		6.5	2.5	6.1	ns

[†] This information was not available at the time of publication.

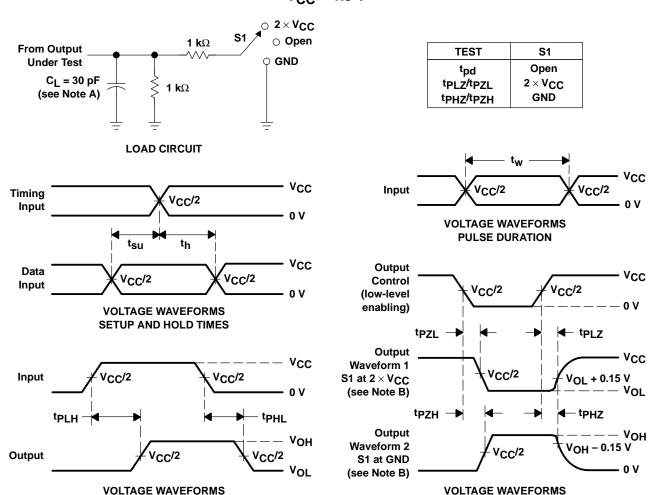
operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
<u> </u>	Power dissipation	All outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	60	60	pF
Cpd	capacitance per exchanger	All outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	60	60	рΓ

[†] This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

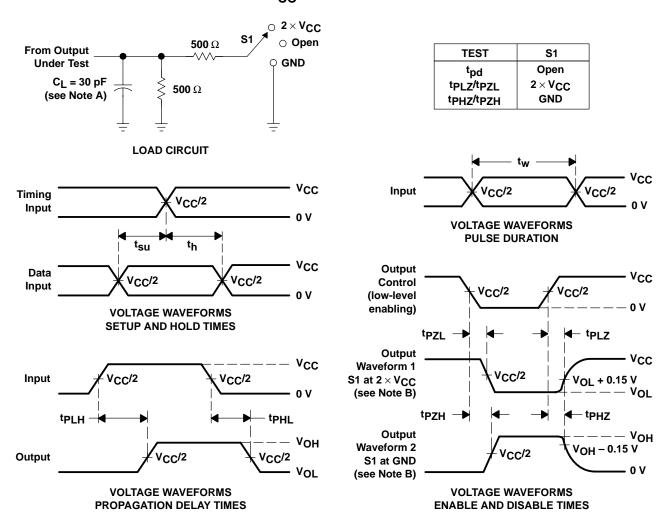
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

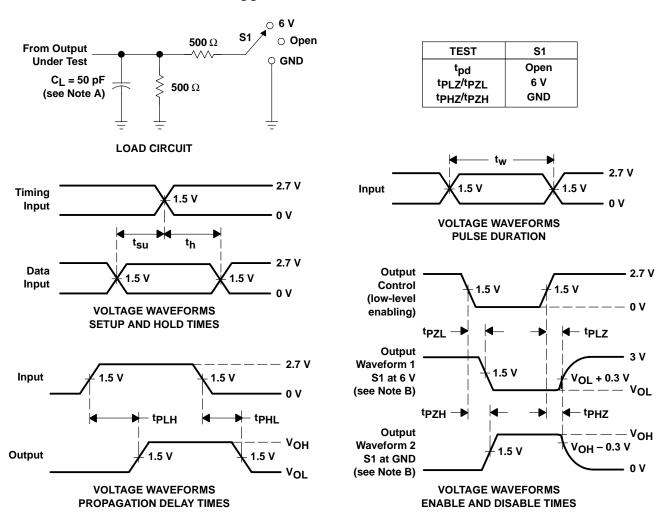


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2 ns. $t_{f} \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBT**™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Bus Hold on Data Inputs Eliminates the** Need for External Pullup/Pulldown **Resistors**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on high-to-low transition of Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

OEAB 56 ¶ GND LEAB **□**2 55 CLKAB А1 Пз 54**∏** B1 GND ∏4 53 GND A2 [5 52**∏** B2 51 B3 A3 🛮 6 V_{CC} **□**7 50 V_{CC} А4 П 8 49 **∏** B4 A5 🛮 9 48 🛮 B5 A6 🛮 10 47 B6 GND [46 GND 11 45 B7 A7 🛮 12 A8 [] 13 44**∏** B8 43 B9 A9 14 42 B10 A10 🛮 15 41 **∏** B11 A11 ∏ 16 40 **∏** B12 A12 | 17 GND Π 18 39 GND 38 **1** B13 A13 19 37 B14 A14 🛮 20 A15 21 36 B15 V_{CC} 🛮 22 35 V_{CC} A16 23 34 B16 A17 🛮 24 33 B17 GND 25 32 **[**] GND A18 **∏** 26 31 **[**] B18 OEBA 27 30 CLKBA LEBA 28 29 | GND

Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

To ensure the high-impedance state during power up or power down, $\overline{\mathsf{OEBA}}$ should be tied to V_CC through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is characterized for operation from –40°C to 85°C.

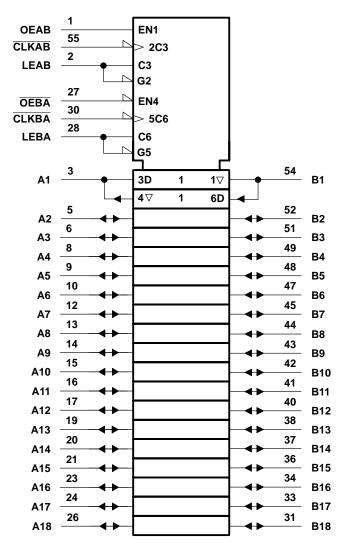
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FUNCTION TABLE†

	INPUTS								
OEAB	LEAB	CLKAB	Α	В					
L	Χ	Х	Χ	Z					
Н	Н	Χ	L	L					
Н	Н	Χ	Н	Н					
Н	L	0	L	L					
Н	L	\downarrow	Н	Н					
Н	L	L or H	Χ	в ₀ ‡					

[†]A-to-B data flow is shown: B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

logic symbol§

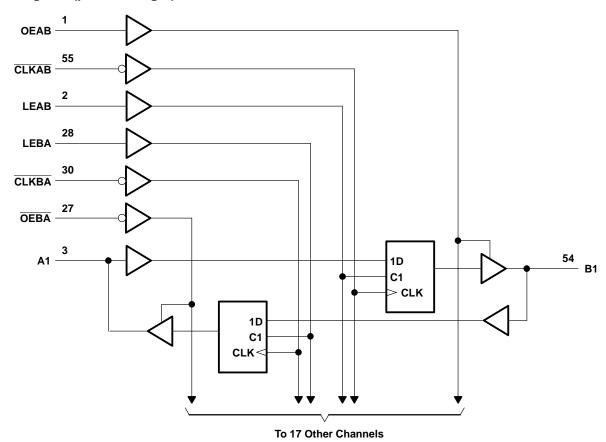


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package .	81°C/W
DL package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES023F – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
1	High level output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Lour lovel output outront	V _{CC} = 2.3 V		12	A
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES023F - JULY 1995 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24 \text{ mA}$		3 V	2			
		$I_{OL} = 100 \mu A$		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		loι – 12 mΛ		2.3 V			0.7	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
l _{OZ} §		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF
C _{io}	A or B ports	VO = VCC or GND		3.3 V		8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				†		150		150		150	MHz
	Pulse duration	LE high		†		3.3		3.3		3.3		20
t _W	Pulse duration	CLK high or low		†		3.3		3.3		3.3		ns
		Data before CLK↓		†		1.7		1.4		1.3		
t _{su}	Setup time	Data batana LEL	CLK high	†		1.1		1		1		ns
		Data before LE↓	CLK low	†		1.9		1.6		1.4		
		Data after CLK↓		†		1.7		1.6		1.3		
t _h	Hold time	Data after LE↓	CLK high	†		2		1.8		1.5		ns
		Data affel LEV	CLK low	†		1.6		1.5		1.2		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B	B or A		†	1	5.1		4.7	1	3.9	
t _{pd}	LEAB or LEBA	A or B		†	1	5.9		5.5	1	4.7	ns
	CLKAB or CLKBA	AUID		†	1	6.6		6.6	1.1	5.5	
t _{en}	OEAB	В		†	1	5.7		5.4	1	4.6	ns
^t dis	OEAB	В		†	1	6.1		5.7	1.5	5	ns
t _{en}	OEBA	Α		†	1	6.2		6.2	1	5.2	ns
t _{dis}	OEBA	Α		†	1	5.4		4.6	1	4.3	ns

[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
PARAMETER			TEST CONDITIONS	TYP	TYP	TYP	ONIT	
<u> </u>	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	40	51	~F	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pr}, f = 10 \text{ MHz}$	†	6	6	pF	

[†] This information was not available at the time of publication.

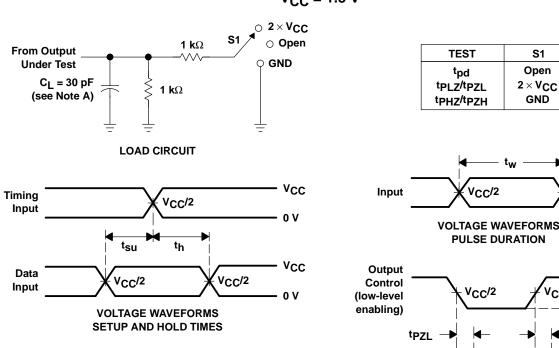
S1

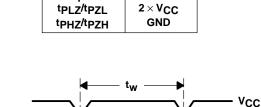
Open

V_{CC}/2

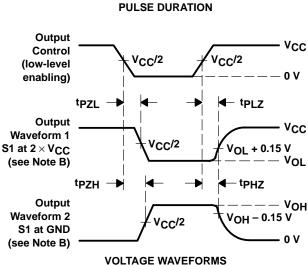
0 V

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





V_{CC}/2



ENABLE AND DISABLE TIMES

^tPLH tpHI VOH Output V_{CC}/2 $V_{CC}/2$ **VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**

NOTES: A. C_L includes probe and jig capacitance.

V_{CC}/2

Input

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

VCC

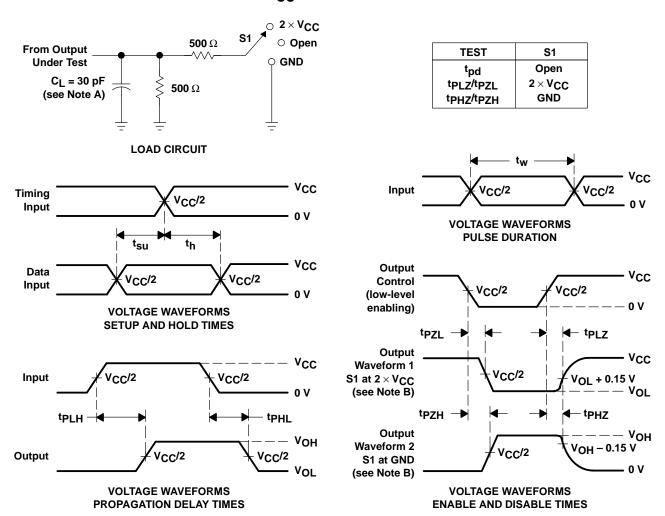
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.

V_{CC}/2

- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



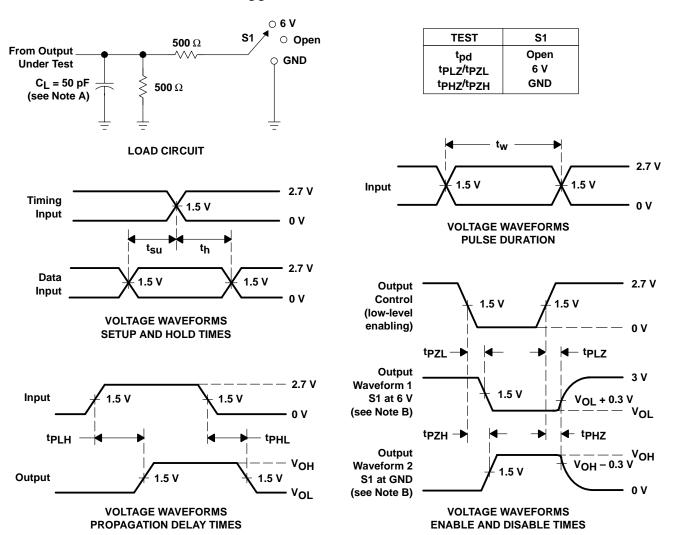
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES024C - JULY 1995 - REVISED FEBRUARY 1999

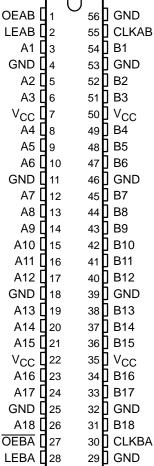
- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- UBT[™] (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)



Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16501 is characterized for operation from –40°C to 85°C.

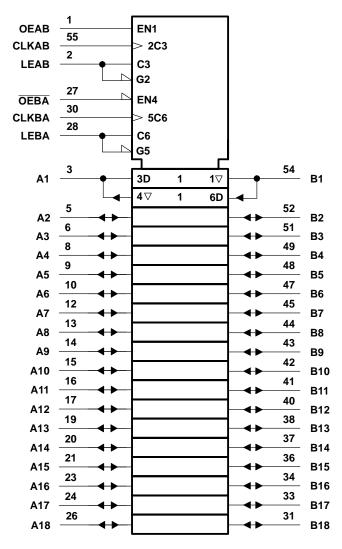
TEXAS INSTRUMENTS

FUNCTION TABLE†

	INPUTS								
OEAB	LEAB	CLKAB	Α	В					
L	Х	Х	Х	Z					
Н	Н	Χ	L	L					
Н	Н	Χ	Н	Н					
Н	L	\uparrow	L	L					
Н	L	\uparrow	Н	Н					
Н	L	L or H	Χ	в ₀ ‡					

[†] A-to-B data flow is shown: B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

logic symbol§

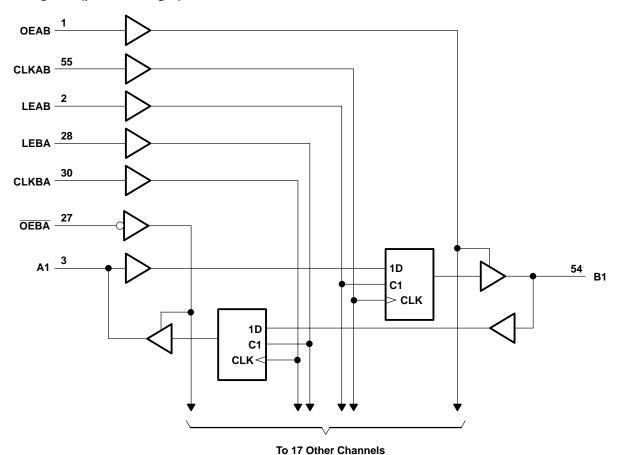


[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT			
VCC	Supply voltage		1.65	3.6	V			
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}					
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V			
		V _{CC} = 2.7 V to 3.6 V	2					
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$				
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$						
		V _{CC} = 2.7 V to 3.6 V		0.8				
٧ _I	Input voltage		0	VCC	V			
٧o	Output voltage		0	Vcc	V			
		V _{CC} = 1.65 V		-4				
1	High-level output current	V _{CC} = 2.3 V		-12	mA			
ЮН		V _{CC} = 2.7 V		-12	IIIA			
		V _{CC} = 3 V		-24				
		V _{CC} = 1.65 V		4				
1	Lour lovel output ourrent	V _{CC} = 2.3 V		12	A			
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA			
		V _{CC} = 3 V		24				
Δt/Δν	Input transition rise or fall rate			10	ns/V			
T _A	Operating free-air temperature		-40	85	°C			

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		Vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	.2			
^V ОН		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		I _{OH} = -6 mA	2.3 V	2					
				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V	
VOL		I _{OL} = 12 mA		2.3 V			0.7	v	
		IOL = 12 IIIA		2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55			
II		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ		
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V	1.65 V	-25					
		V _I = 0.7 V	2.3 V	45					
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ		
		V _I = 0.8 V	3 V	75					
		V _I = 2 V	3 V	-75					
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500			
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
ΔlCC		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V			750	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8		pF	

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock} Clock frequency				¶		150		150		150	MHz		
	Pulse duration	LE high		¶		3.3		3.3		3.3		ns	
t _W	Puise duration	CLK high or low	1	¶		3.3		3.3		3.3			
		Data before CL	K↑	¶		2.2		2.1		1.7			
t _{su}	Setup time	Data	CLK high	¶		1.9		1.6		1.5		ns	
		before LE↓	CLK low	¶		1.3		1.1		1			
t _h	Hold time	Data after CLK	`	¶		0.6		0.6		0.7			
		Data after LE↓	CLK high or low	¶		1.4		1.7		1.4		ns	

This information was not available at the time of publication.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES024C - JULY 1995 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B	B or A		†	1	4.8		4.5	1	3.9	
^t pd	LE	A or B		†	1.1	5.7		5.3	1.3	4.6	ns
	CLK			†	1.2	6.1		5.6	1.4	4.9	
t _{en}	OEAB	В		†	1	5.8		5.3	1	4.6	ns
^t dis	OEAB	В		†	1.5	6.2		5.7	1.4	5	ns
t _{en}	OEBA	А		†	1.3	6.3		6	1.1	5	ns
t _{dis}	OEBA	А		†	1.3	5.3		4.6	1.3	4.2	ns

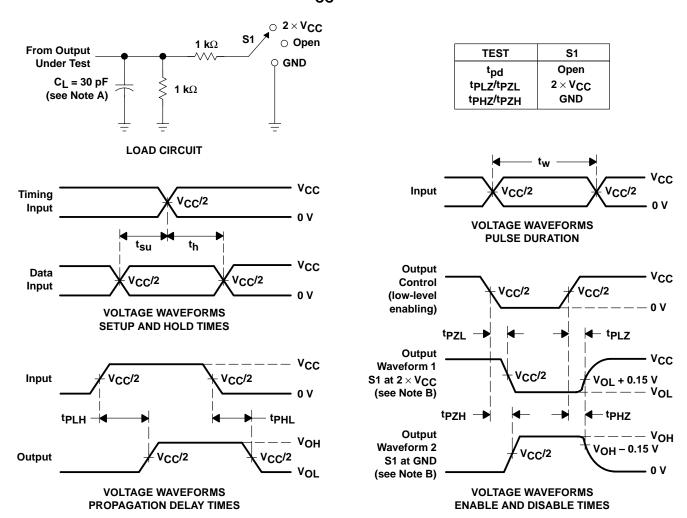
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
			TEST CONDITIONS	TYP	TYP	TYP	ONII	
	Power dissipation capacitance	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	44	54	pF	
Cpd		Outputs disabled	$C_L = 50 \text{ pH}, f = 10 \text{ MHz}$	†	6	6	рг	

[†] This information was not available at the time of publication.

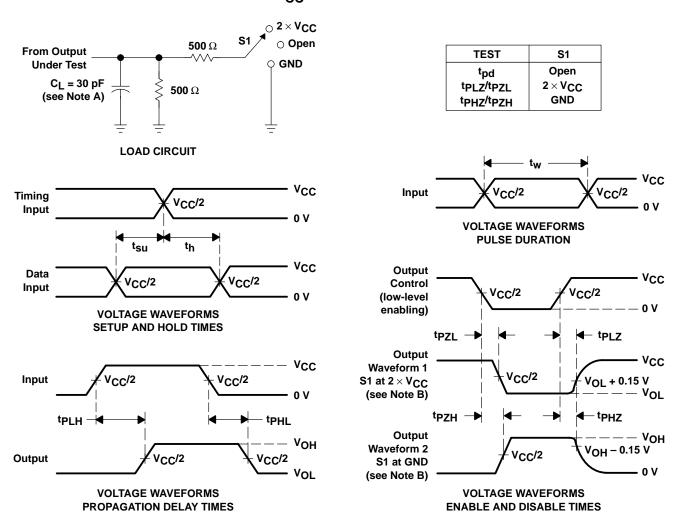
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



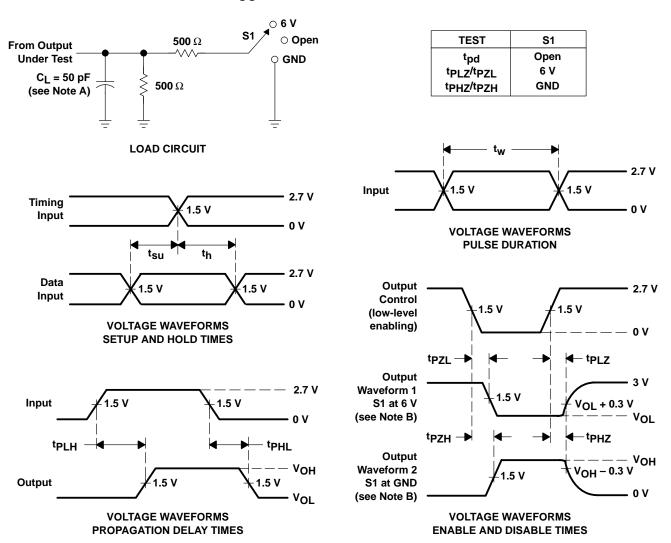
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16524 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

SCES080C - JULY 1996 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock-enable (CLKENBA) inputs. For the A-to-B data flow, the data flows through a single buffer. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select (SEL) input.

Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate CLKENBA input is low. The B-to-A data transfer is synchronized with CLK.

GND [56 ¶ GND OEAB 🛮 2 55 SEL A1 🛮 3 54 **∏** B1 GND 4 53 ¶ GND A2 🛮 5 52 B2 A3 **∏** 6 51 T B3 50 V_{CC} V_{CC} **∐** 7 A4 🛮 8 49 🛮 B4 A5 **∏** 9 48 **∏** B5 A6 🛮 10 47 ∏ B6 GND [] 11 46 ∏ GND A7 Π 12 45 ¶ B7 44 B8 A8 🛮 13 A9 🛮 14 43 T B9 A10 Π 15 42**∏** B10 41 TB11 A11 ∏ 16

40 **∏** B12

39 | GND

38 T B13

37 **∏** B14

36 **∏** B15

29 GND

A12 **∏** 17

GND **1**18

A13 **∏** 19

A14 Π 20

A15 **∏** 21

CLKENBA 28

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16524 is characterized for operation from -40°C to 85°C.

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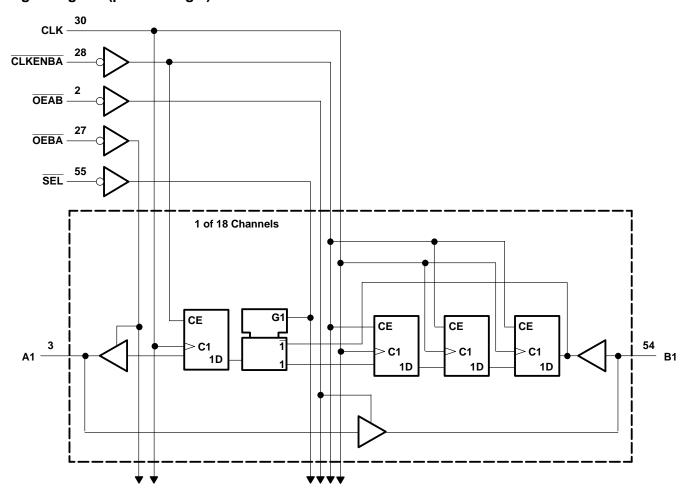


FUNCTION TABLE B-TO-A STORAGE (OEBA = L)

	INPUTS					
CLKENBA	CLK	SEL	В	Α		
Н	Χ	Х	Х	A ₀ †		
L	\uparrow	Н	L	L		
L	\uparrow	Н	Н	Н		
L	\uparrow	L	L	L‡		
L	\uparrow	L	Н	H [‡]		

[†]Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



[‡] Four positive CLK edges are needed to propagate data from B to A when SEL is low.

SN74ALVCH16524 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES080C - JULY 1996 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage r	ange, V _{CC}	
Input voltage rar	nge, V _I : Except I/O ports (see Note 1)	
	I/O ports (see Notes 1 and 2)	
Output voltage ra	ange, VO (see Notes 1 and 2)	
Input clamp curr	ent, I _{IK} (V _I < 0)	
Output clamp cu	rrent, I _{OK} (V _O < 0)	
Continuous outp	ut current, IO	±50 m/s
Continuous curre	ent through each V _{CC} or GND	±100 m
Package therma	I impedance, θ_{JA} (see Note 3): DGG p	package 81°C/V
		ckage
Storage tempera	ature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
۷o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	^	
ЮН	nign-ievei output current	V _{CC} = 2.7 V		-12	mA	
	/IH High-level input voltage /IL Low-level input voltage /I Input voltage /O Output voltage OH High-level output current \[\text{V} \text{V} \] Low-level output current \[\text{V} \text{V} \] Input transition rise or fall rate	V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Law lavel output ourrest	V _{CC} = 2.3 V		12	A	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate	<u>-</u>		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
VOH			2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
	I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
VOL	I _{OL} = 6 mA		2.3 V			0.4	V	
	I _{OL} = 12 mA		2.3 V			0.7	V	
			2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
IĮ		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-4 5			μΑ
, ,		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	- 75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V		-	±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			¶		120		125		150	MHz
t _W	Pulse duration, CLK high or low		¶		3.2		3.2		3		ns
	Setup time	B data before CLK↑	¶		1.5		1.2		1.1		ns
t _{su}		SEL before CLK↑	¶		2.7		2.4		2.1		
		CLKENBA before CLK↑	¶		2.7		2.6		2		
		B data after CLK↑	¶		1		0.6		1.2		
t _h I	Hold time	SEL after CLK↑	¶		0.5		0.2		0.8		ns
		CLKENBA after CLK↑	¶		0.1		0.1		0.3		

 $[\]P$ This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]S$ For I/O ports, the parameter IOZ includes the input leakage current.

SCES080C - JULY 1996 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(114701) (0017)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		125		150		MHz
4 .	А	В		†	1	3.9		3.8	1	3.2	no
^t pd	CLK	А		†	1	6.1		6.2	1	5.2	ns
t _{en}	OEAB or OEBA	A or B		†	1	6.1		6.1	1	5.1	ns
^t dis	OEAB or OEBA	A or B		†	1	6.3		5.4	1	4.9	ns

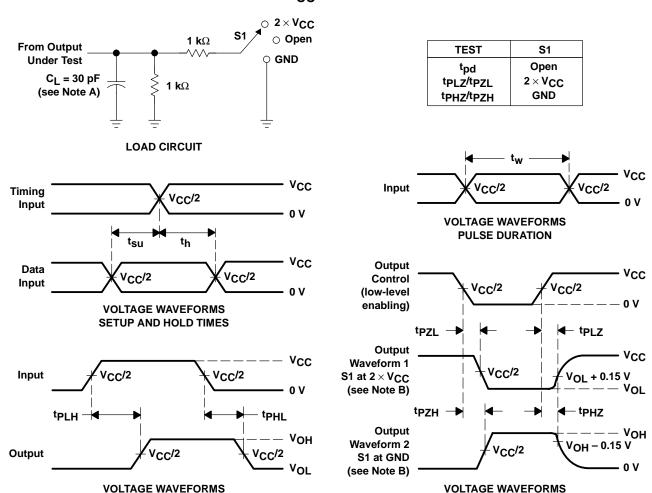
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP		
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	160	160	ς.E
Cpd	capacitance Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	160	160	pF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

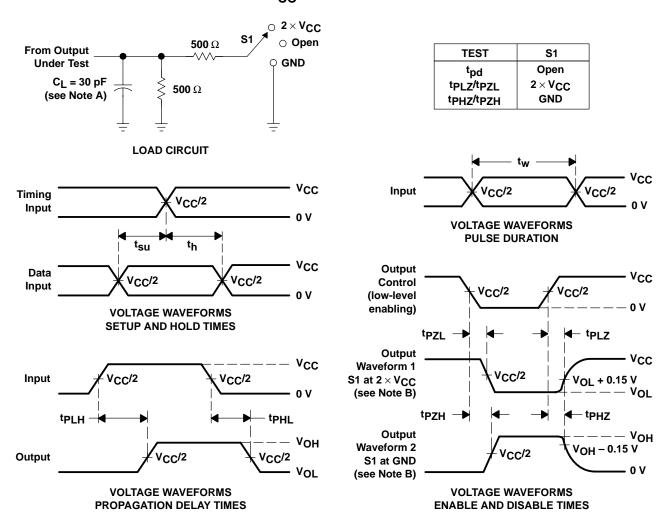
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

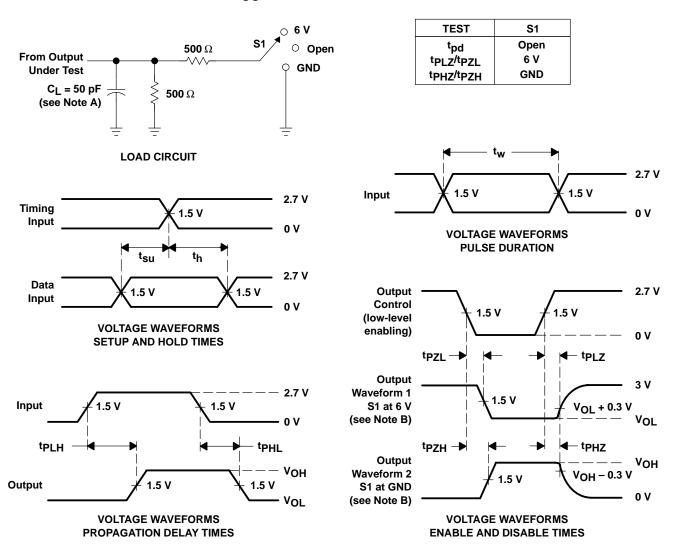


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzi and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

SCES059C - NOVEMBER 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock-enable (CLKENAB and CLKENBA) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select (SEL) input.

Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

CLKENAB 56 SEL OEAB 2 55 CLKAB A1 **Π**3 54 **∏** B1 GND ¶4 53 NG GND A2 5 52 **| B**2 51 | B3 АЗ 50 🛮 V_{CC} V_{CC} 8 A4 49**∏** B4 A5 48 **∏** B5 47 B6 A6 110 GND 46 | GND 11 Α7 12 45 **∏** B7 Α8 **∏** 13 44 🛮 B8 Α9 14 43 **∏** B9 A10 15 42 **∏** B10 A11 П 16 41 **∏** B11 A12 17 40**∏** B12 GND **∏** 18 39 | GND A13 **∏** 19 38 B13

А14 П

A15 [] 21

V_{CC} [] 22 A16 [] 23

A17 | 24

П 25

127

GND

OEBA

CLKENBA 28

A18 **∏** 26

20

37 N B14

36 **∏** B15

35 [] V_{CC}

34**∏** B16

33**∏** B17

32 | GND

31 **|** B18

30 CLK1BA

29 CLK2BA

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from -40°C to 85°C.

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TEXAS

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Function Tables

A-TO-B STORAGE (OEAB = L)

II.	NPUTS		OUTPUT
CLKENAB	CLKAB	Α	В
Н	Χ	Χ	в ₀ †
L	\uparrow	L	L
L	\uparrow	Н	Н

[†] Output level before the indicated steady-state input conditions were established

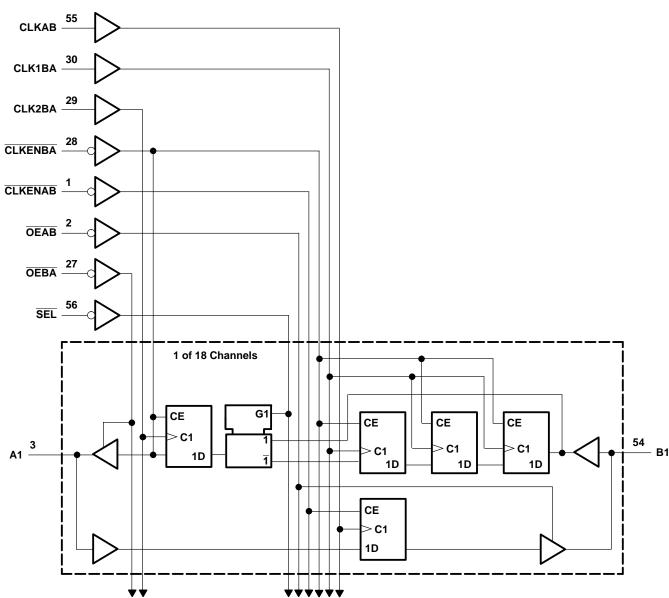
B-TO-A STORAGE $(\overline{OEBA} = L)$

	OUTPUT				
CLKENBA	CLK2BA	CLK1BA	SEL	В	Α
Н	Х	Х	Χ	Χ	A ₀ †
L	\uparrow	Χ	Н	L	L
L	\uparrow	Χ	Н	Н	Н
L	\uparrow	\uparrow	L	L	L‡
L	\uparrow	\uparrow	L	Н	H‡

[†] Output level before the indicated steady-state input conditions were established

 $[\]ddagger$ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when $\overline{\text{SEL}}$ is low.

logic diagram (positive logic)



SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059C - NOVEMBER 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	Vcc	V	
۷o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-12		
		Deltage Del				
		V _{CC} = 1.65 V		4		
	Lour lovel output ourrent	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP† M	AX	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	VCC-0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
Vон	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
VOH IOH = -100 μA						
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V		0	.45	
V _{OL}	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	\/
	lo 12 mA	2.3 V			0.7	V
	IOL = 12 IIIA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V		0	.55	
Ц	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±5	00	
loz§	$V_O = V_{CC}$ or GND	3.6 V		±	10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		7	'50	μΑ
C _i Control inputs	V _I = V _{CC} or GND	3.3 V		3		pF
C _{io} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	ck Clock frequency			†		120		125		150	MHz
t _W	Pulse duration, CLK high or low		†		3.2		3.2		3		ns
		A data before CLKAB↑	†		1.3		1.3		1.3		
		B data before CLK2BA↑	†		2.1		1.8		1.7		ns
	Setup time	B data before CLK1BA↑	†		1.3		1.2		1.1		
t _{su}		SEL before CLK2BA↑	†		3.3		3.3		3.3		
		CLKENAB before CLKAB↑	†		2.1		1.9		1.6		
		CLKENBA before CLK1BA↑	†		2.7		2.5		2.1		
		CLKENBA before CLK2BA↑	†		2.7		2.5		2.2		
		A data after CLKAB↑	†		0.7		0.4		0.9		
		B data after CLK2BA↑	†		0.4		0		0.6		
		B data after CLK1BA↑	†		0.8		0.4		1		
t _h	Hold time	SEL after CLK2BA↑	†		0		0		0.1		ns
		CLKENAB after CLKAB↑	†		0.1		0.3		0.3		
		CLKENBA after CLK1BA↑	†		0		0		0.1		
		CLKENBA after CLK2BA↑	†		0		0		0		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		125		150		MHz
^t pd	CLKAB or CLK2BA	A or B		†	1	4.5		4.4	1	4.2	ns
t _{en}	OEAB or OEBA	A or B		†	1	6.1		6.1	1	5.1	ns
^t dis	OEAB or OEBA	A or B		†	1	6.3		5.4	1	4.9	ns

[†] This information was not available at the time of publication.

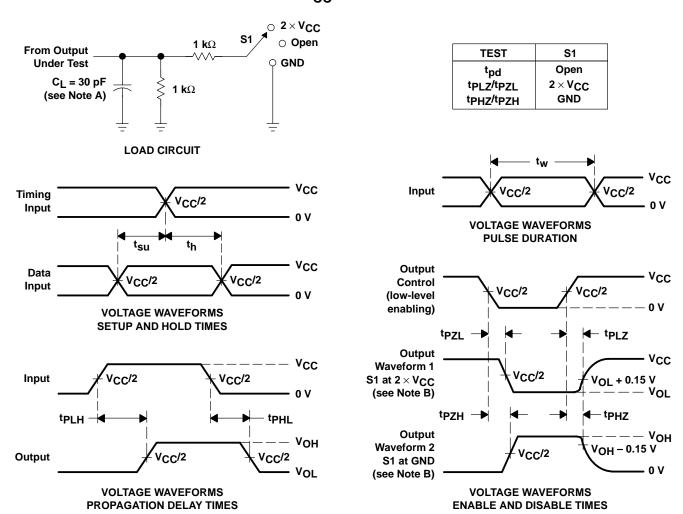
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
			TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	160	160	pF	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	160	160	pr	

[†] This information was not available at the time of publication.



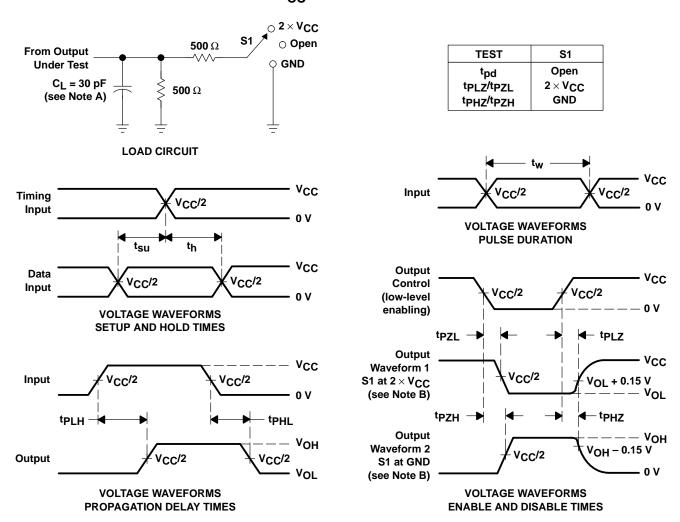
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



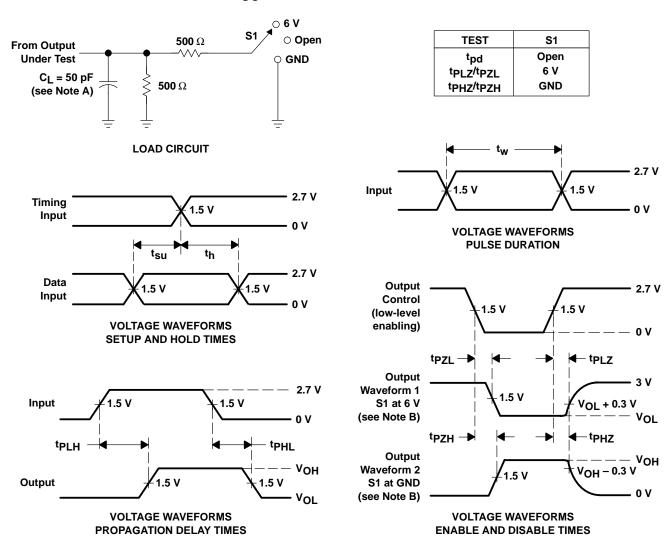
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16540 provides a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16540 is characterized for operation from -40°C to 85°C.

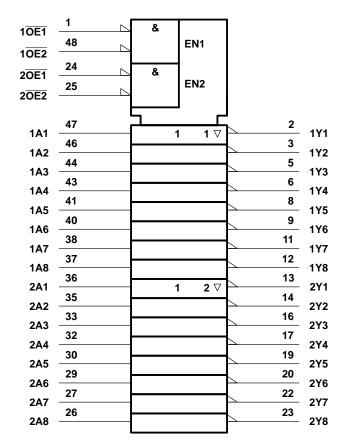
FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
Н	X	Χ	Z
Х	Н	X	Z

DGG OR DL PACKAGE (TOP VIEW)

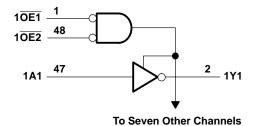
		$\overline{}$		1
1 0E1 [1	O	48	1 0E 2
1Y1 [2		47] 1A1
1Y2 [3		46] 1A2
GND [4		45	GND
1Y3 [44] 1A3
1Y4	1		43] 1A4
v _{cc} [42	$[]$ $v_{\rm cc}$
1Y5 [41] 1A5
1Y6			40] 1A6
GND [39] GND
1Y7 [38] 1A7
1Y8			37] 1A8
2Y1 [36	2A1
2Y2			35	: :-
GND [34	GND
2Y3 [16		33	2A3
2Y4	_		32	2A4
	18		31	□ v _{cc}
2Y5			30	
2Y6 [29	2A6
GND [28	
2Y7 [27	2A7
2Y8			26	2A8
2 0E1	24		25	2 <u>OE2</u>
				ı

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[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



2OE1 24 25 25 2A1 36 13 2Y1
To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	−50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
		V _{CC} = 2.7 V to 3.6 V	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8		
٧ _I	Input voltage	·	0	Vcc	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	High lavel autout average	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Law laval autout aumant	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature	-40	85	°C		

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN T	YPT MAX	UNIT	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -6 mA	2.3 V	2			
Voн		2.3 V	1.7		V	
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2		
	I _{OL} = 4 mA	1.65 V		0.45		
Max	I _{OL} = 6 mA	2.3 V		0.4	\ /	
VOL		2.3 V		0.7	V	
	I _{OL} = 12 mA	2.7 V		0.4		
	I _{OL} = 24 mA	3 V		0.55		
Ц	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ	
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μΑ	
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	- 75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500		
I _{OZ}	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ	
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ	
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	μΑ	
C _i Control inputs Data inputs	V _I = V _{CC} or GND	3.3 V		-	pF	
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V			pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2 ± 0.2	2.5 V V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPOT)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	Α	Υ								ns
t _{en}	ŌĒ	Y								ns
t _{dis}	ŌĒ	Υ								ns

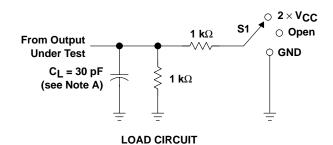
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

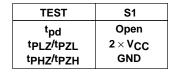
V_{CC}/2

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
<u> </u>	Power dissipation capacitance	Outputs enabled	Cı = 0. f = 10 MHz				ρF
Cpd	rowei dissipation capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$	łz -			pr

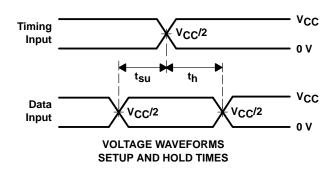
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

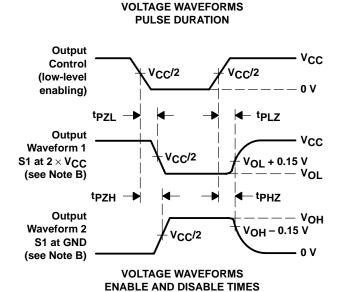


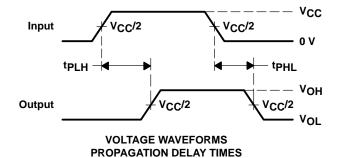


V_{CC}/2

Input







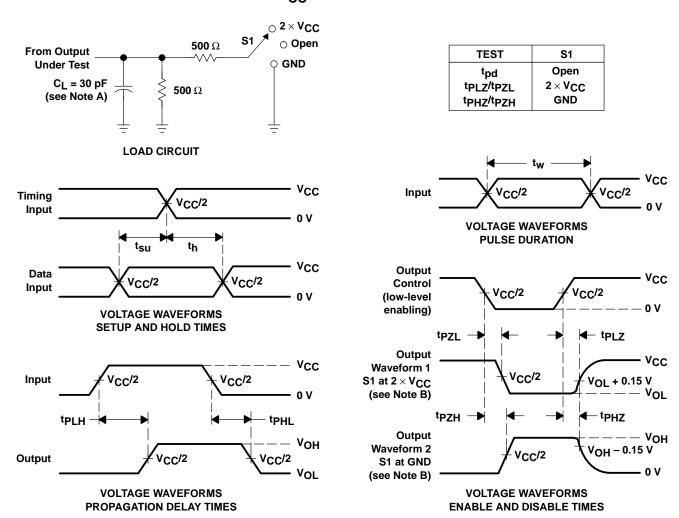
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Ω} = 50 Ω , $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



NOTES: A. C_I includes probe and jig capacitance.

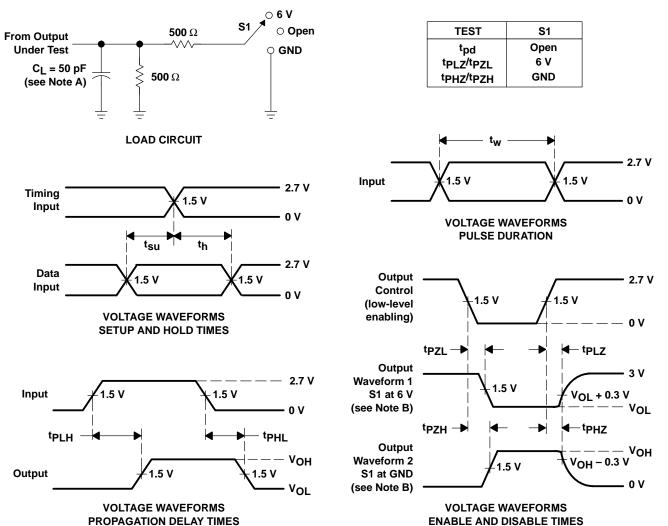
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the output enables (10E1 and 10E2 or 20E1 and 20E2) must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Χ	Z

DGG OR DL PACKAGE (TOP VIEW)

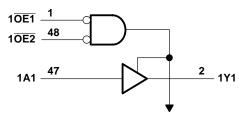
1		\top		
1 0E1 [1	\cup	48	1 <u>OE</u> 2
1Y1 [2		47]1A1
1Y2 🛚	3		46] 1A2
GND [4			GND
1Y3 🛚	5		44	1A3
1Y4 🛚			43	1A4
v _{cc} [7		42	v_{cc}
1Y5 🛚				1A5
1Y6 🛚			40	1A6
GND [GND
1Y7 🛚				_
1Y8 🛚			37	1A8
2Y1 🛚			36	2A1
2Y2 🛚			35	2A2
GND [34	GND
2Y3 🛚	16		33	2A3
2Y4 🛚			32	2A4
v _{cc} [31	
2Y5 🛚			30	2A5
2Y6 🛚			29	2A6
GND L	21		28	GND
2Y7 🛚			27	
2Y8 🛚			26	2A8
2 0E1	24		25	2 <u>OE2</u>

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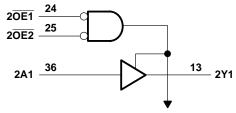
10E1 10E2 20E1 20E2	1 48 24 25	& &	EN1		
444	47	<u> </u>		2	41/4
1A1	46	'	l 1 ▽	3	1Y1
1A2	44			5	1Y2
1A3 1A4	43			6	1Y3 1Y4
	41			8	
1A5 1A6	40			9	1Y5
1A6 1A7	38			11	1Y6
	37			12	1Y7
1A8 2A1	36	1	l 2 ▽	13	1Y8 2Y1
2A1	35		I 2 V	14	2Y2
2A2 2A3	33			16	2Y3
2A3 2A4	32			17	213 2Y4
2A4 2A5	30			19	214 2Y5
2A5 2A6	29			20	213 2Y6
2A7	27			22	2Y7
2A7 2A8	26			23	217 2Y8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		8.0	
٧ _I	Input voltage	•	0	VCC	V
۷o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High-level output current	V _{CC} = 2.3 V		-12	A
ЮН		V _{CC} = 2.7 V		-12	mA
VIL VI VO IOH		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Law law law and a summer	V _{CC} = 2.3 V		12	A
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN T	YPT MAX	UNIT	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -6 mA	2.3 V	2			
Voн		2.3 V	1.7		V	
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2		
	I _{OL} = 4 mA	1.65 V		0.45		
Max	I _{OL} = 6 mA	2.3 V		0.4	\ /	
VOL		2.3 V		0.7	V	
	I _{OL} = 12 mA	2.7 V		0.4		
	I _{OL} = 24 mA	3 V		0.55		
Ц	V _I = V _{CC} or GND	3.6 V		±5	μΑ	
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μΑ	
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	- 75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500		
I _{OZ}	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ	
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ	
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	μΑ	
C _i Control inputs Data inputs	V _I = V _{CC} or GND	3.3 V		-	pF	
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V			pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INFOT)	(001F01)	TYP	MIN MAX	MIN MAX	MIN MAX	
t _{pd}	Α	Y					ns
t _{en}	ŌE	Y					ns
^t dis	ŌĒ	Y					ns



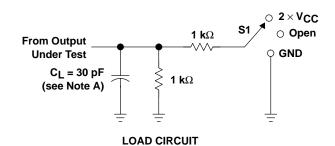
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

operating characteristics, T_A = 25°C

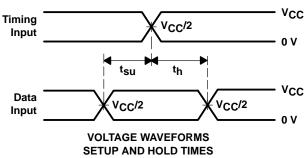
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	V _{CC} = 3.3 V	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP	ONIT	
<u> </u>	Dower dissination conscitance	Outputs enabled	Cı = 0. f = 10 MHz				nE.
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$				pF

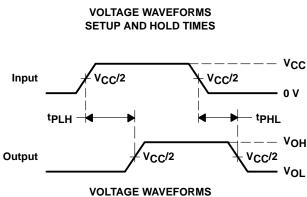
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

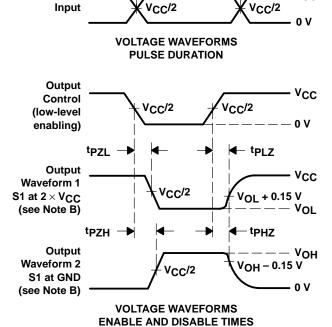
Input



TEST S1 Open tpd tPLZ/tPZL $2 \times V_{CC}$ GND tPHZ/tPZH







NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Ω} = 50 Ω , $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

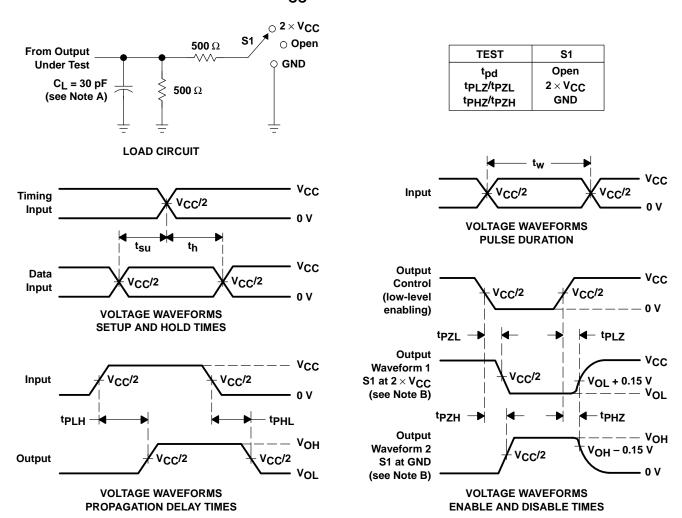
PROPAGATION DELAY TIMES

- tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



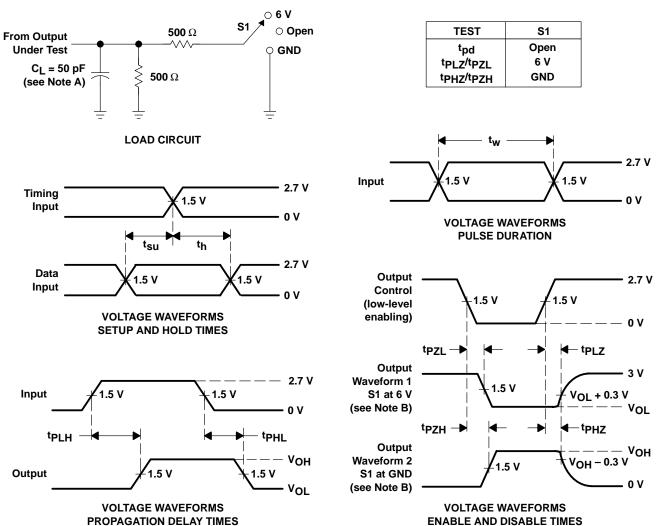
- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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- Member of the Texas Instruments

 Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

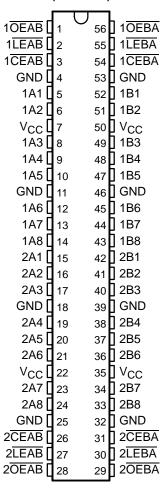
description

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

DGG OR DL PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

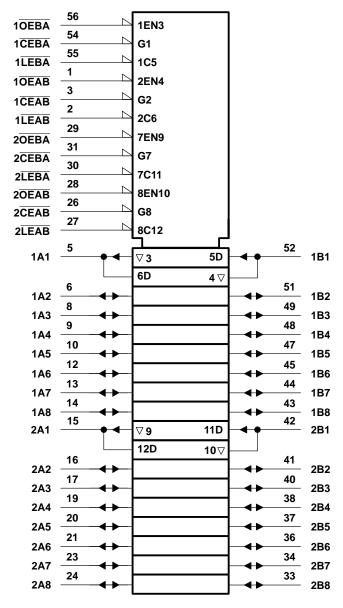
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16543 is characterized for operation from -40°C to 85°C.

of publication date.

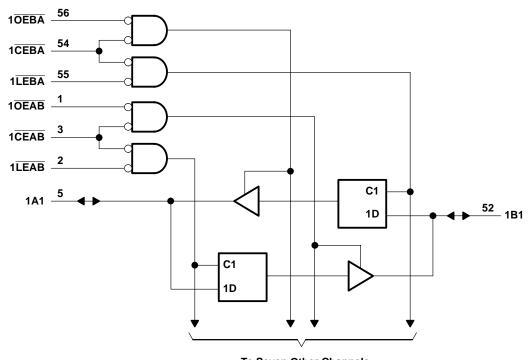
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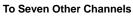
logic symbol†

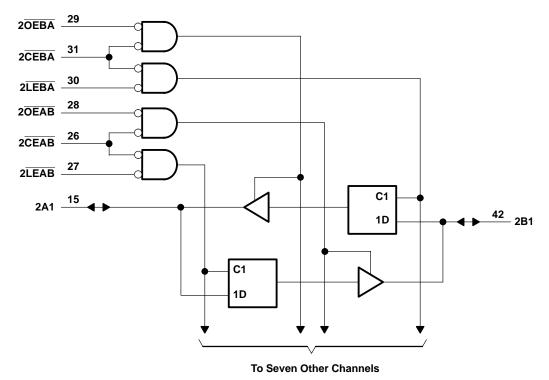


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)







SCES025D - JULY 1995 - REVISED FEBRUARY 1999

FUNCTION TABLE† (each 8-bit section)

	INPUTS						
CEAB	LEAB	OEAB	Α	В			
Н	Х	Х	Х	Z			
Х	Χ	Н	Χ	Z			
L	Н	L	Χ	в ₀ ‡			
L	L	L	L	L			
L	L	L	Н	Н			

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

[‡] Output level before the indicated steady-state input conditions were established

SN74ALVCH16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCES025D – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	LP als level and an extend assessed	V _{CC} = 2.3 V		-12	mA	
VIH High-level is VIL Low-level is VI Input voltag VO Output volt IOH High-level of Δt/Δv Input transi	High-level output current	V _{CC} = 2.7 V		-12	IIIA	
		V _{CC} = 3 V		3.6 0.35 × V _{CC} 0.7 0.8 V _{CC} V _{CC} -4 -12		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	m 1	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24	1	
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\/a:		I _{OL} = 6 mA		2.3 V			0.4	V
VOL		I 40 m/		2.3 V			0.7	·
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V		0.55			
IĮ		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
` ′		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		3.5		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE or CE	low	¶		3.3		3.3		3.3		ns
t _{su}	Setup time	Data before LE↑ or CE↑	¶		1.2		1.5		1.2		ns
th	Hold time	Data after LE↑ or CE↑	¶		1.2	·	0.8		1.3	·	ns

 $[\]P$ This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1111 01)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B	B or A	†	1	5.1		4.8	1	4.3	no
^t pd	LE	A or B	†	1	6.5		6.2	1.1	5	ns
t _{en}	CE	A or B	†	1	7.2		6.9	1	5.6	ns
t _{dis}	CE	A or B	†	1.3	6.1		6.2	1.5	5.1	ns
t _{en}	ŌĒ	A or B	†	1	6.8		6.3	1	5.3	ns
t _{dis}	ŌĒ	A or B	†	1	5.7		4.8	1.1	4.6	ns

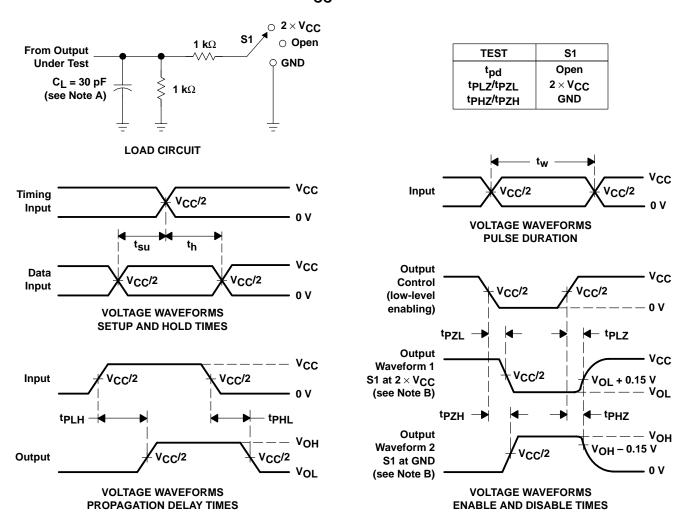
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
		TEST CONDITIONS	TYP	TYP	TYP			
	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	54	64	pF	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	6	7	pr	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



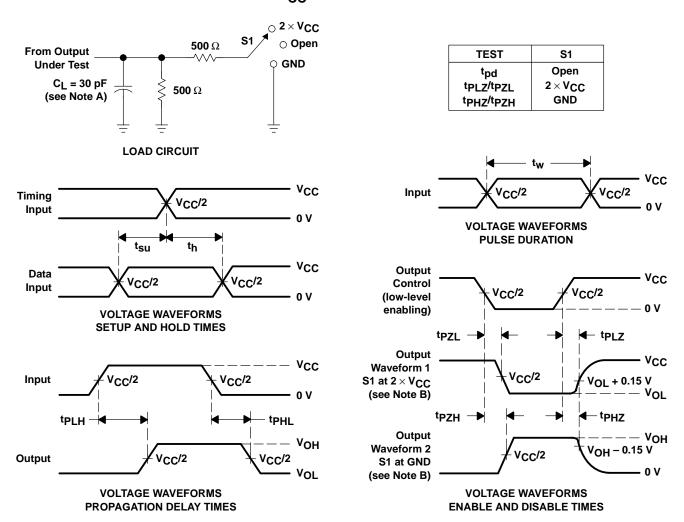
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

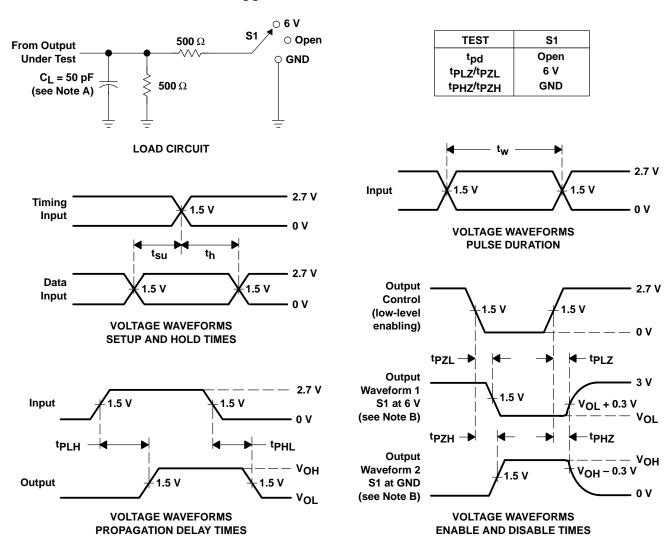


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- UBT[™] (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

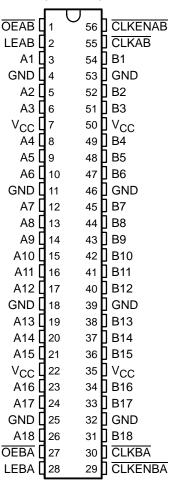
description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the

DGG OR DL PACKAGE (TOP VIEW)



clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16600 is characterized for operation from -40°C to 85°C.

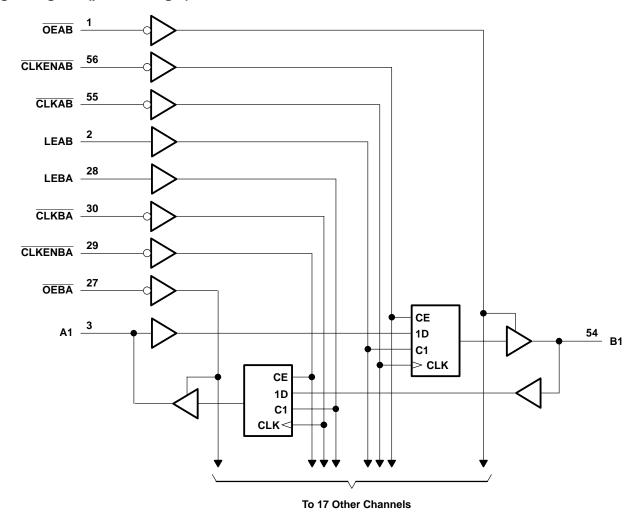
TEXAS INSTRUMENTS

FUNCTION TABLE†

	I	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Χ	Z
Х	L	Н	Χ	L	L
Х	L	Н	Χ	Н	Н
Н	L	L	Χ	Χ	в ₀ ‡
Н	L	L	Χ	Χ	в ₀ ‡ в ₀ ‡
L	L	L	\downarrow	L	L
L	L	L	\downarrow	Н	Н
L	L	L	L or H	Χ	в ₀ ‡

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established

SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG page	ckage 81°C/W
DL packa	age 74°C/W
Storage temperature range, T _{stq}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
VIН	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	1.65 3.6 = 1.65 V to 1.95 V 0.65 × V _{CC} = 2.3 V to 2.7 V 1.7 = 2.7 V to 3.6 V 2 = 1.65 V to 1.95 V 0.35 × V _{CC} = 2.3 V to 2.7 V 0.7 = 2.7 V to 3.6 V 0.8 0 V _{CC} 0 V _{CC} = 1.65 V -4 = 2.3 V -12 = 3 V -24 = 1.65 V 4 = 2.3 V 12 = 2.7 V 12		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		3.6 0.35 × V _{CC} 0.7 0.8 V _{CC} V _{CC} -4 -12 -12 -24 4 12 12 24 10	
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-12	A
ІОН	nign-iever output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Lavidaval autout avenue	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		0.35 × V _{CC} 0.7 0.8 V _{CC} -4 -12 -12 -24 4 12 12 24 10	
Δt/Δν	Input transition rise or fall rate	-		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	VCC-0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
Vol	VOL				0.4	V
VOL	I _{OL} = 12 mA	2.3 V			0.7	V
	IOL = 12 IIIA	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V ₁ = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V ₁ = 2 V	3 V	-75			
	$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4		pF
C _{io} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				†		150		150		150	MHz
t _W Pulse duration	LE high		†		3.3		3.3		3.3		20	
	CLK high or low		†		3.3		3.3		3.3		ns	
		Data before CLK↑		†		1.3		1.3		1.2		
1.	Cotup timo	Setup time Data before LE↓	CLK high	†		1.2		1.1		1.1		ns
t _{su}	Setup time		CLK low	†		1.8		1.5		1.5		
		CLKEN before CLF	₹ ↑	†		0.7		0.7		0.8		
		Data after CLK↑		†		1.5		1.8		1.5		
 	Hold time	Hold time ■ Data after LF↓ ■ ■ ■	CLK high	†		1.6		1.9		1.6		ns
t _h	Holu lille		CLK low	†		1.2		1.6		1.3		
		CLKEN after CLK1		†		1.4		1.7		1.4		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B	B or A		†	1	5.1		4.7	1	4	
t _{pd}	LEAB or LEBA	A or D		†	1	5.9		5.5	1	4.8	ns
-	CLKAB or CLKBA	A or B		†	1	7.3		6.8	1.3	5.7	
t _{en}	OEAB or OEBA	A or B		†	1	6.5		6.3	1.1	5.2	ns
t _{dis}	OEAB or OEBA	A or B		†	1	5.1		4.7	1.2	4.4	ns

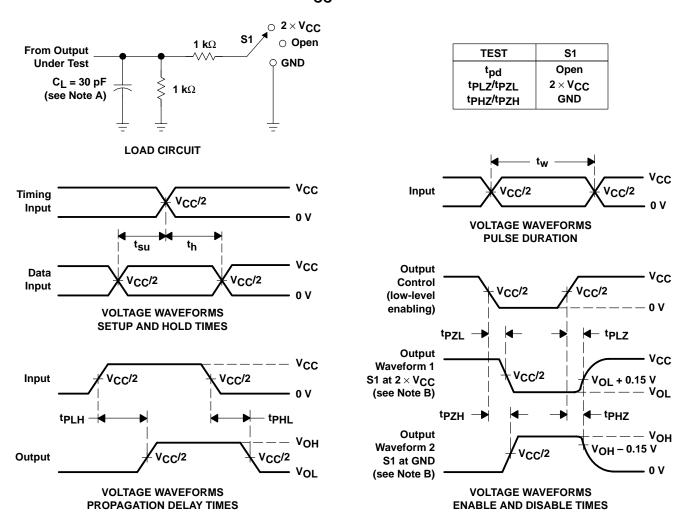
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	OIVII	
	Power dissipation	Outputs enabled	C _I = 50 pF, f = 10 MHz	†	43	56	ς.E
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pH}, f = 10 \text{ MHz}$	†	6	6	pF

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

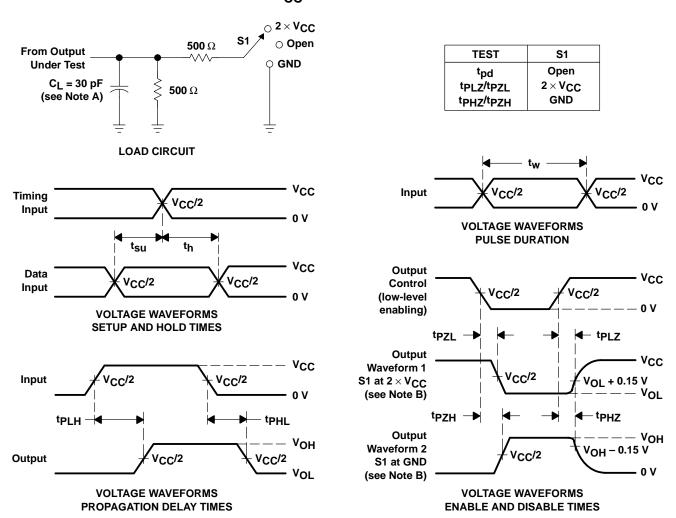


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

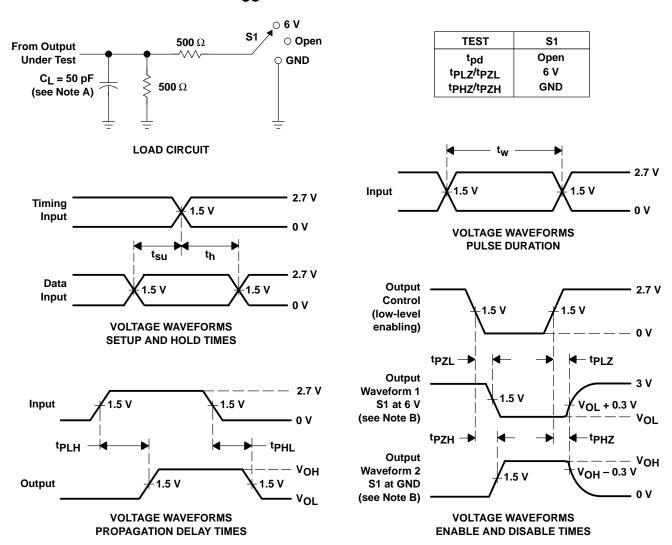


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

OEAB [

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56 CLKENAB

- Member of the Texas Instruments Widebus™ Family
- UBT[™] (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, Clocked, or Clock-Enabled Mode
- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in <u>each</u> direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the

55 TCLKAB LEAB []2 А1 Пз 54 **∏** B1 GND 4 53 | GND A2 🛮 5 52 **∏** B2 A3 🛮 6 51 B3 V_{CC} **□**7 50 🛮 V_{CC} A4 **∏**8 49 П в4 48 🛮 B5 A5 🛮 9 A6 🛮 10 47 🛮 B6 GND 11 46 [] GND A7 🛮 12 45 ∏ B7 A8 **∏** 13 44 **∏** B8 A9 🛮 14 43 **∏** B9 A10 🛮 15 42 B10 A11 ∏ 16 41 **∏** B11 A12 [] 17 40 | B12 GND ∏18 39 🛮 GND 38 **П** В13 A13 ∏ 19 A14 🛮 20 37 **∏** B14 A15 21 36 🛮 B15 V_{CC} **□** 22 35 V_{CC} A16 23 34 🛮 B16 A17 🛮 24 33 🛮 B17 GND II 25 32 **[]** GND A18 **∏** 26 31 **∏** B18 <u>OEBA</u> **[**] 27 30 CLKBA LEBA 28 29 CLKENBA

clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16601 is characterized for operation from -40°C to 85°C.

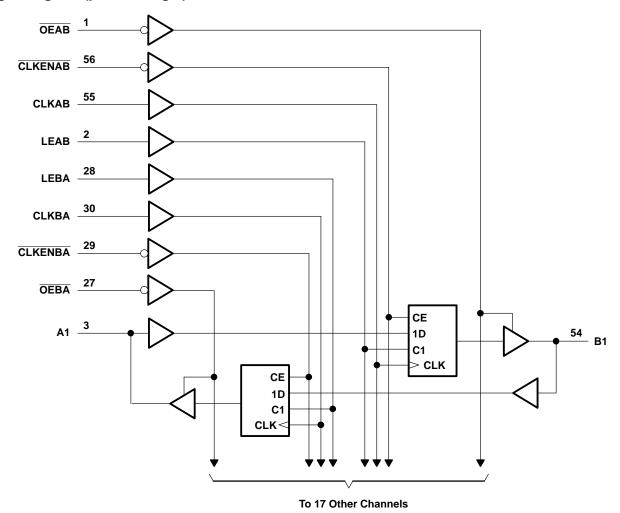
date.

FUNCTION TABLE†

	I	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Χ	Z
Х	L	Н	Χ	L	L
Х	L	Н	Χ	Н	Н
Н	L	L	Χ	Χ	в ₀ ‡ в ₀ ‡
н	L	L	X	Χ	в ₀ ‡
L	L	L	\uparrow	L	L
L	L	L	\uparrow	Н	Н
L	L	L	L or H	Χ	в ₀ ‡

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established

SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage	•	0	Vcc	V
۷o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
Land	I limb lavel autout avenue	V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
Les	Laveland autant amand	V _{CC} = 2.3 V		12],
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate	<u>. </u>		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	VCC-0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
VOL	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V
VOL	I _{OL} = 12 mA	2.3 V			0.7	V
	IOL = 12 IIIA	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	$V_{I} = 0.8 \text{ V}$	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δl _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4		pF
C _{iO} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency				†		150		150		150	MHz	
, Pulse		LE high		†		3.3		3.3		3.3		ns
t _W	duration	CLK high or low		†		3.3		3.3		3.3		115
		Data before CLK↑		†		2.3		2.4		2.1		
	Cotup timo	Setup time Data before LE↓	CLK high	†		2		1.6		1.6		20
t _{su}	Setup time	Data before LE↓	CLK low	†		1.3		1.2		1.1		ns
		CLKEN before CLK↑		†		2		2		1.7		
		Data after CLK↑		†		0.7		0.7		0.8		
4.	I lold time	Hold time Data after LE↓	CLK high	†		1.3		1.6		1.4		
^t h	noia iime		CLK low	†		1.7		2		1.7		ns
		CLKEN after CLK↑		†		0.3		0.5		0.6		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(IIVI O1)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B	B or A		†	1	4		4.6		4.1	
t _{pd}	LEAB or LEBA	A or D		†	1	4.6		5.3		4.7	ns
	CLKAB or CLKBA	A or B		†	1.2	5.2		5.8		5	
t _{en}	OEAB or OEBA	A or B		†	1.1	5.3		6.1		5.2	ns
t _{dis}	OEAB or OEBA	A or B		†	1.4	4.9		4.8		4.4	ns

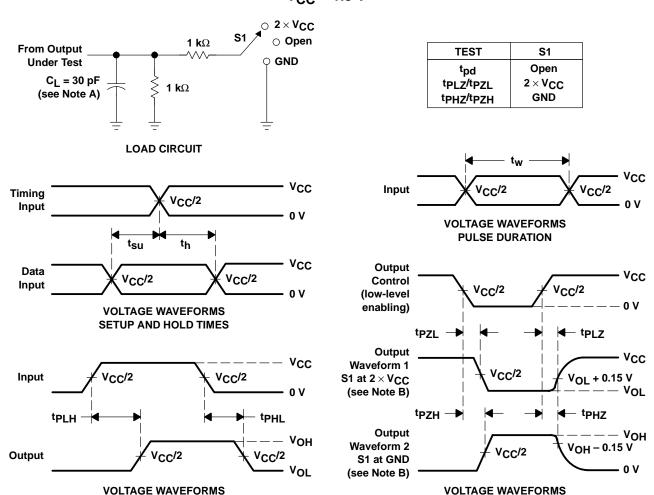
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
PARAMETER			1E31 CONDITIONS	TYP	TYP	TYP	ONIT
	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	41	52	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	6	6	l be

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

ENABLE AND DISABLE TIMES

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

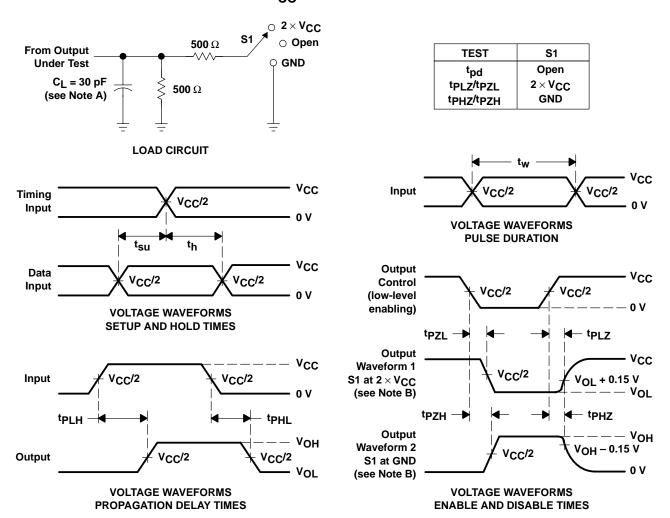
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

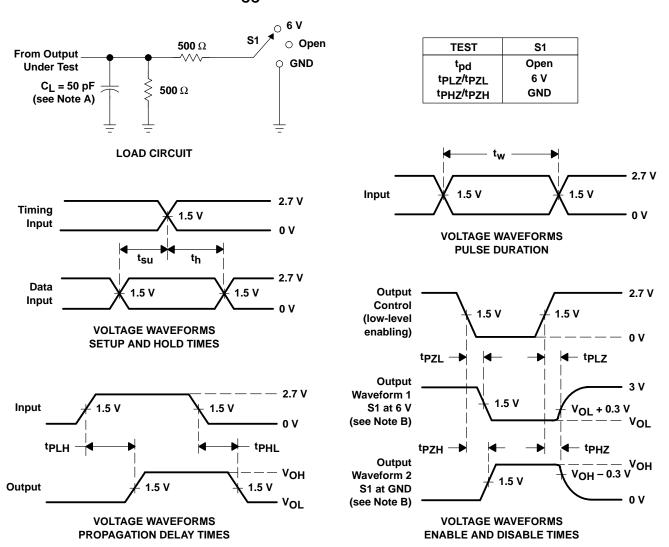


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq 2 \ ns$, $t_f \leq 2 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES032E-JULY 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

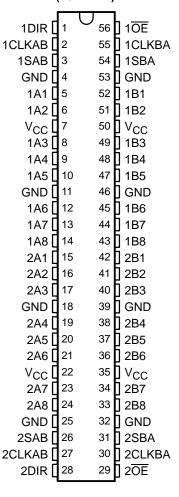
description

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either

DGG, DGV, OR DL PACKAGE (TOP VIEW)



register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16646 is characterized for operation from –40°C to 85°C.

TEXAS INSTRUMENTS

SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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FUNCTION TABLE

		INP	UTS			DATA	\ I/Os	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
Х	Х	1	Х	Χ	Χ	Input	Unspecified [†]	Store A, B unspecified [†]
Х	Χ	Χ	1	Χ	Χ	Unspecified†	Input	Store B, A unspecified [†]
Н	Χ	1	1	Χ	Χ	Input	Input	Store A and B data
Н	Χ	H or L	H or L	Χ	Χ	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	Χ	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	X	Н	Χ	Input	Output	Stored A data to B bus

[†] The data-output functions may be enabled or disabled by various signals at $\overline{\text{OE}}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



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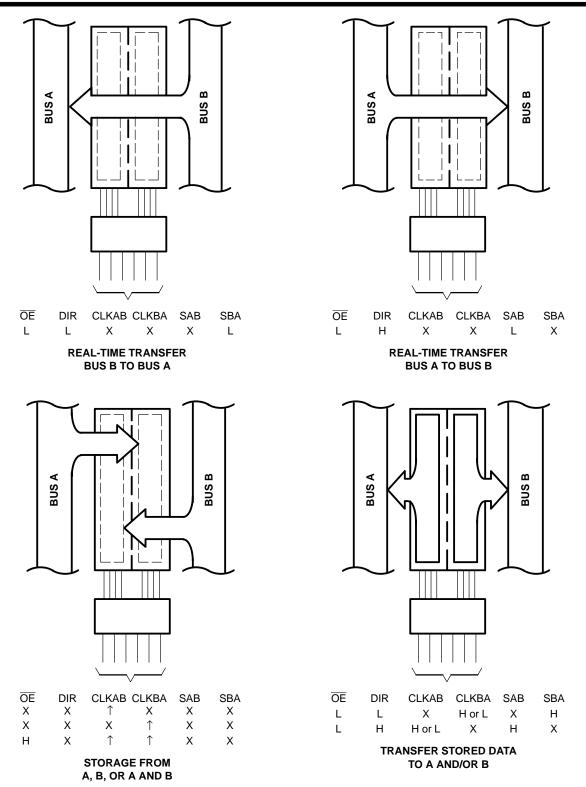
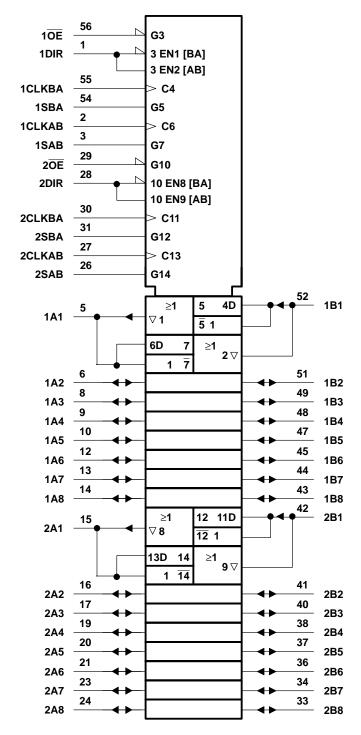


Figure 1. Bus-Management Functions



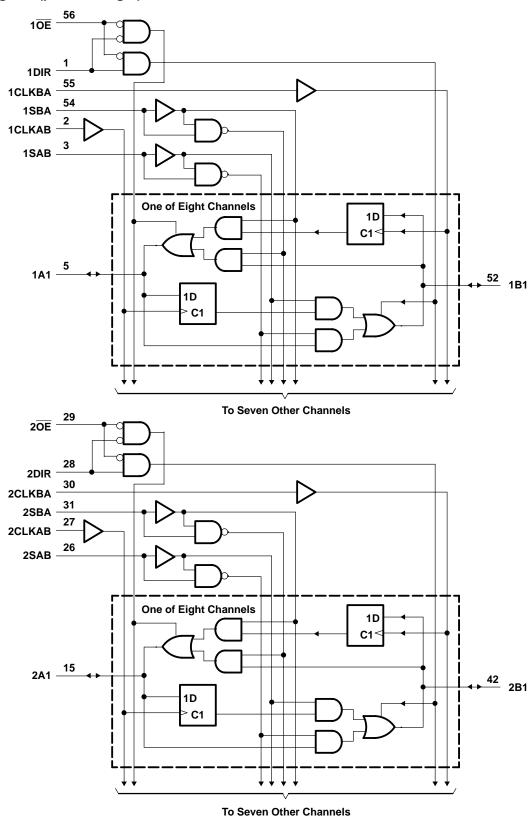
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V_{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High level autout avenue	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
1	Lavidaval autout avenue	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$		2.3 V	2			
Vон				2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24 \text{ mA}$	3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		loι – 12 mΔ		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
l _{OZ} §		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC			Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

				V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			P		150		150		150	MHz
t _W	Pulse duration	CLKAB or CLKBA high or low	¶		3.3		3.3		3.3		ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	¶		1.6		1.7		1.4		ns
th	Hold time	A after CLKAB↑ or B after CLKBA↑	¶		0.6		0.4		0.7		ns

 $[\]P$ This information was not available at the time of publication.

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B	B or A		†	1	4.8		4.5	1	3.9	
t _{pd}	CLKAB or CLKBA	A or B		†	1	5.6		5.2	1	4.5	ns
	SAB or SBA	AUIB		†	1	6.8		6.4	1	5.3	
t _{en}	ŌĒ	A or B		†	1	6.5		6.2	1	5.1	ns
t _{dis}	ŌĒ	A or B		†	1.6	5.7		5	1.4	4.7	ns
t _{en}	DIR	A or B		†	1	7.8		6.2	1	5.1	ns
t _{dis}	DIR	A or B		†	1.5	6.5		6	1.1	5.3	ns

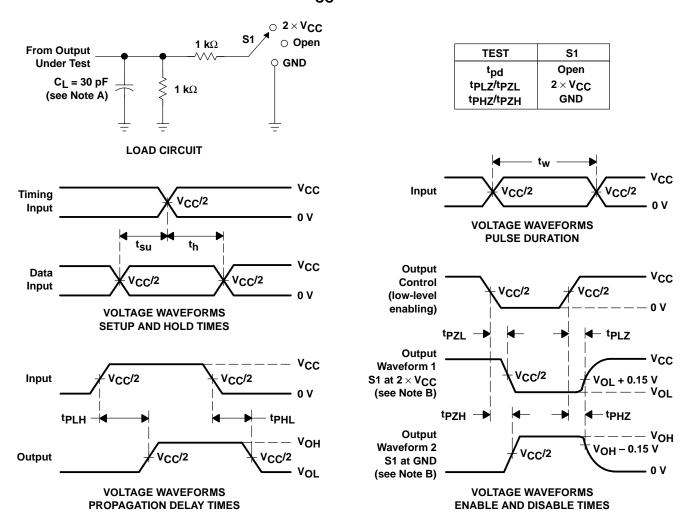
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
PARAMETER			TEST CONDITIONS	TYP	TYP	TYP	ONII
<u> </u>	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	39	43	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pH}, f = 10 \text{ MHz}$	†	10	12	ρг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



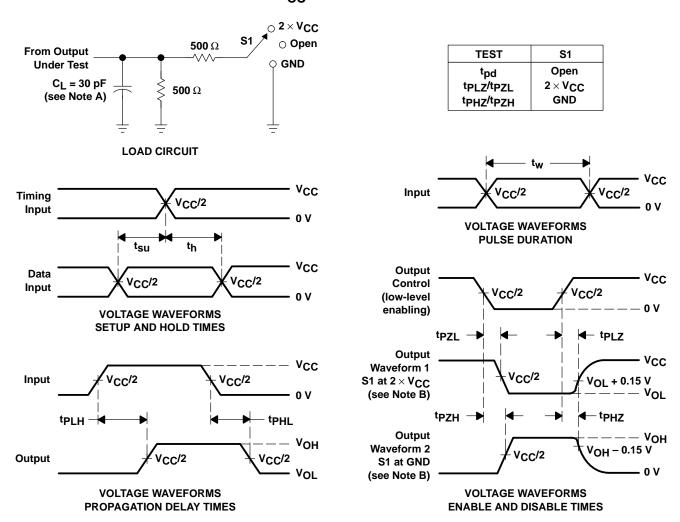
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



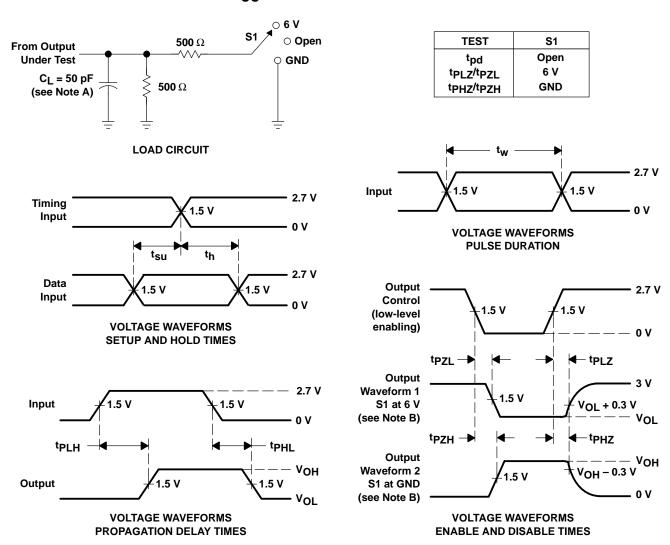
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 4. Load Circuit and Voltage Waveforms

SN74ALVCH16652 **16-BIT BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS

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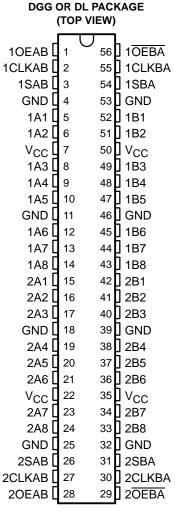
- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink **Small-Outline (DGG) Packages**

description

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16652.



Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are in the high-impedance state, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused for floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, OEBA should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking current-sourcing capability of the driver.

The SN74ALVCH16652 is characterized for operation from –40°C to 85°C.

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SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES034A - JULY 1995 - REVISED FEBRUARY 1999

FUNCTION TABLE

		INPU	TS			DATA	\	OPERATION OR
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1-B8	FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	\uparrow	\uparrow	Χ	Χ	Input	Input	Store A and B data
Х	Н	\uparrow	H or L	Χ	X	Input	Unspecified [‡]	Store A, hold B
Н	Н	\uparrow	\uparrow	X [‡]	X	Input	Output	Store A in both registers
L	Χ	H or L	\uparrow	Χ	X	Unspecified [‡]	Input	Hold A, store B
L	L	\uparrow	\uparrow	Χ	X‡	Output	Input	Store B in both registers
L	L	Χ	Χ	Χ	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	Χ	Н	Output	Input	Stored B data to A bus
Н	Н	Χ	Χ	L	X	Input	Output	Real-time A data to B bus
Н	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



[‡] Select control = L; clocks can occur simultaneously Select control = H; clocks must be staggered in order to load both registers

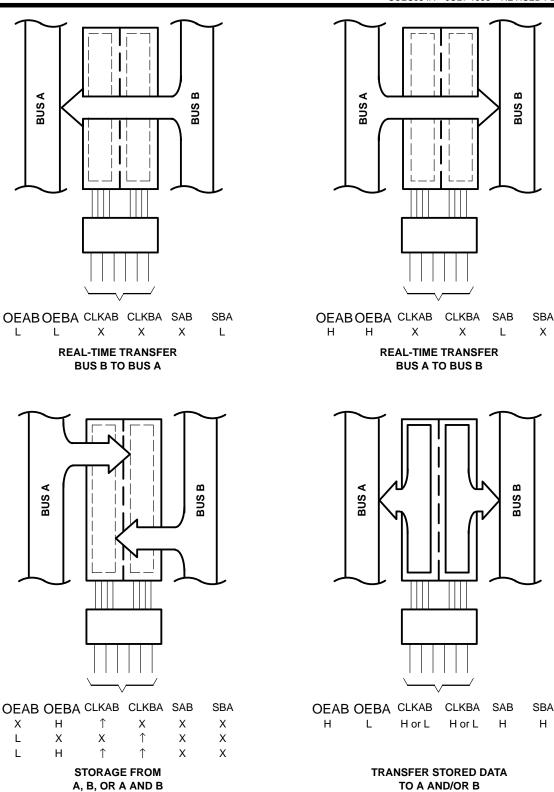


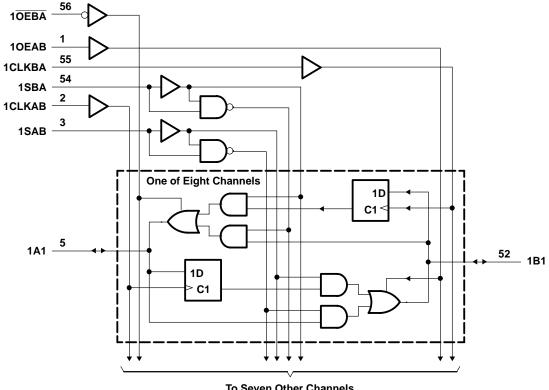
Figure 1. Bus-Management Functions



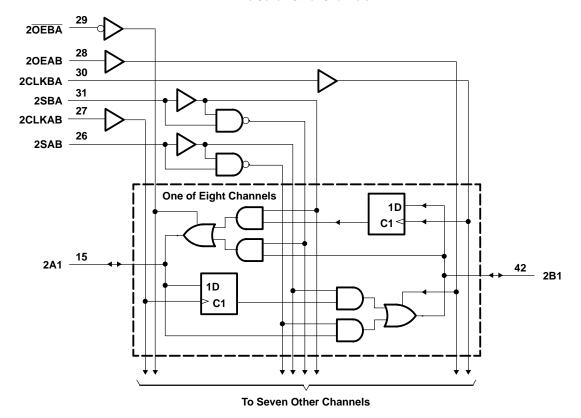
56 10EBA EN1 [BA] 1 10EAB EN2 [AB] 55 1CLKBA > C3 54 1SBA G4 2 1CLKAB > C5 3 1SAB G6 29 20EBA **EN7** [BA] 28 20EAB **EN8 [AB]** 30 2CLKBA > **C9** 31 2SBA G10 27 2CLKAB > C11 26 2SAB G12 1B1 ≥ 1 3D 1A1 4 1 5D 6 51 6 1B2 1A2 49 8 1A3 1B3 9 48 1A4 1B4 10 47 1A5 1B5 45 12 1A6 1B6 44 13 1A7 1B7 14 43 1B8 1A8 42 15 10 9D 2B1 2A1 10 1 11D 12 12 16 41 2B2 2A2 40 17 2A3 2B3 19 38 2B4 2A4 37 20 2A5 2B5 21 36 2A6 2B6 23 34 2A7 2B7 24 33 2A8 2B8

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)









SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Output-voltage range, VO (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	
Storage temperature range, T _{stq}	—65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vсс	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ı	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
	High level output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
IOL	Low-level output current	V _{CC} = 2.7 V		12	MA
	V _{IH} High-level input voltage V _{IL} Low-level input voltage V _I Input voltage V _O Output voltage I _{OH} High-level output current	V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETI	R TEST CONDITIO	NS V _{CC}	MIN	TYP [†]	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	VCC-0	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	$I_{OL} = 100 \mu A$	1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V			0.45	
Vo.	I _{OL} = 6 mA	2.3 V			0.4	V
VOL	lo 12 m/	2.3 V			0.7	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
l _l (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
∆lcc	One input at V _{CC} – 0.6 V, Other in	nputs at V _{CC} or GND 3 V to 3.6 V			750	μΑ
C _i Contro	inputs $V_I = V_{CC}$ or GND	3.3 V				pF
C _{io} A or B	orts $V_O = V_{CC}$ or GND	3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

		V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency									MHz
t _W	Pulse duration, CLK high or low									ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑									ns
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑								·	ns

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\$}$ For I/O ports, the parameter $\mbox{I}_{\mbox{OZ}}$ includes the input leakage current.

SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
	A or B	B or A									
tpd	CLKAB or CLKBA	A or B									ns
	SAB or SBA	B or A									
t _{en}	OE or OE	A or B									ns
t _{dis}	OE or OE	A or B									ns

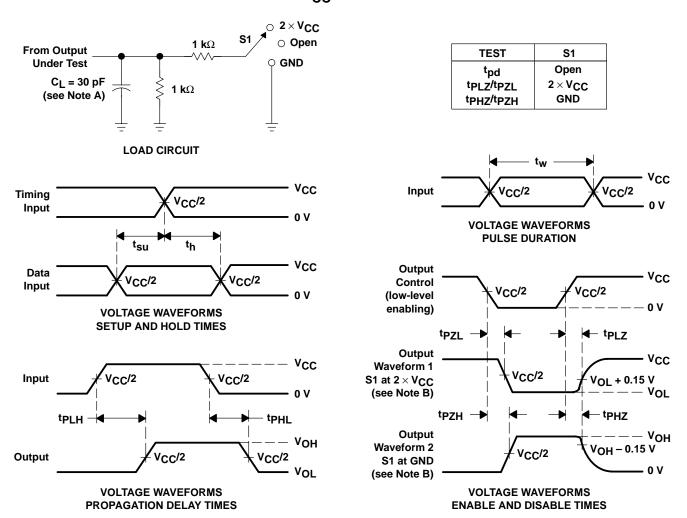
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V	UNIT
C .	Power dissipation capacitance	Outputs enabled	f 40 MHz				pF
Cpd	per transceiver	Outputs disabled	f = 10 MHz				pΕ



PRODUCT PREVIEW

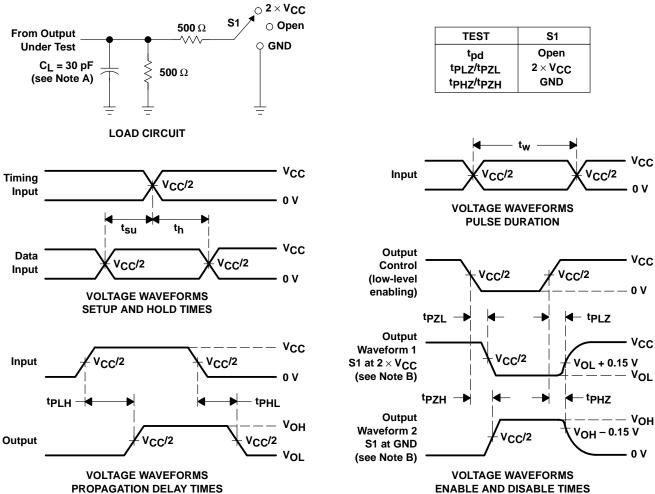
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

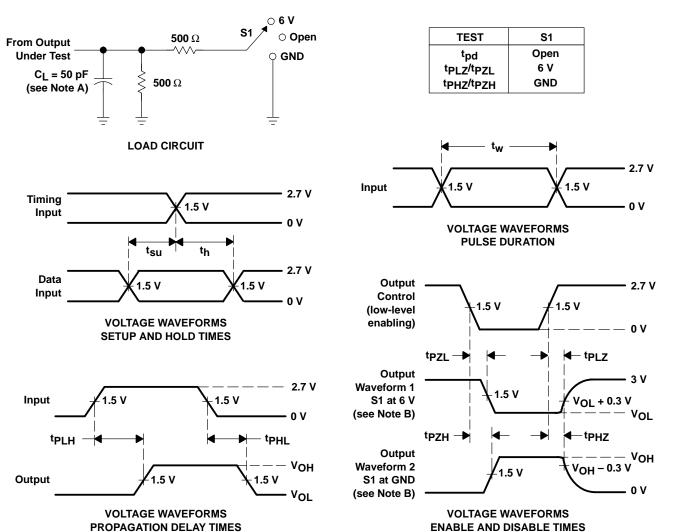


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PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 4. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

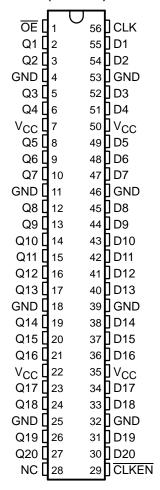
description

This 20-bit flip-flop is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The 20 flip-flops of the SN74ALVCH16721 are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (\overline{OE}) input places the 20 outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16721 is characterized for operation from –40°C to 85°C.

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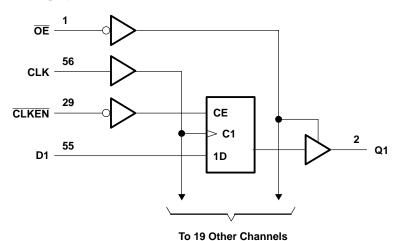
testing of all parameters.

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FUNCTION TABLE (each flip-flop)

	INPU	JTS		OUTPUT
OE	CLKEN	CLK	D	Q
L	Н	Х	Χ	Q ₀
L	L	\uparrow	Н	Н
L	L	\uparrow	L	L
L	L	L or H	Χ	Q_0
Н	Х	Х	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		. –0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5	V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		_65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ı	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
	V _O Output voltage	V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-12	mA
ЮН		V _{CC} = 2.7 V		-12	IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
IOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
	OH High-level output current OL Low-level output current \textstyle \textst	V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	VCC-0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
V		I _{OL} = 6 mA	2.3 V			0.4	V
VOL		la. 12 mA	2.3 V			0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
lį		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V [‡]	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5		pF
Co	Data inputs Outputs	$V_O = V_{CC}$ or GND	3.3 V		6 7		pF
+ 4117		VO = VCC 01 GND	J.5 v		'		Pı

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency			§		150		150		150	MHz
t _W	Pulse duration, CLK high or low		§		3.3		3.3		3.3		ns
	Catua tima	Data before CLK↑	§		4		3.6		3.1		20
t _{su}	Setup time	CLKEN before CLK↑	§		3.4		3.1		2.7		ns
4.	I Hald Co.	Data after CLK↑	§		0		0		0		
th	Hold time	CLKEN after CLK↑	§		0		0		0		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001101)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	5.6	1	5.1	1	4.3	ns
t _{en}	ŌĒ	Q		†	1	6.1	1	5.8	1	4.8	ns
^t dis	ŌĒ	Q		†	1	5.5	1	4.7	1	4.4	ns

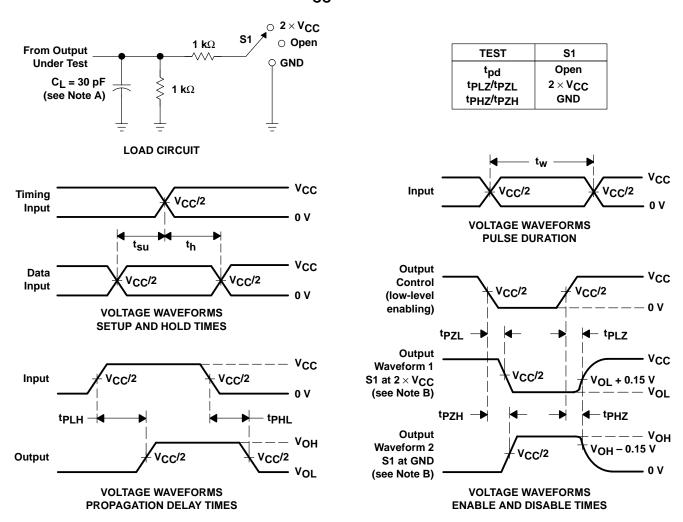
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FANAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONIT
	Power dissipation	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	†	55	59	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	46	49	ρг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

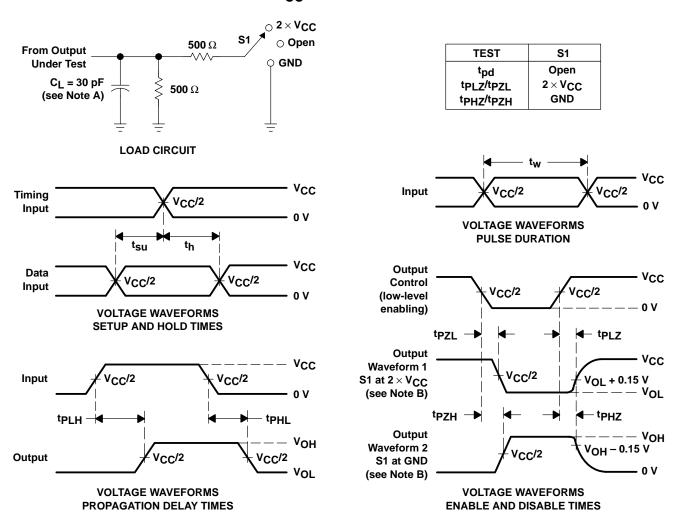


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

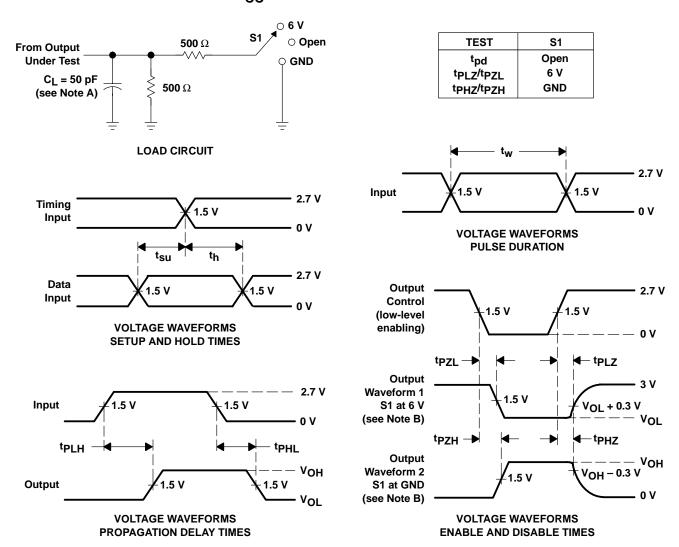


NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

DGG OR DL PACKAGE

SCES035E - JULY 1995 - REVISED FEBRUARY 1999

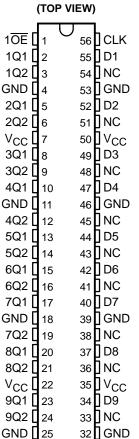
- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 10-bit flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The flip-flops of the SN74ALVCH16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.



NC - No internal connection

31 D10

30 NC

29 NC

10Q1 **[**] 26

10Q2 [] 27

20E | 28

OE input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16820 is characterized for operation from -40°C to 85°C.

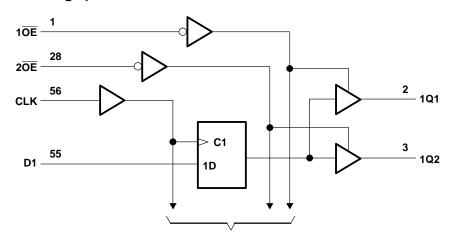
TEXAS INSTRUMENTS

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE _n †	CLK	D	q _n t
L	1	Η	Н
L	\uparrow	L	L
L	L	Χ	Q_0
Н	Χ	Χ	Z

† n = 1, 2

logic diagram (positive logic)



To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{IK}(V_I < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES035E – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
	USah Israel and and annual	V _{CC} = 2.3 V		-12	A	
ІОН	nigh-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA	
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	m 1	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA	$I_{OH} = -6 \text{ mA}$					
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\/ - ·		I _{OL} = 6 mA		2.3 V			0.4	V
VOL		1- 40 m A		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V			0.4	
l _l		I _{OL} = 24 mA	3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-4 5			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	- 75			
		$V_I = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	VI – Voc or CND		221/		3.5		n.E
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		1.7		1.8		1.4		ns
t _h	Hold time, data after CLK↑	§		1.1		1.1		1		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	5.9		5.5	1	4.8	ns
t _{en}	ŌĒ	Q		†	1	6.4		6.1	1	5	ns
^t dis	ŌĒ	Q		†	1	5.7		5	1	4.5	ns

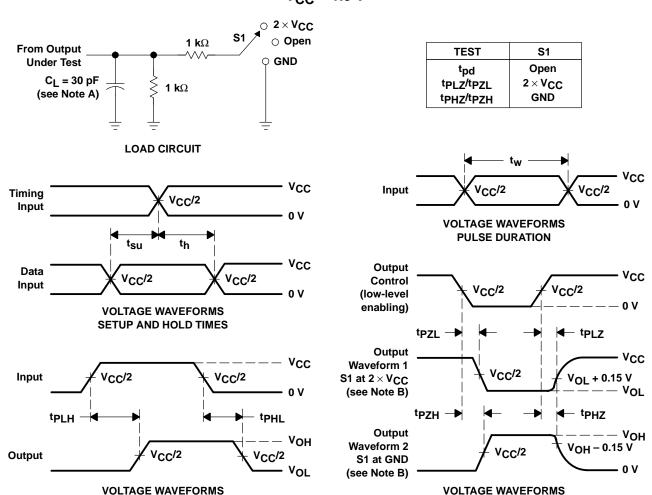
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETE	:D	TEST CONDITION	٠	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAMETE		TEST CONDITIONS -	TYP	TYP	TYP	ONIT	
<u> </u>	Power dissipation	All outputs enabled	C ₁ = 50 pF. f = 10	\1LI-	†	60	63	pF
Cpd	capacitance	All outputs disabled	$C_L = 50 \text{ pF}, f = 10$	VIIIZ	†	38	46	рг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

ENABLE AND DISABLE TIMES

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

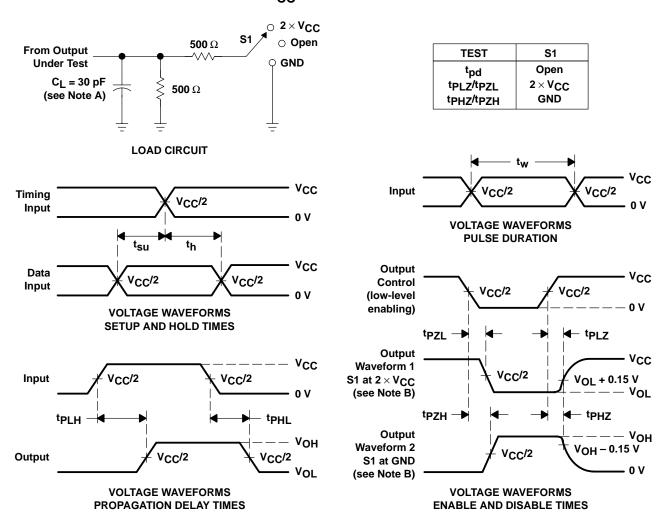
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



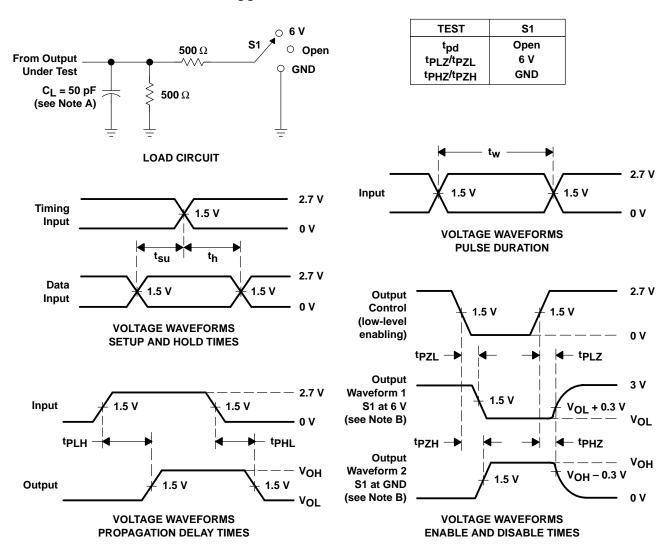
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES037C - JULY 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

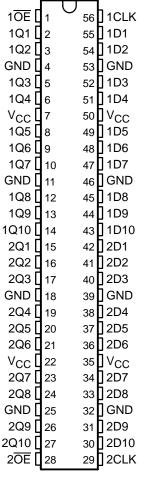
description

This 20-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

DGG OR DL PACKAGE (TOP VIEW)



OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

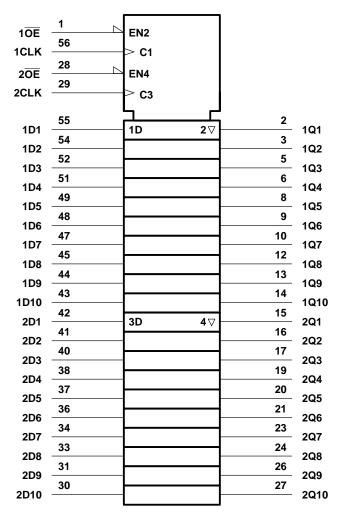
The SN74ALVCH16821 is characterized for operation from –40°C to 85°C.

TEXAS INSTRUMENTS

FUNCTION TABLE (each 10-bit flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	↑	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	X	Χ	Z

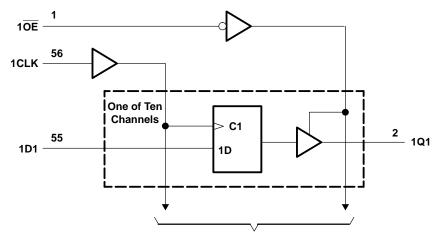
logic symbol†



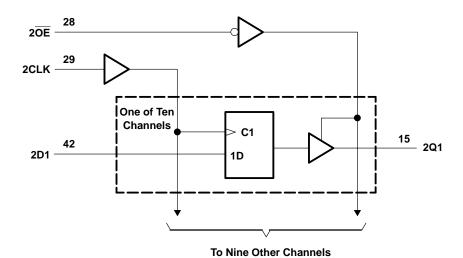
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



To Nine Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037C – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	mA
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP† N	ИΑХ	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.2	2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
VOH		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 4 mA	1.65 V		(0.45	
Vo	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V
VOL	I.a. 12 mA	2.3 V			0.7	V
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V		(0.55	
I _I	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±	500	
loz	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔICC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
Control inputs	V. Vocar CND	221/		3.5		~F
C _i Data inputs	V _I = V _{CC} or GND	3.3 V	6			pF
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		4.4		3.9		3.4		ns
th	Hold time, data after CLK↑	§		0		0		0		ns

[§] This information was not available at the time of publication.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
^t pd	CLK	Q		†	1	5.8		5.3	1	4.5	ns
t _{en}	ŌĒ	Q		†	1	6.6		6.2	1	5.1	ns
t _{dis}	ŌĒ	Q		†	1	5.7		5	1	4.6	ns

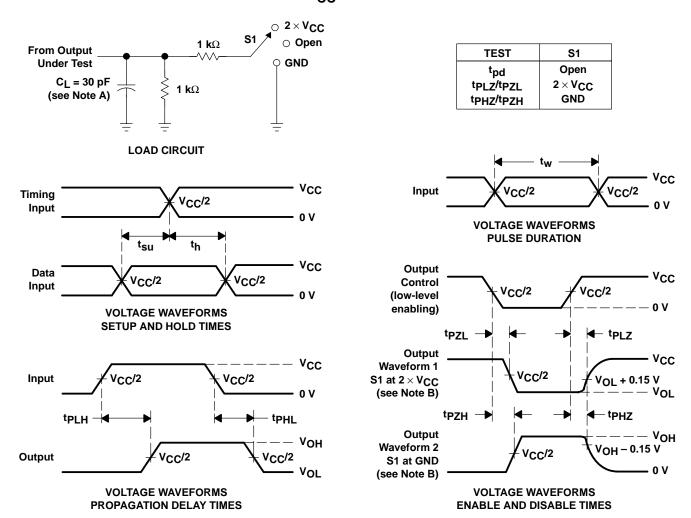
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} = 3.3 V	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	36	40	PΓ
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	22	24	ρг

[†]This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

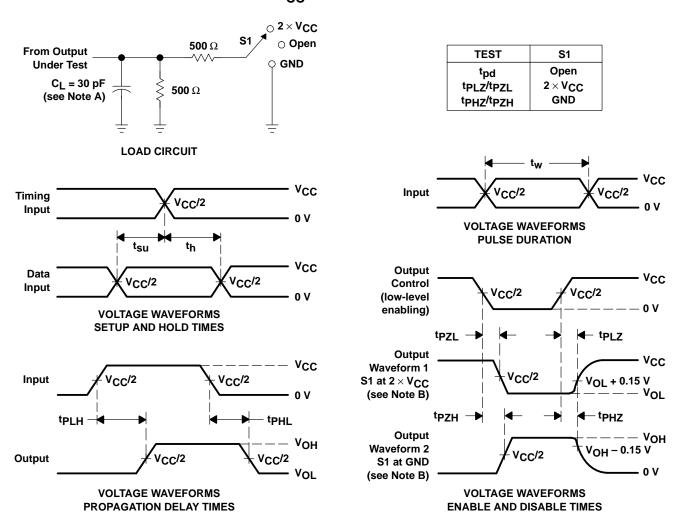


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



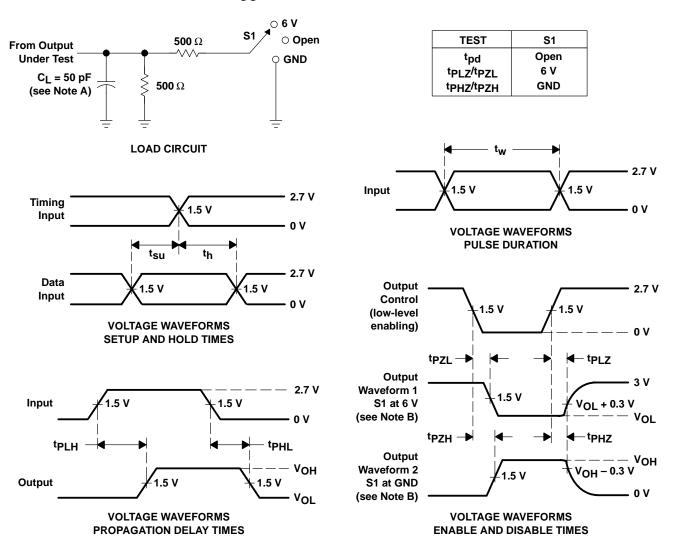
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES038D - JULY 1995 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus ™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

1CLR 56 ¶ 1CLK 1OE 2 55 1 1 CLKEN 1Q1 🛮 3 54 🛮 1D1 GND ∏4 53 **∏** GND 1Q2 **[**] 5 52 ¶ 1D2 1Q3 **[**] 6 51 **∏** 1D3 V_{CC} \square 7 50 VCC 1Q4 🛮 8 49**∏**1D4 1Q5 **∏** 9 48**∏**1D5 1Q6 🛮 10 47 1D6 GND [] 11 46 GND 1Q7 Π 12 45 🛮 1D7 44**∏**1D8 1Q8 📙 13 1Q9 **1**14 43**∏**1D9

42 1 2D1

41 2D2

30 2 CLKEN

29 1 2CLK

DGG OR DL PACKAGE

(TOP VIEW)

40 2D3 2Q3 **∏** 17 GND [39 **[]** GND 18 2Q4 🛮 19 38 2D4 2Q5 🛮 20 37 2D5 2Q6 **∏**21 36**∏**2D6 V_{CC} 1 22 35 V_{CC} 2Q7 **[**] 23 34 🛮 2D7 2Q8 🛮 24 33 **1** 2D8 GND 25 32 GND 2Q9 **[**] 26 31 1 2D9

2Q1 Π

2Q2 16

20E **1**27

15

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V_{CC}}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

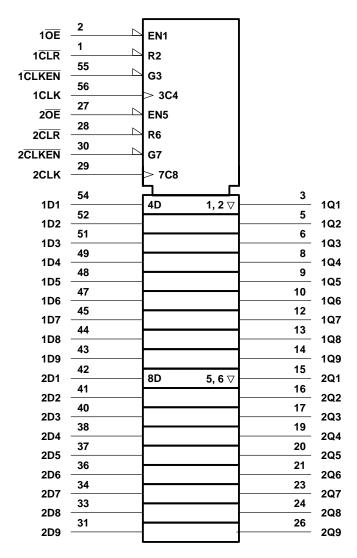
The SN74ALVCH16823 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLE (each 9-bit flip-flop)

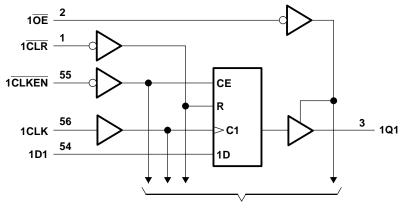
	INPUTS					
OE	CLR	CLKEN	CLK	D	Q	
L	L	Х	Χ	Χ	L	
L	Н	L	\uparrow	Н	Н	
L	Н	L	\uparrow	L	L	
L	Н	L	L	Χ	Q_0	
L	Н	Н	Χ	Χ	Q_0	
Н	Χ	X	Χ	Χ	Z	

logic symbol†

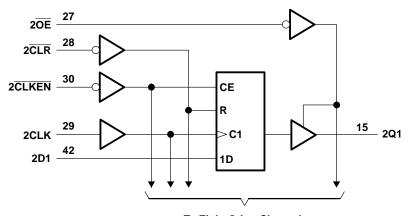


 $[\]dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Eight Other Channels



To Eight Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to $V_{\mbox{\footnotesize CC}}$ + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES038D - JULY 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage	0	VCC	V	
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High-level output current	V _{CC} = 2.3 V		-12	A
ЮН		$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V	12 12		m 1
loL	Low-level output current	$V_{CC} = 2.7 \text{ V}$			mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CO	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$		2.3 V	2				
Vон				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 4 \text{ mA}$		1.65 V			0.45		
\/~.		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V		
VOL		Jan. 12 mA		2.3 V			0.7	V	
		I_{OL} = 12 mA	2.7 V			0.4			
		I _{OL} = 24 mA	3 V			0.55			
II		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		V _I = 0.7 V	2.3 V	45			μА		
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45					
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μΑ	
lcc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	ol inputs		3.3 V		4.5		~F	
Ci	Data inputs	$V_I = V_{CC}$ or GND		3.3 v		6.5		pF	
C _o C	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	VCC =	2.5 V	VCC =	2.7 V	V _{CC} =		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency			†		150		150		150	MHz	
	Pulse duration	CLR low	†		3.3		3.3		3.3		ns	
t _W	Puise duration	CLK high or low	†		3.3		3.3		3.3		115	
	Cation times	CLR inactive	†		0.7		0.7		0.8			
١.		Data low before CLK↑	†		1.6		1.6		1.3		ns	
t _{su}	Setup time	Data high before CLK↑	†		1.1		1.1		1			
		CLKEN low before CLK↑	†		1.9		1.9		1.5			
		Data low after CLK↑	†		0.5		0.5		0.5			
t _h	Hold time	Data high after CLK↑	†		0.1		0.1		0.8		ns	
		CLKEN low after CLK↑	†		0.3		0.3		0.4			

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(IIVFOT)	(OUTFUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
4 .	CLK	Q		†	1	5.8		5.2	1	4.5	no
^t pd	CLR	y		†	1	5.4		5.2	1.2	4.6	ns
t _{en}	ŌĒ	Q		†	1	6		5.7	1	4.8	ns
^t dis	ŌĒ	Q		†	1.1	5.4		4.7	1.3	4.5	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
PARAMETER			TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	Power dissipation	Outputs enabled	C. 50 pF f 40 MU =	†	27	30	۲	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, \qquad f = 10 \text{ MHz}$	†	16	18	pF	

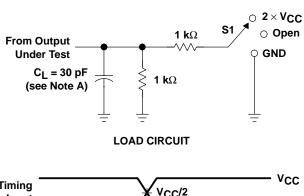
[†] This information was not available at the time of publication.

VCC

0 V

V_{CC}/2

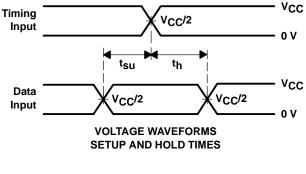
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

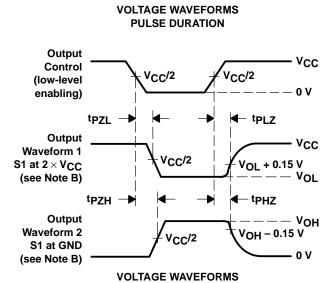


TEST	S 1
^t pd	Open
tpLZ/tpZL	2×V _{CC}
tpHZ/tpZH	GND

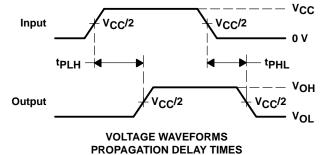
V_{CC}/2

Input





ENABLE AND DISABLE TIMES

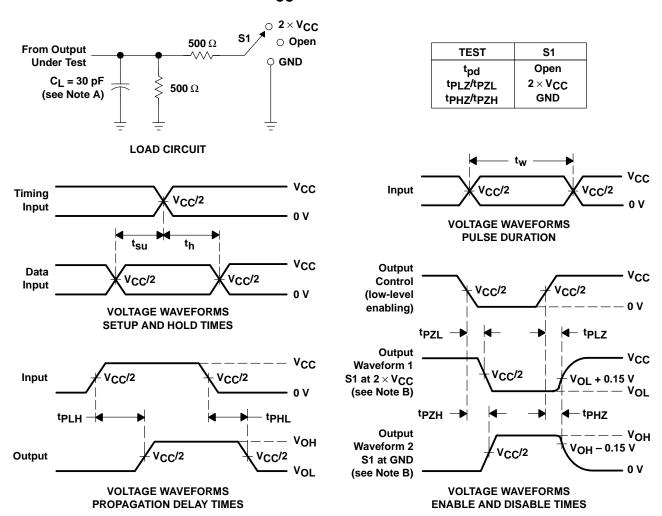


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

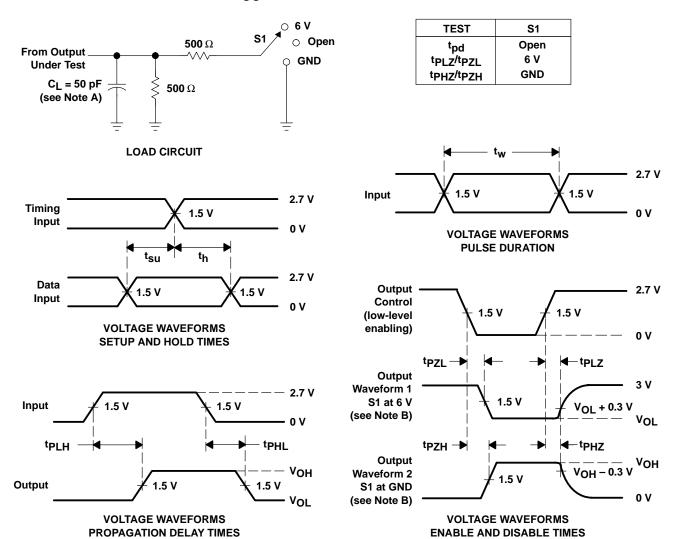


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

Member of the Texas Instruments Widebus™ Family

- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit buffer and line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

This SN74ALVCH16825 improves the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all nine affected outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)

			U		L	
1 <u>OE1</u>	Q	1	_	56	P	1 0E 2
1Y1		2		55	1	1A1
1Y2		3		54		1A2
GND		4		53	1	GND
1Y3		5		52		1A3
1Y4		6		51		1A4
V_{CC}		7		50		V_{CC}
1Y5		8		49		1A5
1Y6		9		48	1	1A6
1Y7		10		47	1	1A7
GND		11		46	1	GND
1Y8		12		45	1	1A8
1Y9		13		44		1A9
GND		14		43	1	GND
GND		15		42	1	GND
2Y1		16		41	•	2A1
2Y2		17		40	1	2A2
GND		18		39	1	GND
2Y3		19		38	1	2A3
2Y4		20		37		2A4
2Y5		21		36	þ	2A5
V_{CC}		22		35	1	V_{CC}
2Y6		23		34	1	2A6
2Y7		24		33	1	2A7
GND		25		32	•	GND
2Y8	D	26		31	þ	2A8
2Y9		27		30	þ	2A9
2OE1		28		29	þ	2OE2
					•	

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

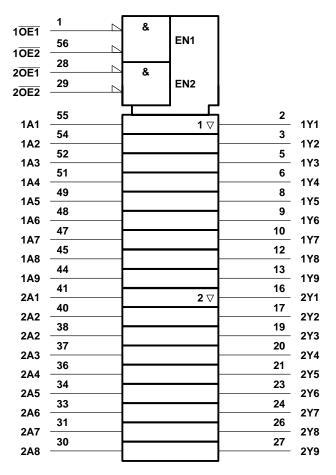
The SN74ALVCH16825 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 9-bit section)

	INPUTS	ОИТРИТ	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Χ	Z

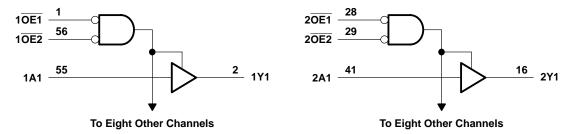
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logic symbol†



 $[\]dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
lau	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ЮН	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature	-40	85	°C		
	All 1 (1' (6) 1 1 1 (1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	L ()/ OND:				

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST COND	ITIONS	VCC	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$		2.3 V	2				
Vон				2.3 V	1.7			V	
		$I_{OH} = -12 \text{ mA}$		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		$I_{OL} = 100 \mu A$	1.65 V to 3.6 V			0.2			
		I _{OL} = 4 mA		1.65 V			0.45		
\/a:		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V	
VOL		I _{OL} = 12 mA		2.3 V			0.7	v	
		IOC = 12 IIIA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V	1.65 V	-25					
		V _I = 0.7 V		2.3 V	45				
I _I (hold)		V _I = 1.7 V		2.3 V	-4 5			μΑ	
, ,		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	- 75				
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND, I_O	= 0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V, Oth	her inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs			221/		3.5		nE.	
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		6		pF		
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = ± 0.2		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT	
	(1141 01)	(0011 01)	TYP	MIN	MAX	MIN MAX		MIN	MAX		
t _{pd}	Α	Y	§	1	4.1		3.9	1	3.4	ns	
t _{en}	ŌĒ	Υ	§	1	6		5.7	1	4.7	ns	
t _{dis}	ŌĒ	Υ	§	1.2	5.6		4.9	1.3	4.5	ns	

[§] This information was not available at the time of publication.



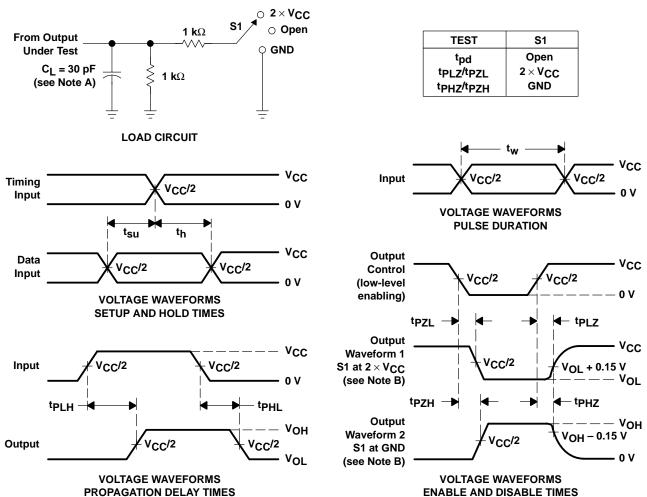
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
PARAMETER			1E31 CONDITIONS	TYP	TYP	TYP	ONIT	
<u> </u>	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	16	18		
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	6	pF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

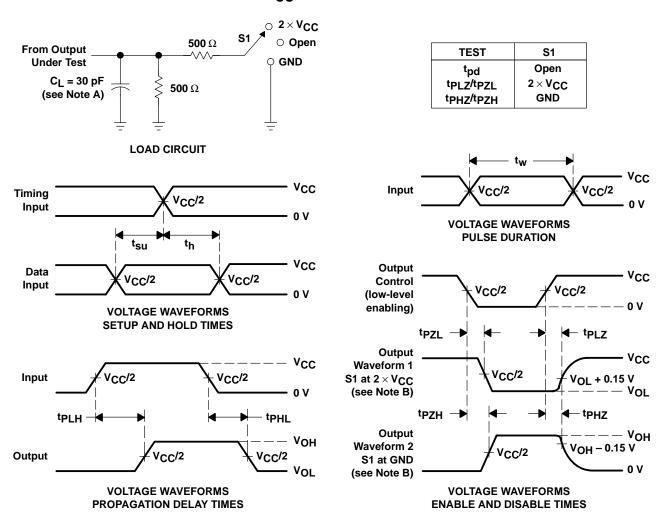


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

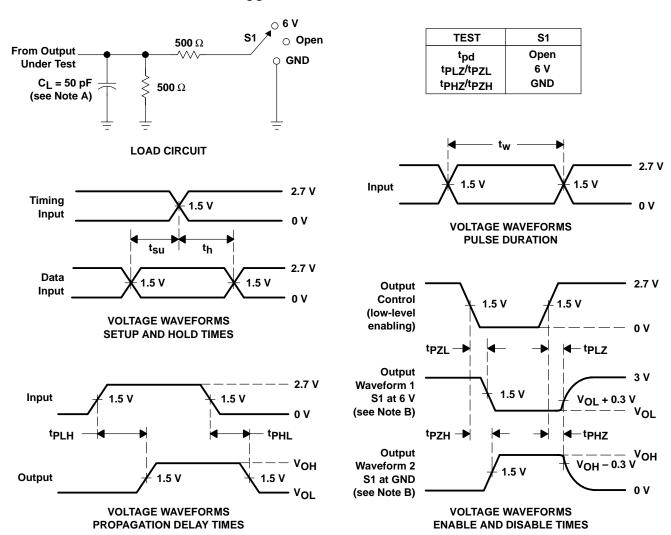


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus ™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit noninverting buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16827 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

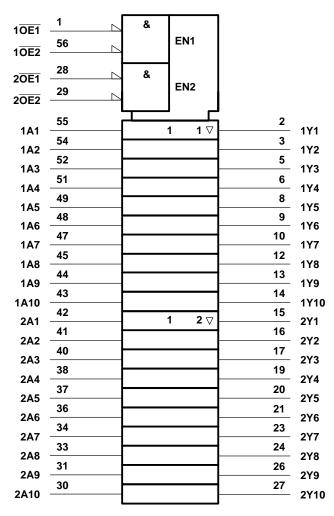
1		_		1	
1 <u>0E1</u> [1	\cup	56	b	1 OE 2
1Y1[2		55	Ь	1A1
1Y2[3		54		1A2
GND[4		53	D	GND
1Y3[5		52	D	1A3
1Y4[6		51		1A4
V _{CC} [7		50		V_{CC}
1Y5[8		49		1A5
1Y6[9		48		1A6
1Y7[10		47		1A7
GND[11		46		GND
1Y8[12		45		1A8
1Y9[13		44		1A9
1Y10[14		43		1A10
2Y1[15		42		2A1
2Y2[16		41		2A2
2Y3[17		40		2A3
GND[18		39		GND
2Y4[19		38		2A4
2Y5[20		37		2A5
2Y6	21		36	р	2A6
V _{CC} [22		35	р	V_{CC}
2Y7[23		34		2A7
2Y8[24		33		2A8
GND[25		32	р	GND
2Y9[26		31	0	2A9
2Y10	27		30	р	2A10
2 0E1 [28		29	p	2OE2

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FUNCTION TABLE (each 10-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Χ	Z

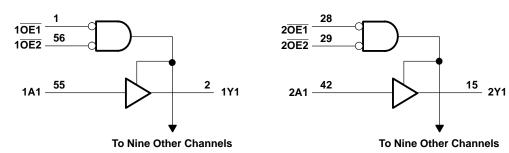
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High lovel output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	nign-ievei output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
	H High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low level output ourrent	V _{CC} = 2.3 V		12	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$	12		mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Voн				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\/		I _{OL} = 6 mA		2.3 V			0.4	V
VOL		1- 40 m A		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
Ιį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	V. Vaaar CND		221		3.5		~F
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF
Со	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTBUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	UT) (OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	Α	Υ	§	1	4.1		3.9	1	3.4	ns
t _{en}	ŌĒ	Υ	§	1	6		5.7	1	4.7	ns
^t dis	ŌĒ	Υ	§	1.2	5.6		4.9	1.3	4.5	ns

[§] This information was not available at the time of publication.



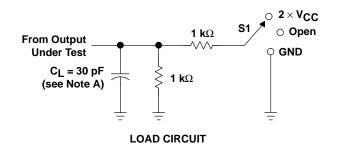
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

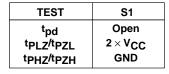
operating characteristics, $T_A = 25^{\circ}C$

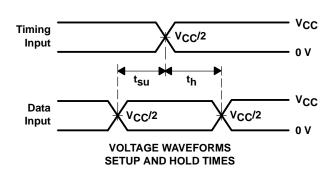
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TEST CONDITIONS	TYP	TYP	TYP	ONIT
	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	16	18	۲
Cpc	capacitance	Outputs disabled	$C_L = 50 \text{ pH}, f = 10 \text{ MHz}$	†	4	6	pF

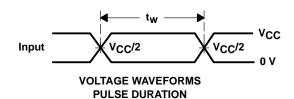
[†] This information was not available at the time of publication.

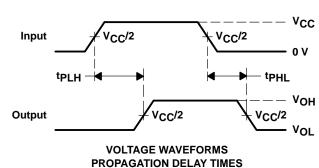
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

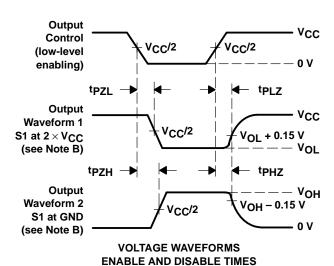










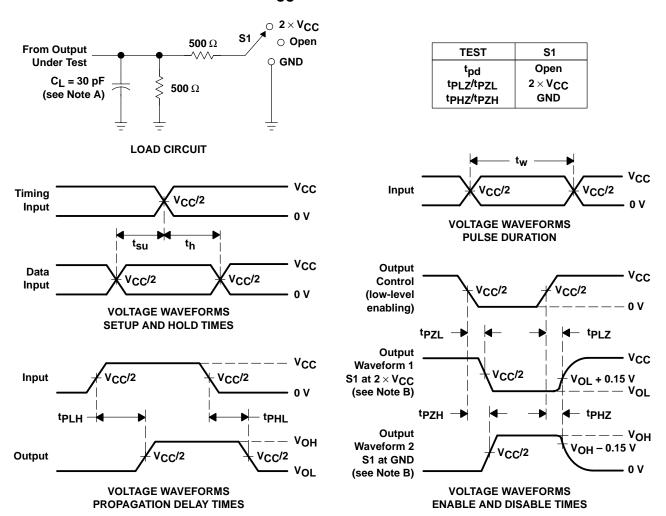


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



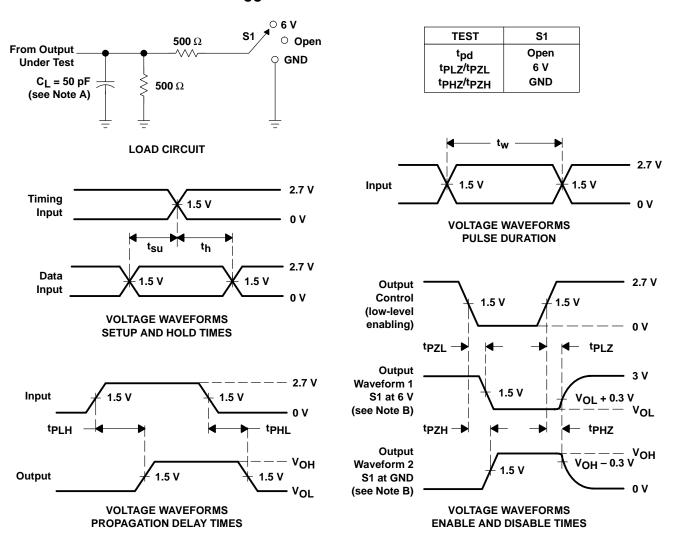
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit inverting buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16828 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16828 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

	- 1				1	
1 0E1	d	1	O	56	b	1 0 E2
1Y1		2		55	b	1A1
1Y2		3		54	b	1A2
GND		4		53	b	GND
1Y3		5		52	0	1A3
1Y4		6		51		1A4
V_{CC}		7		50	0	V_{CC}
1Y5		8		49		1A5
1Y6		9		48		1A6
1Y7		10		47		1A7
GND		11		46		GND
1Y8		12		45	D	1A8
1Y9		13		44		1A9
1Y10		14		43		1A10
2Y1		15		42	0	2A1
2Y2		16		41	0	2A2
2Y3		17		40		2A3
GND	Ц	18		39	0	GND
2Y4		19		38		2A4
2Y5		20		37	0	2A5
2Y6	Ц	21		36	р	2A6
V_{CC}	Ц	22		35	р	V_{CC}
2Y7		23		34	0	2A7
2Y8		24		33	р	2A8
GND		25		32	Ц	GND
2Y9		26		31	Ц	2A9
2Y10		27		30	Ц	2A10
2OE1	Ц	28		29	Ц	2OE2

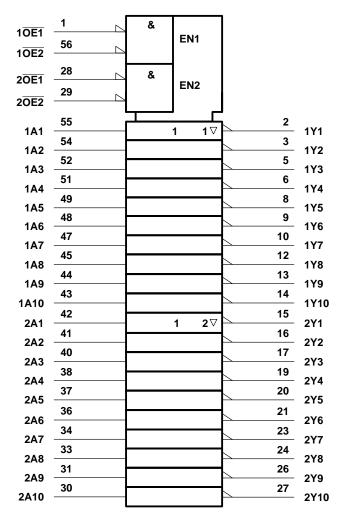
FUNCTION TABLE (each 10-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
Н	X	Χ	Z
Х	Н	Χ	Z

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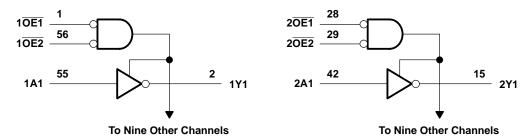


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{Stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
1	Lligh lovel output ourrant	V _{CC} = 2.3 V		-12	A
ЮН	riigii-ievei output current	V _{CC} = 2.7 V		-12	mA
	/IH High-level input voltage /IL Low-level input voltage /I Input voltage /O Output voltage OH High-level output current OL Low-level output current	V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
lai	Low lovel output ourront	V _{CC} = 2.3 V		12	mA
IOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	Vcс	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
1/01		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		lo 12 mΛ		2.3 V			0.7	v
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
` ´		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	VI – Voo or CND		221/				n.E
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V				pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V				рF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INPOT)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN MAX	
t _{pd}	А	Y					ns
t _{en}	ŌĒ	Υ					ns
^t dis	ŌĒ	Y					ns



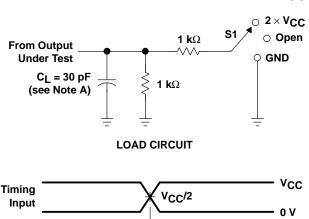
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

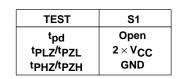
PRODUCT PREVIEW

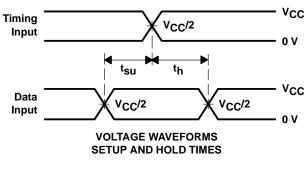
operating characteristics, T_A = 25°C

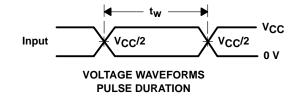
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
					111	111	
l	Power dissipation	Outputs enabled	Cı = 0. f = 10 MHz				pF
Cpd	capacitance	Outputs disabled	$C_L = 0,$ $f = 10 MHz$				pr

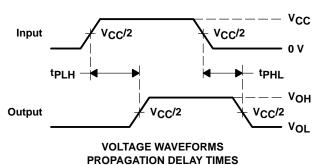
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

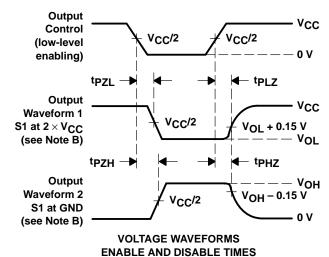










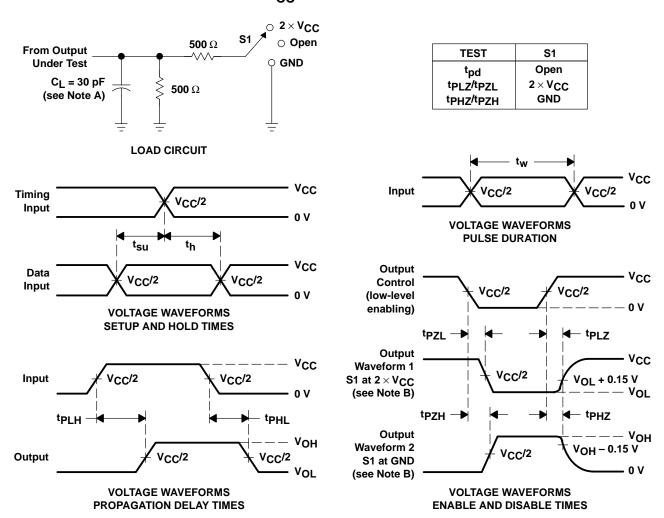


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



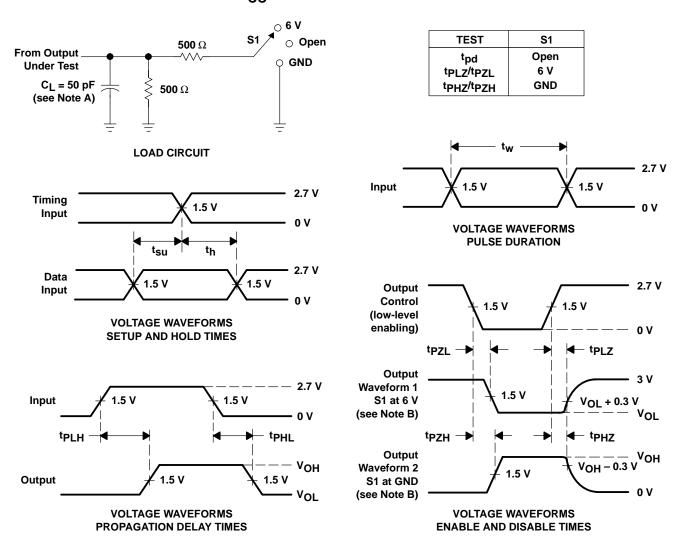
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DBB PACKAGE

(TOP VIEW)

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Plastic 300-mil Thin Shrink Small-Outline **Package**

description

This 1-bit to 2-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, the output-enable (OE) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH16830 is characterized for operation from -40°C to 85°C.

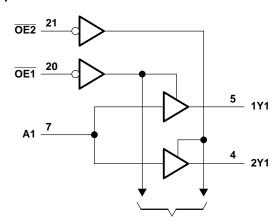
FUNCTION TABLE

	INPUTS	OUTPUTS		
OE1	OE2	Α	1Yn	2Yn
L	Н	Н	Н	Z
L	Н	L	L	Z
Н	L	Н	Z	Н
Н	L	L	Z	L
L	L	Н	Н	Н
L	L	L	L	L
Н	Н	Χ	z	Z

	(TOP VIEW)							
2Y2	Н	1	U	80	h	1Y3		
1Y2	П	2		79		2Y3		
GND	d	3		78		GND		
2Y1	d	4		77	6	1Y4		
1Y1	d	5		76	6	2Y4		
V_{CC}	d	6		75	þ	V_{CC}		
A1	Ц	7		74	þ	1Y5		
A2	П	8		73		2Y5		
GND	Ц	9		72	0	GND		
A3	Ц	10		71	0	1Y6		
A4	Ц	11		70	0	2Y6		
GND	Ц	12		69	Į	GND		
A5	Ц	13		68	Ų	1Y7		
A6	Ц	14		67	2	2Y7		
Vcc	Ц	15		66	P	VCC		
A7	Ц	16		65	Ľ	1Y8		
A8	Н	17		64	K	2Y8		
GND	Н	18		63	K	GND		
A9	Н	19		62	K	1Y9		
OE1	Н	20		61	K	2Y9		
OE2 A10	H	21		60	K	1Y10		
GND	H	22		59	K	2Y10 GND		
A11	H	23		58 57	K	1Y11		
A11	H	24		57 56	K	2Y11		
V _{CC}	H	25 26		56 55	K	V _{CC}		
A13	H	27		55 54	K	1Y12		
A14	H	28		53	K	2Y12		
GND	H	29		52	K	GND		
A15	K	30		51	K	1Y13		
A16	H	31		50	K	2Y13		
GND	H	32		49	K	GND		
A17	ď	33		48	Ħ	1Y14		
A18	П	34		47	ħ	2Y14		
V_{CC}	d	35		46	ħ	V_{CC}		
2Y18	d	36		45	Б	1Y15		
1Y18	0	37		44	6	2Y15		
GND	d	38		43	Ď	GND		
2Y17		39		42	þ	1Y16		
1Y17	d	40		41	þ	2Y16		
	•				•			

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To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to $V_{\mbox{CC}}$ + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage				V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
	High lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	1	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0	2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
1/01		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V	
VOL		lo 12 mΛ	2.3 V			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
lį		V _I = V _{CC} or GND	3.6 V			±5	μΑ	
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V	2.3 V	45				
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
` ´		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	VI – Voo or CND		221/				n.E
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V				pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V				рF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	MIN MAX	MIN MAX	MIN MAX	
t _{pd}	А	Y					ns
t _{en}	ŌĒ	Υ					ns
^t dis	ŌĒ	Y					ns



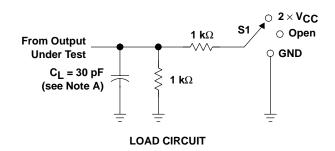
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

PRODUCT PREVIEW

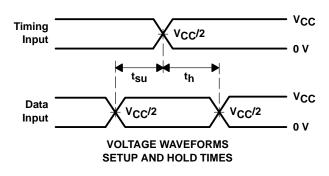
operating characteristics, T_A = 25°C

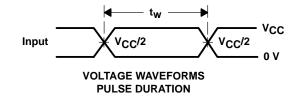
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C _{pd}	Power dissipation	Outputs enabled	C _L = 0, f = 10 MH	7			pF
Фра	capacitance	Outputs disabled	0L = 0, 1 = 10 mm				۲۰

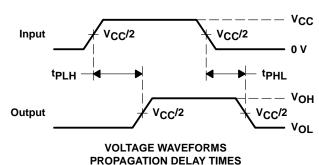
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

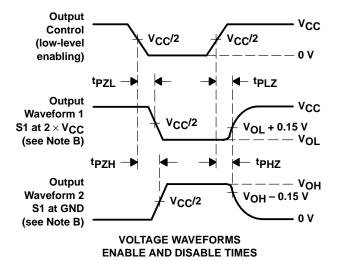










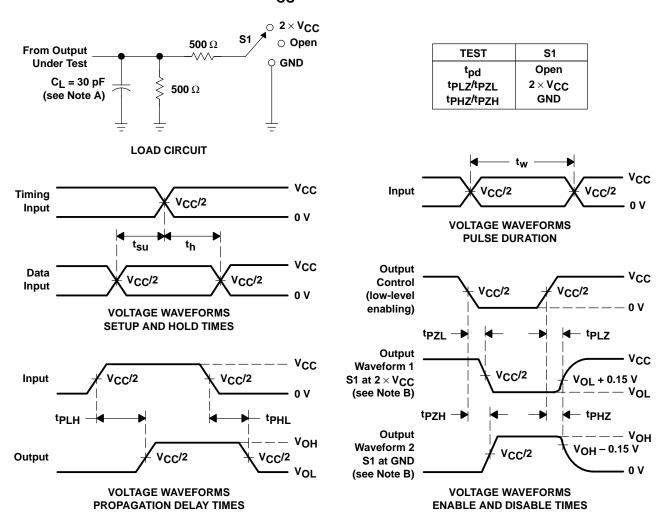


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



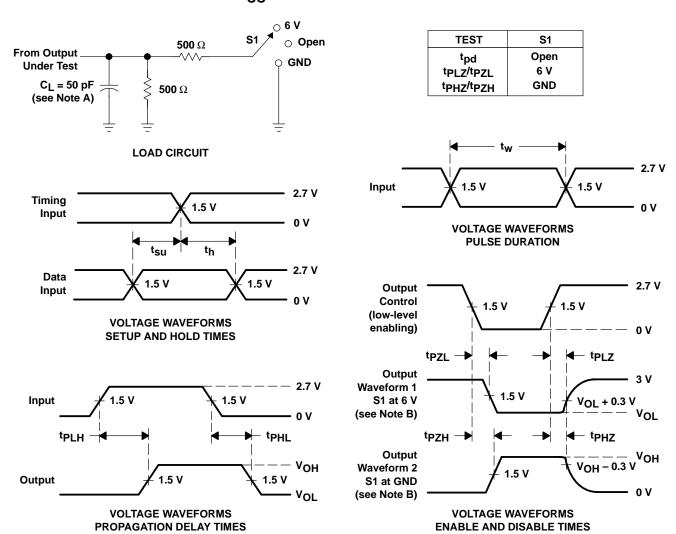
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DBB PACKAGE

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Packaged in Thin Very Small-Outline **Package**

description

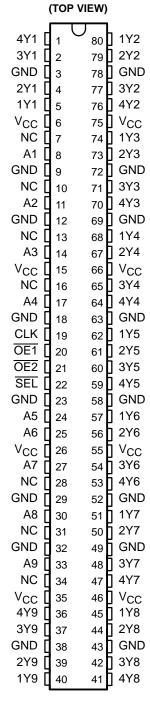
This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V V_{CC} operation. The device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVCH16831 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When SEL is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) controls. Each OE controls two groups of nine outputs.

When SEL is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. OE controls operate the same as in buffer mode.

When \overline{OE} is logic low, the outputs are in a normal logic state (high or low logic level). When OE is logic high, the outputs are in the high-impedance state.

SEL and OE do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



NC - No internal connection

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description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

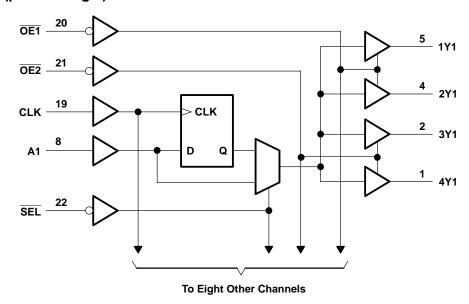
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16831 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	OUTPUT			
OE	SEL	CLK	Α	Y
Н	Χ	Х	Χ	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T _{sta}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage	Supply voltage			V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8		
٧ _I	Input voltage	0	VCC	V		
۷o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
1	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
lOH	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24]	
		V _{CC} = 1.65 V		4		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	1 .	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		VCC = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature			85	°C	
	Allows and an atraction of a fither device a count had be held		nation Defeat			

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		3 V	2				
		$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
\/a:		I _{OL} = 6 mA	2.3 V			0.4	V
VOL		I _{OL} = 12 mA	2.3 V			0.7	V
		IOL = 12 IIIA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
lį		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _I (hold)		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V, Other inputs	at V _{CC} or GND 3 V to 3.6 V			750	μΑ
	Control inputs				4.5		nE.
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5		pF
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, A data before CLK↑	§		2		2		1.6		ns
th	Hold time, A data after CLK↑	§		0.7		0.5		1.1	·	ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1.2	4		4.1	1.6	3.6	
t _{pd}	CLK	Y		†	1.1	4.5		4.4	1.5	3.9	ns
	SEL			†	1.3	5.2		5.2	1.7	4.4	
^t en	ŌĒ	Υ		†	1.1	5.1		5	1.2	4.3	ns
^t dis	ŌĒ	Y		†	1.4	5.5		4.7	1.6	4.5	ns

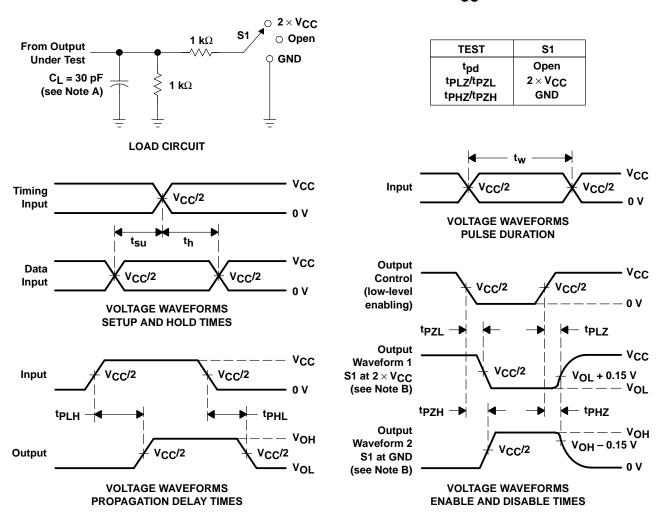
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CO	ONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
	Power dissipation	All outputs enabled	C: -0	f = 10 MHz	†	119	132	pF
Cpd	capacitance per register/driver	All outputs disabled	C _L = 0,	I = 10 WINZ	†	22	25	рг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



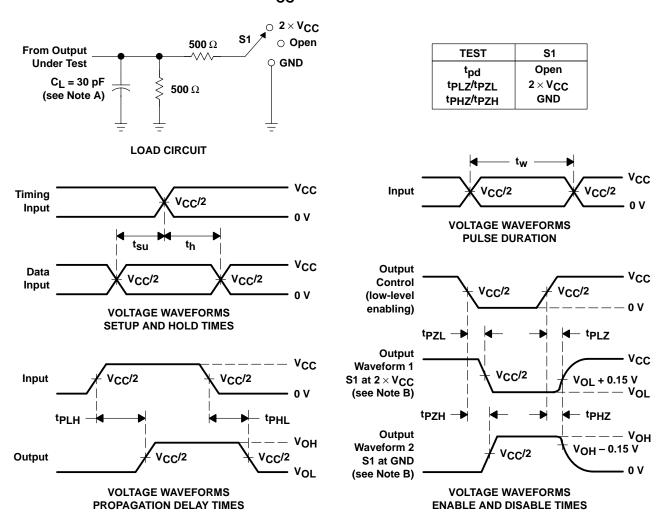
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

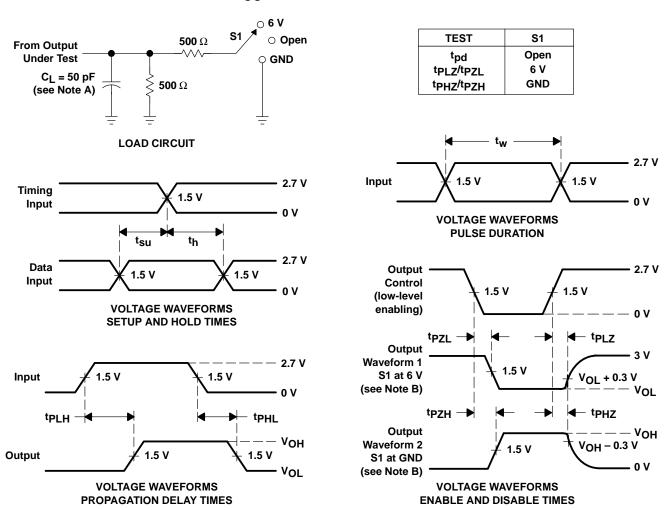


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2 \ ns$, $t_f \leq 2 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzl and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG PACKAGE

(TOP VIEW)

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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown**
- Packaged in Thin Shrink Small-Outline **Package**

description

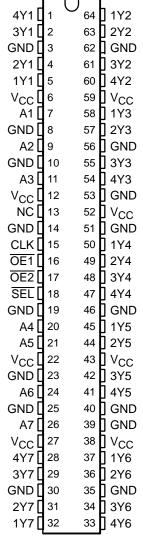
This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V V_{CC} operation. This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVCH16832 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When SEL is a logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) inputs. Each OE controls two groups of seven outputs.

When SEL is a logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data at the A inputs is stored in the internal registers. OE operates the same as in the buffer mode.

When \overline{OE} is a logic low, the outputs are in a normal logic state (high or low logic level). When OE is a logic high, the outputs are in the high-impedance state.

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NC - No internal connection

Neither SEL nor OE affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

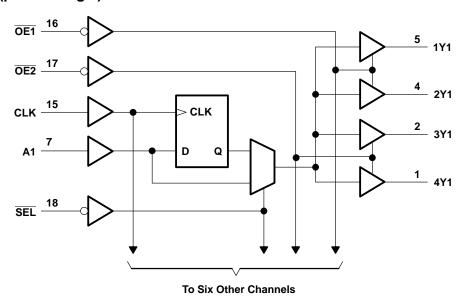
The SN74ALVCH16832 is characterized for operation from –40°C to 85°C.

testing of all parameters.

FUNCTION TABLE

	INP	OUTPUT		
OE	SEL	CLK	Α	Υ
Н	Х	Х	Х	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	–0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16832 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS SCES098D - MAY 1997 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
lou	High level output ourrent	V _{CC} = 2.3 V		-12	mA
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		3 V	2				
		$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
\/a:		I _{OL} = 6 mA	2.3 V			0.4	V
VOL		I _{OL} = 12 mA	2.3 V			0.7	V
		IOL = 12 IIIA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
lį		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _I (hold)		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V, Other inputs	at V _{CC} or GND 3 V to 3.6 V			750	μΑ
	Control inputs				4.5		nE.
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5		pF
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, A data before CLK↑	§		2		2		1.6		ns
th	Hold time, A data after CLK↑	§		0.7		0.5		1.1	·	ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	AMETER FROM (INPUT)		V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1.2	4		4.1	1.6	3.6	
t _{pd}	CLK	Y		†	1.1	4.5		4.4	1.5	3.9	ns
	SEL			†	1.3	5.2		5.2	1.7	4.4	
^t en	ŌĒ	Υ		†	1.1	5.1		5	1.2	4.3	ns
^t dis	ŌĒ	Υ		†	1.4	5.5		4.7	1.6	4.5	ns

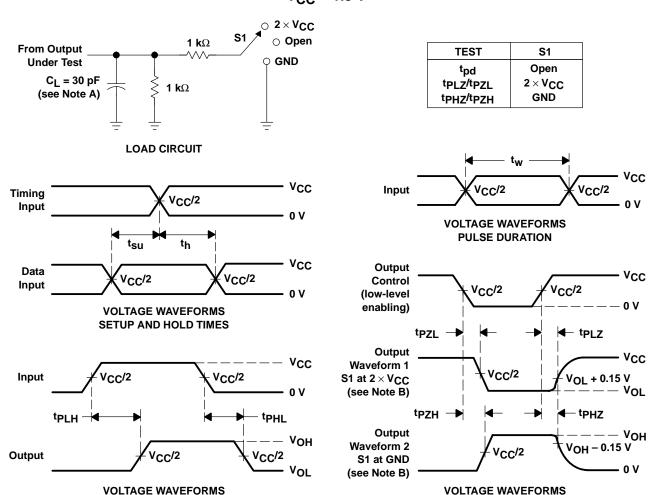
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		R	TEST CONDITIONS		V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
	Power dissipation capacitance	on	All outputs enabled	C. – 0	f = 10 MHz	†	119	132	pF
1	per register/driv	er	All outputs disabled	C _L = 0,	1 = 10 NIMZ	†	22	25	pΓ

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

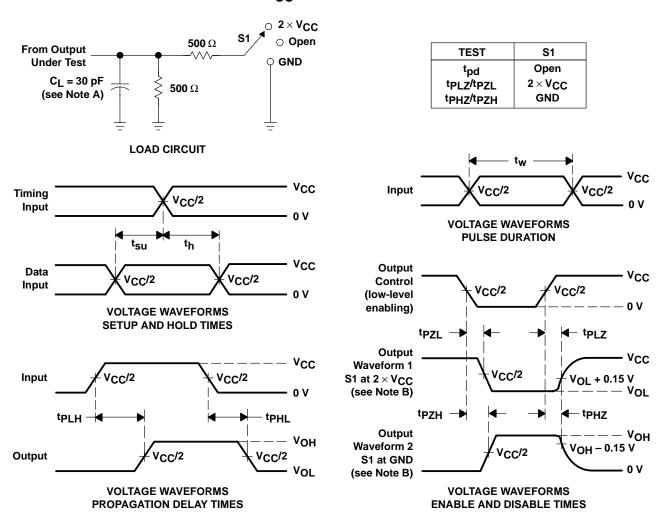
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

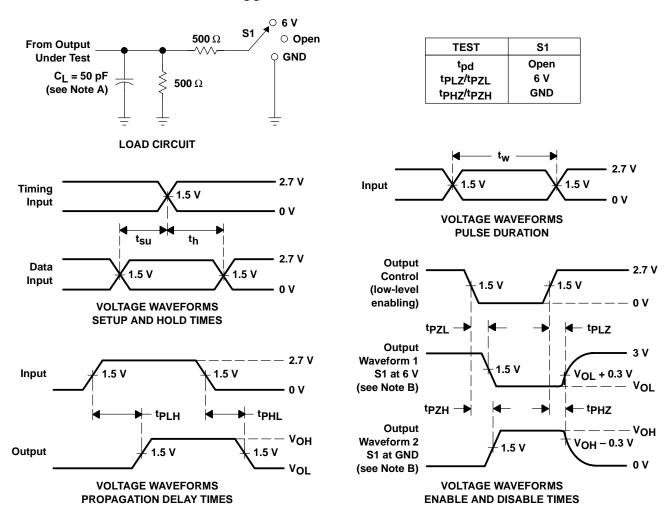


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SCES140B - JULY 1998 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

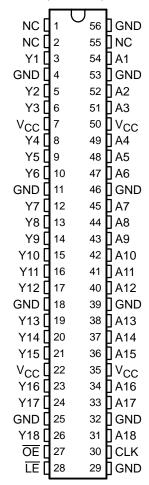
This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC16834 is characterized for operation from –40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



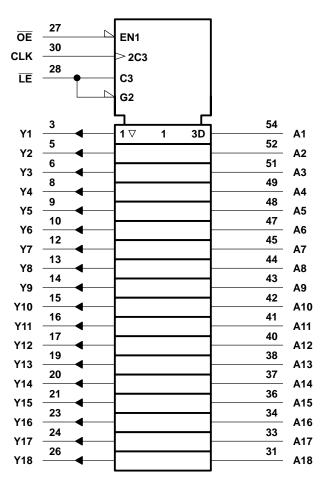
NC - No internal connection

FUNCTION TABLE

	INP		OUTPUT	
OE	LE	CLK	Α	Υ
Н	Х	Х	Х	Z
L	L	Χ	L	L
L	L	Χ	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	Н	Χ	Y ₀ †
L	Н	L	Χ	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high

logic symbol§

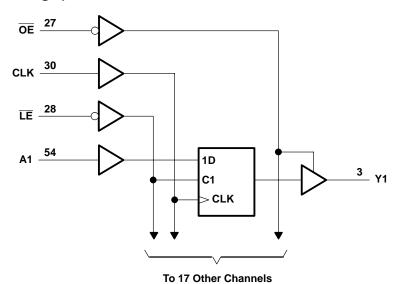


[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3):	: DGG package	81°C/W
•	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	mA
ЮН	VIH High-level input voltage VIL Low-level input voltage VI Input voltage VO Output voltage IOH High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
'OL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CON	NDITIONS	VCC	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
VOH IOH = -4 mA 1.65 V 1.2 IOH = -6 mA 2.3 V 2 IOH = -12 mA 2.7 V 2.2 3 V 2.4 IOH = -24 mA 3 V 2 IOL = 100 μA 1.65 V to 3.6 V IOL = 4 mA 1.65 V 0 IOL = 6 mA 2.3 V IOL = 12 mA 2.3 V IOL = 24 mA 3 V 0 IOL = 24 mA 3 V 0 IOL = 12 mA 3 V 0 IOL = 24 mA 3 V 0 IOL = 24 mA 3 V 0 IOL = 24 mA 3 V 0 IOL = 12 mA 3 V 0 IOL									
	I _{OH} = -6 mA		2.3 V	2					
∨он				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
Vol		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V		
VOL		loι = 12 mΛ		2.3 V			0.7	V	
		IOL = 12 IIIA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	O = 0	3.6 V			40	μΑ	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
C.	Ci Control inputs $V_1 = V_C C$ or GND 3.3 V		/ Vocas CND		4		pF		
L ^G	Data inputs	AL = ACC OLGIAD		3.3 v		5.5		ρι	
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	Pulse duration	LE low		‡		3.3		3.3		3.3		ns
t _W	CLK high or low			‡		3.3		3.3		3.3		115
		Data before CLK↑		‡		2.1		2.1		1.7		
t _{su}	Setup time		CLK high	‡		2.2		2.3		1.9		ns
		Data before LE ↑	CLK low	‡		1.5		1.9		1.5		
		Data after CLK↑		‡		0.6		0.6		0.7		
t _h	Hold time	Data after LE ↑	CLK high or low	‡		0.8	·	0.8		0.9	·	ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(IIVI O1)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	Α			†	1	4.4		4.2	1	3.6	
^t pd	LE	Υ		†	1.3	6		5.9	1.5	4.9	ns
	CLK			†	1.2	6		5.3	1.5	4.6	
t _{en}	ŌĒ	Υ		†	1.4	5.6		5.6	1.5	5	ns
t _{dis}	ŌĒ	Y		†	1	4		4.7	1.8	4.5	ns

[†]This information was not available at the time of publication.

switching characteristics from 0° C to 65° C, C_{L} = 50 pF

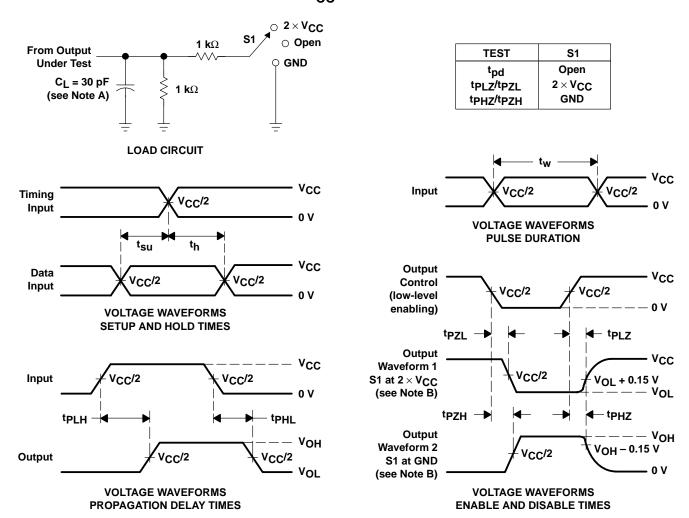
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	
^t pd	CLK	Υ	1.7	4.3	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} = 3.3 V	UNIT	
	FARAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONIT	
<u> </u>	Dower discination conscitones	Outputs enabled	C. O. f. 10 MHz	†	38	41	pF	
Cpd	Power dissipation capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$	†	13	15	p _F	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

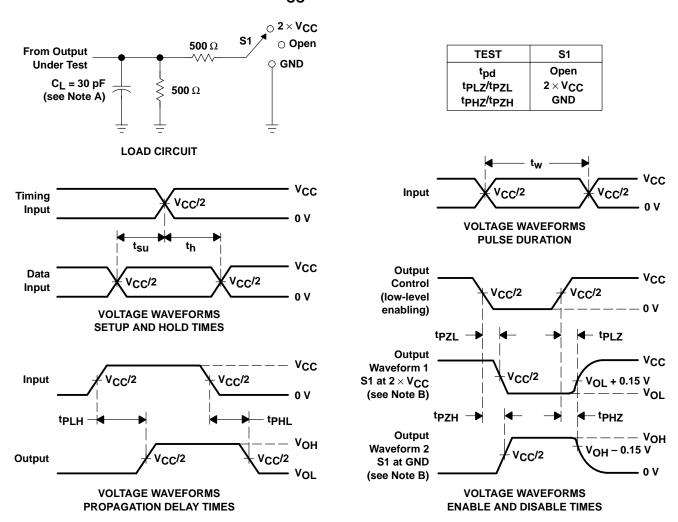


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



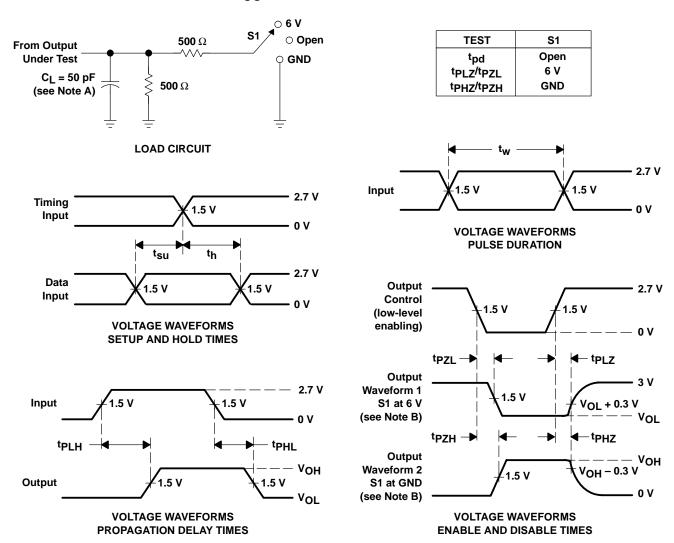
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16834 **18-BIT UNIVERSAL BUS DRIVER** WITH 3-STATE OUTPUTS

SCES190 - FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

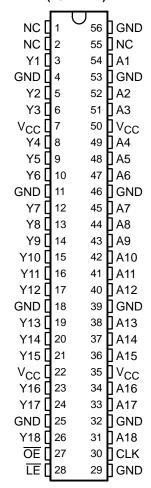
Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When OE is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16834 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

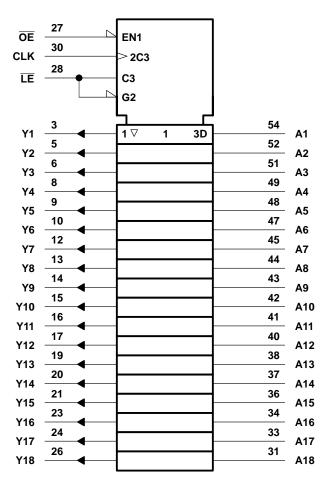
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

	INP	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Х	Z
L	L	Χ	L	L
L	L	Χ	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	Н	Χ	Y ₀ †
L	Н	L	Χ	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before $\overline{\text{LE}}$ goes high

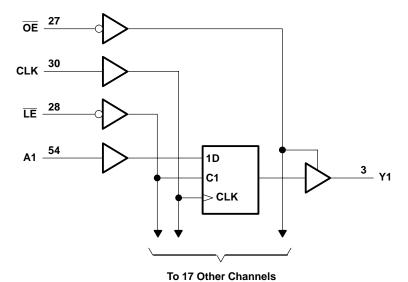
logic symbol§



[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, I _O		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):		
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16834 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES190 - FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
lau	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-12	m 1
IOH	nign-ievei output current	$V_{CC} = 2.7 V$		-12	mA
	L Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2	-		
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
\ \/ - ·		I _{OL} = 6 mA	2.3 V			0.4	
VOL		104	2.3 V		-	0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
Ц		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
` ′		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
∆lcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs Data inputs	V _I = V _{CC} or GND	3.3 V				pF
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		-		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$			V _{CC} = 2.7 V		V _{CC} =		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency											MHz
	Pulse duration	LE low										
t _w	Puise duration	CLK high or low										ns
		Data before CLK↑										
t _{su}	Setup time	Data hatawa LE ↑	CLK high									ns
		Data before LE ↑	CLK low									
		Data after CLK↑										
th	Hold time	Data after LE↑	CLK high or low									ns



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(IIVFOT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
	Α										
t _{pd}	LE	Y									ns
	CLK										
t _{en}	ŌĒ	Υ									ns
^t dis	ŌĒ	Y									ns

switching characteristics from 0°C to 65°C, C_L = 50 pF

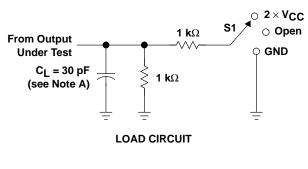
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V	UNIT
	(111 01)	(6611-61)	MIN MAX	
t _{pd}	CLK	Y		ns

operating characteristics, $T_A = 25^{\circ}C$

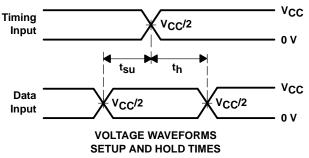
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V V _{CC} = 3.3 V		UNIT	
		1201 CONDITIONS	TYP	TYP	TYP	0	
<u> </u>	Power dissipation	Outputs enabled	C _I = 0, f = 10 MHz				ρF
C _{pd} capacitance		Outputs disabled	$C_L = 0,$ $f = 10 MHz$				þΓ

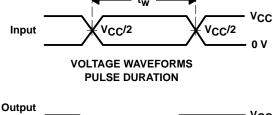


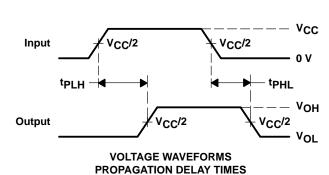
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

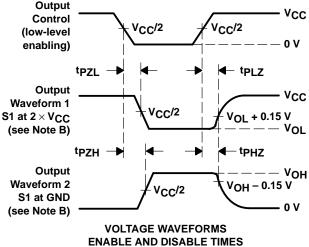


TEST	S1
^t pd	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND







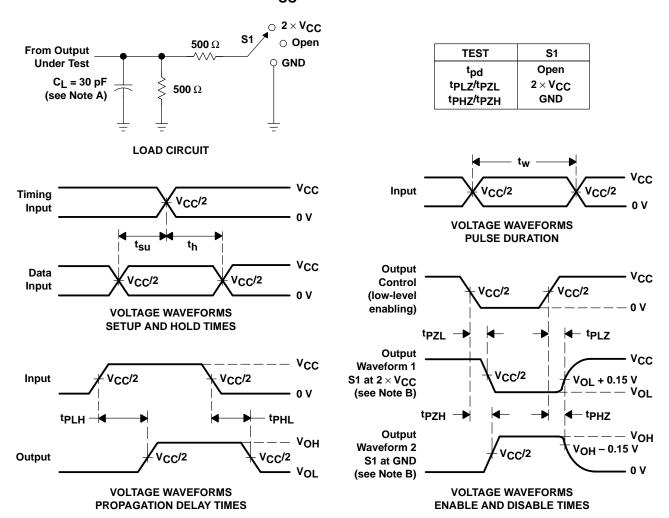


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

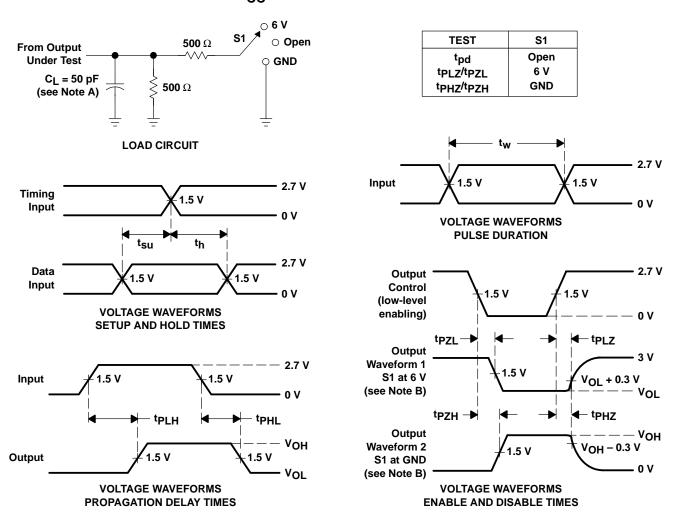
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzI and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SCES125D - FEBRUARY 1998 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Ideal for Use in PC100 Register DIMM **Revision 1.1**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC16835 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

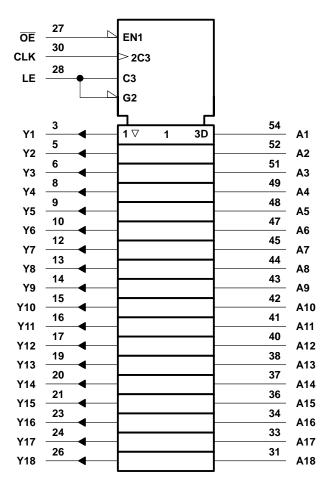
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

	INF	OUTPUT		
OE	LE	CLK	Α	Υ
Н	Х	Х	Χ	Z
L	Н	Χ	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н
L	L	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

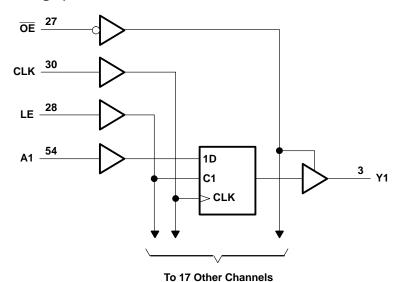
logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		. -0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
1	High-level output current	V _{CC} = 2.3 V		-12	A	
ЮН		V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Low-level output current	V _{CC} = 2.3 V	12 12		mA	
IOL		V _{CC} = 2.7 V				
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	NDITIONS	VCC	MIN	TYP [†]	MAX	UNIT		
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2				
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2					
	I _{OH} = -6 mA	2.3 V	2							
Voн			2.3 V	1.7			V			
		I _{OH} = -12 mA		2.7 V	2.2					
			3 V	2.4						
		I _{OH} = -24 mA	3 V	2						
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2				
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45				
V		$I_{OL} = 6 \text{ mA}$	2.3 V			0.4				
VOL		I _{OL} = 12 mA	2.3 V			0.7				
		IOL = 12 IIIA	2.7 V			0.4				
		I _{OL} = 24 mA	3 V			0.55				
П		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ		
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ		
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ		
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ		
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5		pF				
	Data inputs	AL = ACC OLGIND		3.3 v	5			ρг		
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF		

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	tw Pulse duration	LE high		‡		3.3		3.3		3.3		ns
t _W	Puise duration	CLK high or low		‡		3.3		3.3		3.3		115
		Data before CLK↑		‡		2.2		2.1		1.7		
t _{su}	t _{SU} Setup time	Data before LE↓	CLK high	‡		1.9		1.6		1.5		ns
		Data before LEV	CLK low	‡		1.3		1.1		1		
		Data after CLK↑		‡		0.6		0.6		0.7		
t _h Hold time	Hold time	Data after LE↓	CLK high or low	‡		1.4		1.7		1.4		ns

[‡] This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(IIVFOT)	(001101)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	4.2		4.2	1	3.6	
t _{pd}	LE	Y		†	1.3	5		4.9	1.3	4.2	ns
·	CLK			†	1.4	5.5		5.2	1.4	4.5	
t _{en}	ŌĒ	Y		†	1.4	5.5		5.6	1.1	4.6	ns
t _{dis}	ŌĒ	Y		†	1	4.5		4.3	1.3	3.9	ns

[†] This information was not available at the time of publication.

switching characteristics from 0° C to 85° C, $C_L = 0$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(INFOT)	(001F01)	MIN	MAX	
t _{pd} †	A	Y	0.9	2	
	CLK	Υ	1.5	2.9	ns

[†] Texas Instruments SPICE simulation data

switching characteristics from 0° C to 65° C, $C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	
^t pd	A	Y	1	4	no
	CLK	Y	1.7	4.5	ns

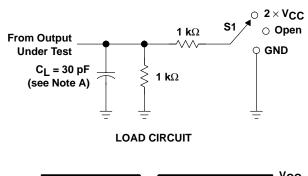
operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V V _{CC} = 3.3 V		UNIT	
PARAMETER		1E31 CONDITIONS	TYP	TYP	TYP	UNII	
<u> </u>	Power dissipation	Outputs enabled	Cı = 0. f = 10 MHz	†	26	31	pF
C _{pd}	capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHZ$	†	12	14	рΓ

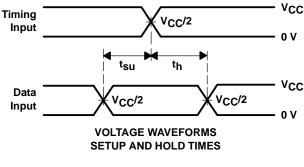
[†] This information was not available at the time of publication.

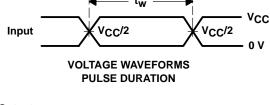


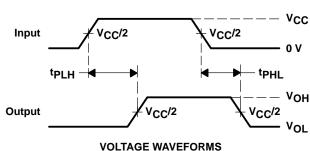
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



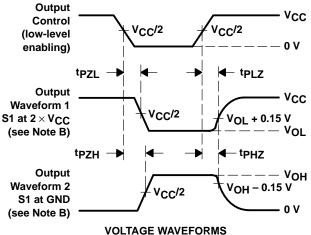
TEST	S 1
^t pd	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND







PROPAGATION DELAY TIMES



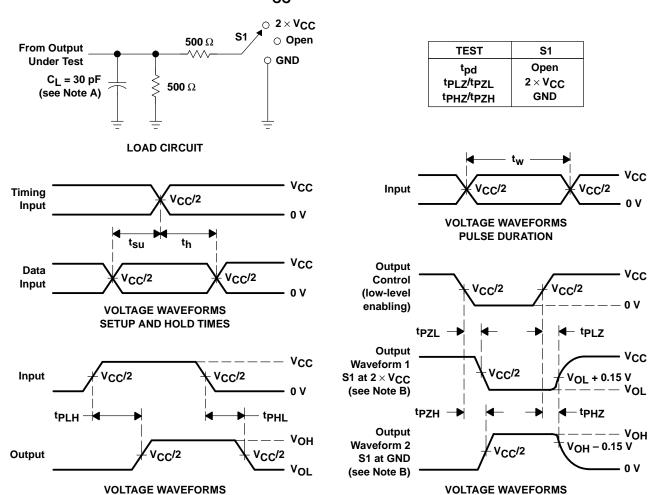
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

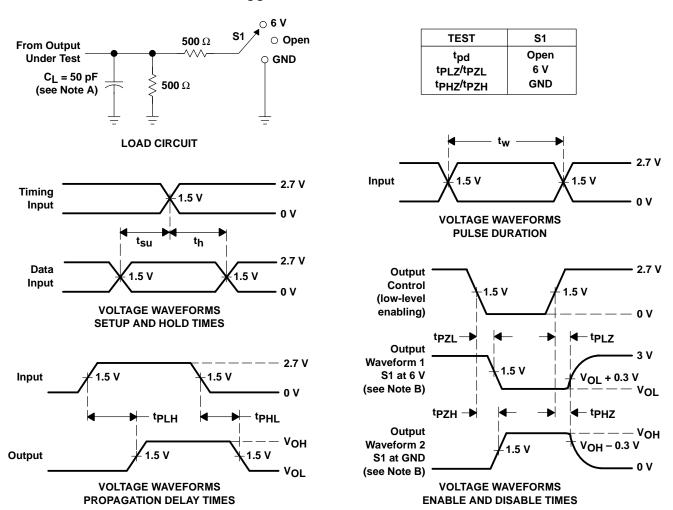
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzI and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

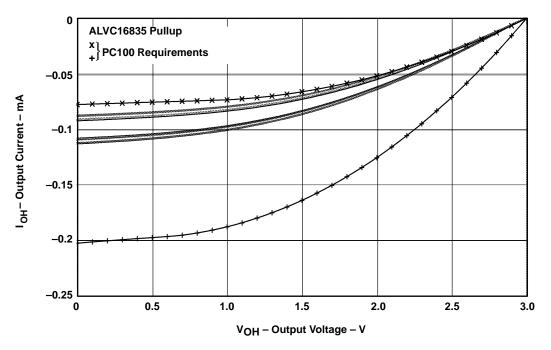


Figure 4. IV Characteristics - Pullup

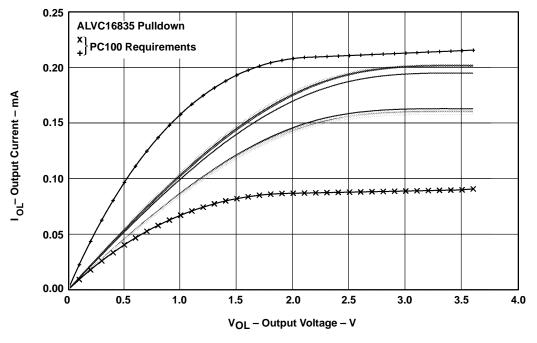


Figure 5. IV Characteristics - Pulldown



SCES053E - SEPTEMBER 1995 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

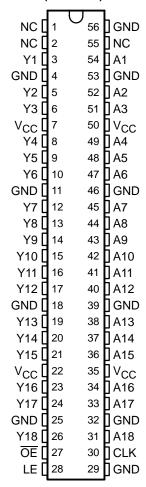
Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16835 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

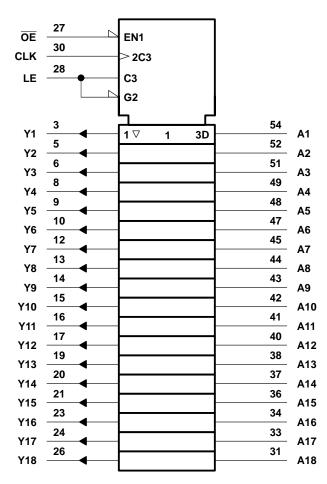
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FUNCTION TABLE

	INP		OUTPUT	
OE	LE	CLK	Α	Υ
Н	Х	Х	Х	Z
L	Н	Χ	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н
L	L	Н	Χ	Y ₀ †
L	L	L	Χ	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

logic symbol§

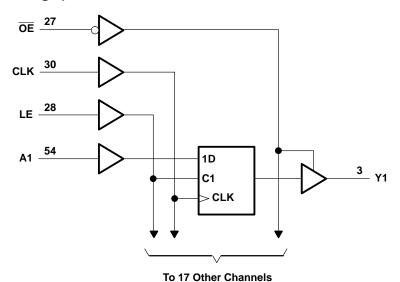


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		–0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND)	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)): DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	IPak Israel and assessed	V _{CC} = 2.3 V	-12		m^
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	IIIA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Voн				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA						
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		I _{OL} = 12 mA		2.3 V			0.7	v
		IOL = 12 IIIA		2.7 V			0.4	
		I _{OL} = 24 mA					0.55	
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs Data inputs	V _I = V _{CC} or GND		3.3 V		3.5 6		pF
Со	Outputs	V _O = V _{CC} or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency			§		150		150		150	MHz		
Pulse	Ilse LE high		§		3.3		3.3		3.3		20	
t _w	duration	CLK high or low		§		3.3		3.3		3.3		ns
	_	Data before CLK↑		§		2.2		2.1		1.7		
t _{su}	Setup time	Data hafana I E l	CLK high	§		1.9		1.6		1.5		ns
	unic	Data before LE↓	CLK low	§		1.3		1.1		1		
4.	t _h Hold time	Data after CLK↑		§		0.6		0.6		0.7		20
l th		Data after LE↓	CLK high or low	§		1.4		1.7		1.4		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(001101)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	Α			†	1	4.2		4.2	1	3.6	
t _{pd}	LE	Y		†	1.3	5		4.9	1.3	4.2	ns
·	CLK			†	1.4	5.5		5.2	1.4	4.5	
t _{en}	ŌĒ	Y		†	1.4	5.5		5.6	1.1	4.6	ns
^t dis	ŌĒ	Y		†	1	4.5		4.3	1.3	3.9	ns

[†] This information was not available at the time of publication.

switching characteristics from 0° C to 65° C, C_{L} = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	
^t pd	CLK	Υ	1.7	4.5	ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation	Outputs enabled	C _I = 50 pF, f = 10 MHz	†	26	31	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	12	14	þΓ

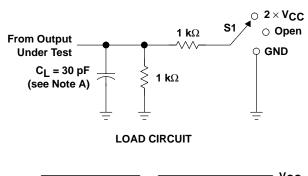
[†] This information was not available at the time of publication.



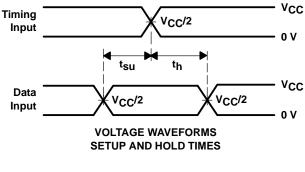
VCC

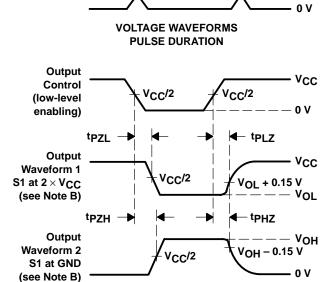
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



TEST	S 1
^t pd	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND



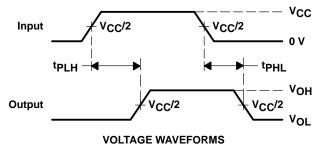


VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

V_{CC}/2

Input

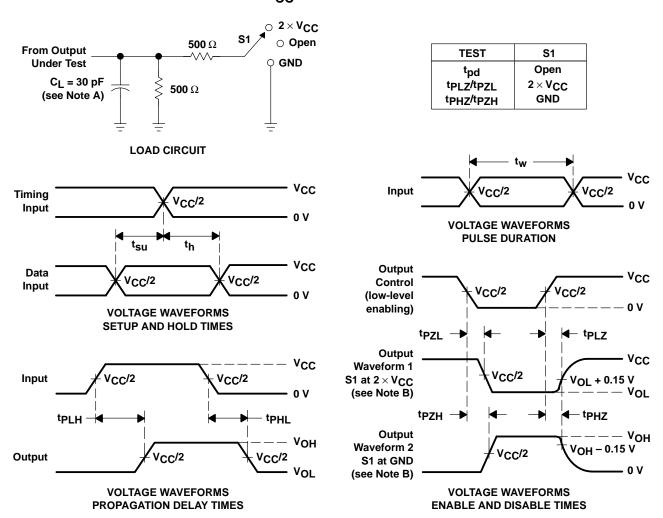


 $\label{eq:propagation delay times}$ NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



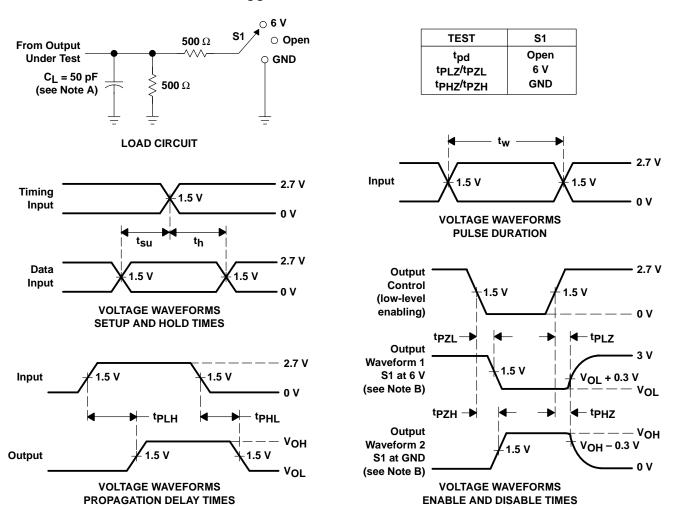
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzI and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **Designed to Comply With JEDEC 168-Pin** and 200-Pin SDRAM Buffered DIMM Specification
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Shrink** Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16836 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)



NC - No internal connection

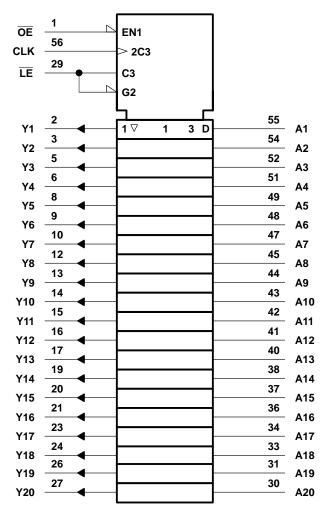
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

	INPUTS							
OE	LE	CLK	Α	Y				
Н	Х	Х	Х	Z				
L	L	Χ	L	L				
L	L	Χ	Н	Н				
L	Н	\uparrow	L	L				
L	Н	\uparrow	Н	Н				
L	Н	Н	Χ	Y ₀ †				
L	Н	L	Χ	Y ₀ ‡				

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before $\overline{\text{LE}}$ goes low

logic symbol§

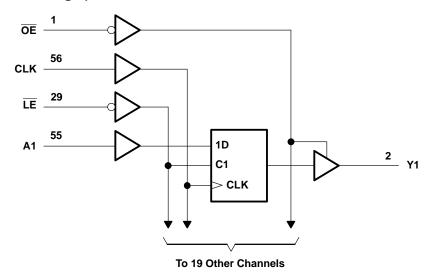


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package 81°C/W
•••	DL package 74°C/W
Storage temperature range, T _{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16836 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
1	High-level output current	V _{CC} = 2.3 V		-12	A
ІОН		V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Lave laved autout avenue	V _{CC} = 2.3 V		12	A
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
\ \/		I _{OL} = 6 mA		2.3 V			0.4	\/
VOL		1- 40 m A		2.3 V			0.7	V
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
lį		V _I = V _{CC} or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
` ´		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V		-	±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V		-	40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs Data inputs	V _I = V _{CC} or GND		3.3 V				pF
Со	Outputs	$V_O = V_{CC}$ or GND		3.3 V				pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	f _{clock} Clock frequency										MHz		
	Pulse	LE low											
t _W	duration	CLK high or low										ns	
		Data before CLK↑											
t _{su}	Setup time	D	CLK high									ns	
	Data before LE ↑	CLK low											
4.	I laid time	Data after CLK↑										20	
t _h	Hold time	Data after LE↑	CLK high or low									ns	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
	А										
t _{pd}	LE	Y									ns
	CLK										
t _{en}	ŌĒ	Υ									ns
^t dis	ŌĒ	Y									ns

operating characteristics, T_A = 25°C

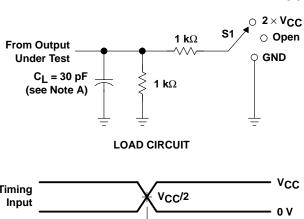
PARAMETER			TEST CON	DITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAWIETER		TEST CONDITIONS		TYP	TYP	TYP	ONIT
<u> </u>	Power dissipation	Outputs enabled	C. – 0	f = 10 MHz				pF
Cpd	capacitance	Outputs disabled	$C_L = 0$,	I = IU IVINZ				рг

VCC

0 V

V_{CC}/2

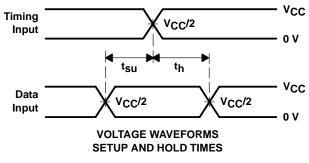
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

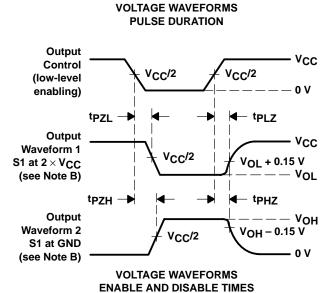


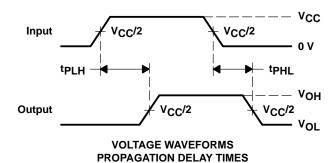
TEST	S 1
^t pd	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND

V_{CC}/2

Input





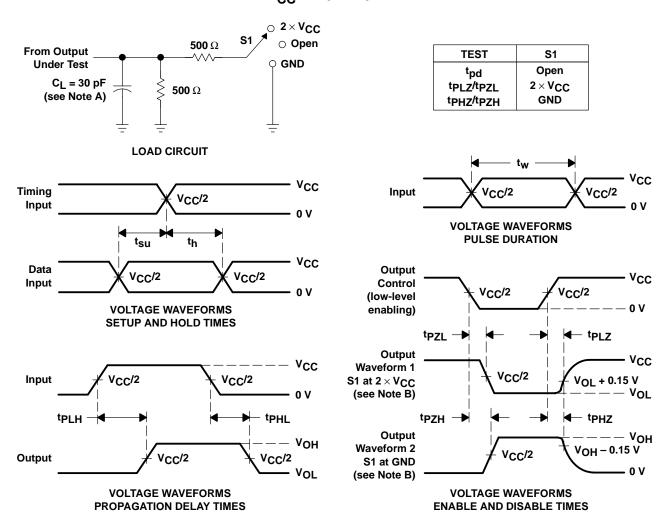


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



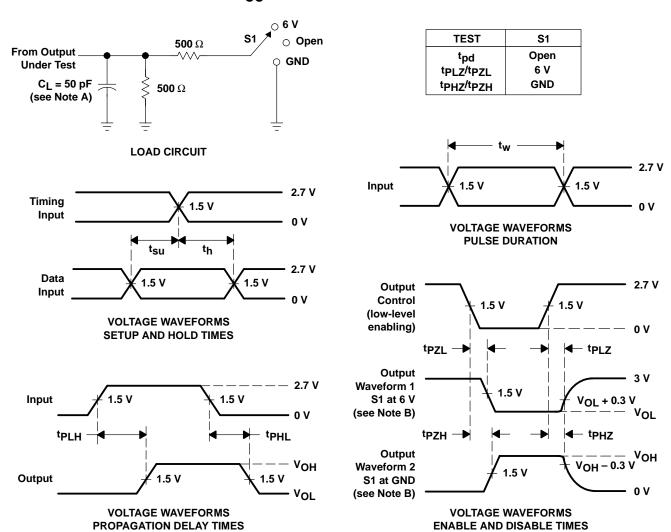
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DGG OR DL PACKAGE

(TOP VIEW)

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

56 11LE 10E L 55 🛭 1D1 1Q1 **[**] 2 54 1D2 1Q2 🛮 3 GND 4 53 GND 52 D 1D3 1Q3 4 5 51 🛮 1D4 1Q4 **[**] 6 V_{CC} [] 7 50 V_{CC} 49 1D5 1Q5 L 8 1Q6 🛮 9 48 1D6 47 🛮 1D7 107 10 46 | GND GND **1**11 1Q8 📙 12 45 🛮 1D8 1Q9 🛮 13 44 D 1D9 43 1D10 1Q10 **1** 14 2Q1 🛮 15 42 2D1 202 16 41 | 2D2 40 2D3 2Q3 **[**] 17 GND [] 18 39 D GND 38 🛭 2D4 19 2Q4 L 2Q5 🛮 20 37 2D5 2Q6 🛮 21 36 2D6

35 V_{CC}

34 L 2D7

33 2D8 32 GND

31 2D9

30 2D10

29 2LE

V_{CC} 422

2Q7 🛮 23

2Q8 L 24

GND 25

2Q9 4 26

2OE 4 28

2Q10 27

A buffered output-enable $(1\overline{OE} \text{ or } 2\overline{OE})$ input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OE does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.

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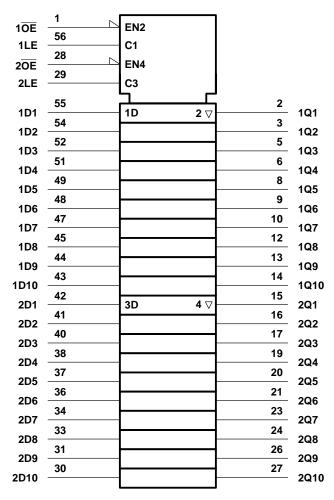
PRODUCTION DATA information is current as of publication date.



FUNCTION TABLE (each 10-bit latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

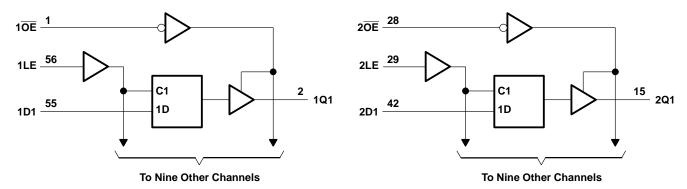
logic symbol†



 $^{\ ^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCES043D - JULY 1995 - REVISED FEBRUARY 1999

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCES043D - JULY 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	3.6	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		1.65 3.6 95 V 0.65 × V _{CC} V 1.7 V 2 95 V 0.35 × V _{CC} V 0.7 V 0.8 0 V _{CC} -4 -12 -12 -24 4 12 12 24	V	
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-4	
1	High level output ourrent	V _{CC} = 2.3 V		-12	A
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V	1.65 3.6 0.65 × V _{CC} 1.7 2 0.35 × V _C 0.7 0.8 0 V _{CC} 0 V _{CC} -4 -12 -12 -24 4 12 12 24 10	-24	
		V _{CC} = 1.65 V		4	
1	Law lavel output ourrent	V _{CC} = 2.3 V		12	A
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETE	R TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Voн		2.3 V	1.7			V
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
V	$I_{OL} = 6 \text{ mA}$	2.3 V			0.4	V
VOL	In. 12 m/s	2.3 V			0.7	V
	I _{OL} = 12 mA	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
Ц	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{\parallel} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔlCC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
Control	nputs VI – Vice or GND	3.3 V		4.5		nE.
C _i Data inp	$V_{I} = V_{CC} \text{ or GND}$	3.3 V		6.5		pF
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} =	V _{CC} = 1.8 V		2.5 V 2 V	$V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$			UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↑	§		0.9		0.7		1.1		ns
th	Hold time, data after LE↑	§		1.2		1.5		1.1		ns

[§] This information was not available at time of publication.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
4 .	D	Q	†	1	5		4.7	1.2	3.9	no
^t pd	LE	ζ	†	1	5.6		5.1	1	4.3	ns
t _{en}	ŌĒ	Q	†	1	6.2		6	1	4.9	ns
^t dis	ŌĒ	Q	†	1.1	5.3		4.3	1.3	4.1	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

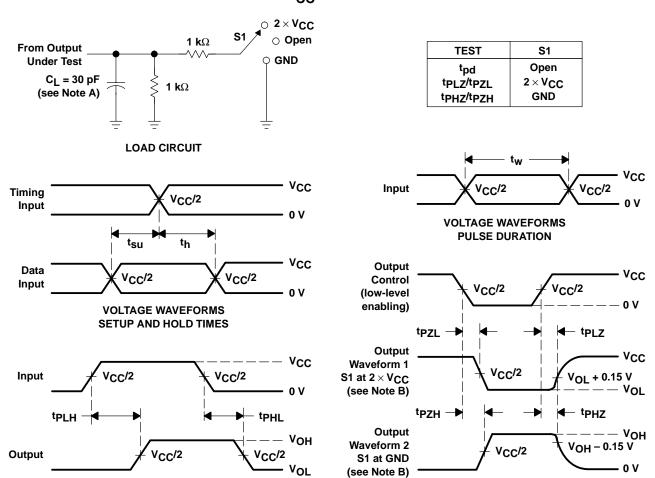
	and		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAMETER		1E31 CONDITIONS	TYP	TYP	TYP	ONIT
<u> </u>	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	12	20	pF
C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	1	3	рг

[†] This information was not available at the time of publication.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.

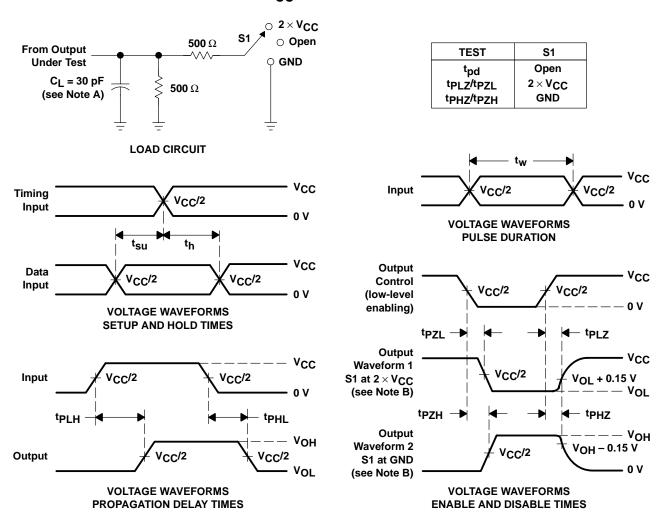
VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



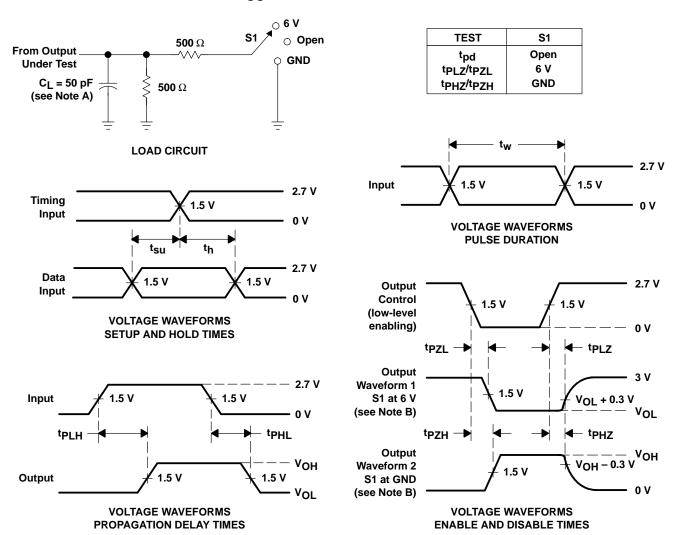
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

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- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V $V_{\rm CC}$ operation.

The SN74ALVCH16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

This device can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or the high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered

1CLR 56 1LE 1OE 2 55 1PRE 1Q1 **[**] 3 54 ¶ 1D1 GND []4 53 GND 1Q2 **[**] 5 52 1D2 1Q3 **[**] 6 51 1D3 50 V_{CC} V_{CC} 47 1Q4 🛮 8 49 1 1D4 1Q5 🛮 9 48 1 1D5 47 🛮 1D6 1Q6 110 GND [11 46 | GND 1Q7 L 12 45 1D7 1Q8 🛮 13 44 🛛 1D8 43 D9 1Q9 🛮 14 42 **∏** 2D1 2Q1 15 2Q2 116 41 2D2 2Q3 [] 17 40 2D3 39 GND GND 18 38 2D4 2Q4 1 19 2Q5 **∏** 20 37 T 2D5 2Q6 **1** 21 36 2D6 35 V_{CC} V_{CC} 22 2Q7 **[**] 23 34 🛮 2D7 33 2D8 2Q8 L 24 GND **1**25 32 🛮 GND 2Q9 [26 31 **∏** 2D9 20E 27 30 2PRE 2CLR 28 29 2LE

down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

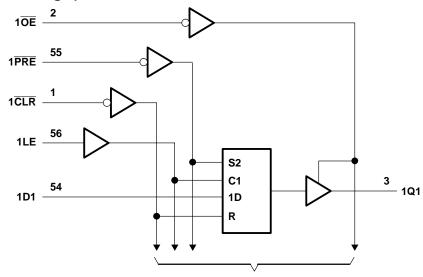
The SN74ALVCH16843 is characterized for operation from -40°C to 85°C.

TEXAS
INSTRUMENTS

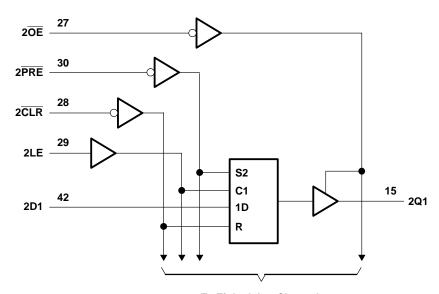
FUNCTION TABLE (each 9-bit latch)

		OUTPUT			
PRE	CLR	Q			
L	Х	L	Х	Χ	Н
Н	L	L	X	Χ	L
Н	Н	L	Н	L	L
Н	Н	L	Н	Н	Н
Н	Н	L	L	Χ	Q_0
Х	Χ	Н	Χ	Χ	Z

logic diagram (positive logic)



To Eight Other Channels



To Eight Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{Sto}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		V _{CC} = 2.7 V to 3.6 V	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
V _I V _O		V _{CC} = 2.7 V to 3.6 V		0.7 0.8 VCC VCC -4 -12 -12 -24 4 12		
٧ _I	Input voltage	-	0	Vcc	V	
٧o	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
1	High lavel autout average	V _{CC} = 2.3 V		-12	Λ	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
V _{IH} V _{IL}		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Lavidaval autavi avimost	V _{CC} = 2.3 V		12	Λ	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0	2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
1/01		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		lo 12 mΛ		2.3 V			0.7	v
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
` ´		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	VI – Voo or CND		221/				n.E
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V				pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V				рF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Pulse duration	PRE or CLR low									ns
t _W I	Puise duration	LE high or low									
		Data high before LE↓									
١.	Catum times	Data low before LE↓									no
t _{su}	Setup time	PRE inactive before LE↓									ns
		CLR inactive before LE↓									
th	Hold time	Data after LE↓									ns



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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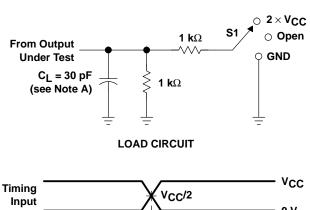
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

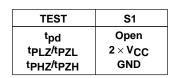
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	(IIVI O1)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN MAX	
	D						
t _{pd}	LE	Q					ns
·	PRE or CLR						
^t en	ŌĒ	Q					ns
^t dis	ŌĒ	Q					ns

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
Cpo	Power dissipation capacitance	Outputs enabled Outputs disabled	C _L = 0, f = 10 MH	z			pF

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$





V_{CC}/2

VOLTAGE WAVEFORMS PULSE DURATION

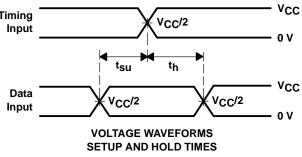
ENABLE AND DISABLE TIMES

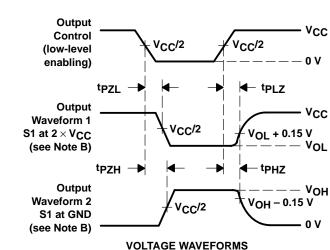
Input

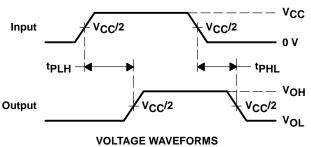
VCC

0 V

V_{CC}/2







 $\label{eq:propagation delay times}$ NOTES: A. C_L includes probe and jig capacitance.

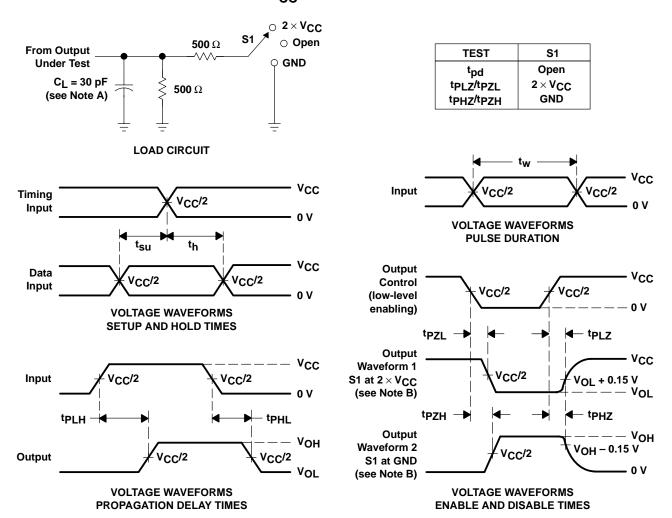
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

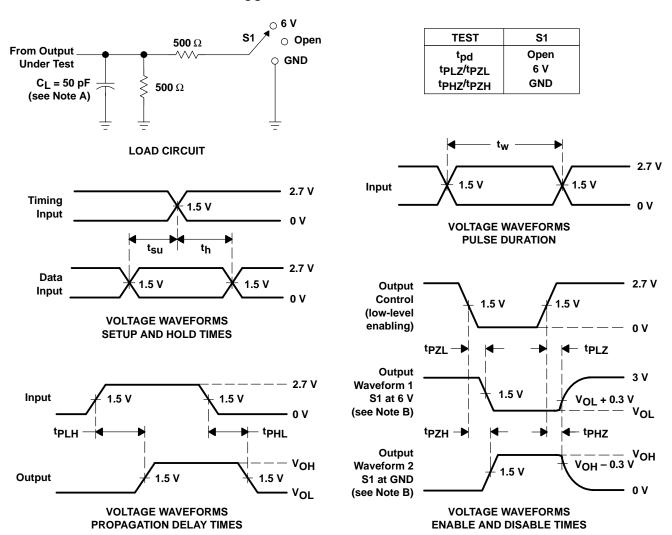
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16863 is an 18-bit noninverting transceiver designed for synchronous communication between data buses. The control-function implementation minimizes external timing requirements.

The SN74ALVCH16863 can be used as two 9-bit transceivers or one 18-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable (OEAB or OEBA) inputs.

DGG OR DL PACKAGE (TOP VIEW)

		U		
1OEAB				1OEBA
1B1 [2		55] 1A1
1B2 🕻	3] 1A2
GND [4		53	GND
1B3 🛚	5		52	1A3
1B4 🛚	6		51] 1A4
v _{cc} [7		50]v _{cc}
1B5 🛚				1A5
1B6 🛚	9		48] 1A6
1B7 🛚	10] 1A7
GND [11		46	GND
1B8 🛚	12] 1A8
1B9 🛚	13] 1A9
GND [14			GND
	15			GND
	16			2A1
2B2	17			2A2
GND	18			GND
2B3	19			2A3
2B4 🛚	20		37]2A4
2B5 🛚	21		36] 2A5
v _{cc} [22		35] v _{cc}
	23		34	2A6
_	24			2A7
GND [25		32	GND
2B8 🛚	26			2A8
2B9 🛚	27		30	2A9
2OEAB	28		29	2 <mark>OEBA</mark>
				-

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

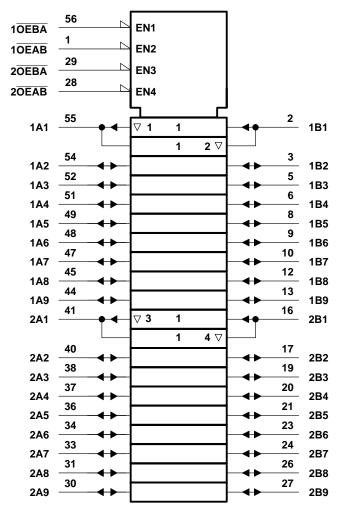
The SN74ALVCH16863 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 9-bit section)

INP	UTS	ODEDATION
OEAB	OEBA	OPERATION
Н	L	B data to A bus
L	Н	A data to B bus
Н	Н	Isolation

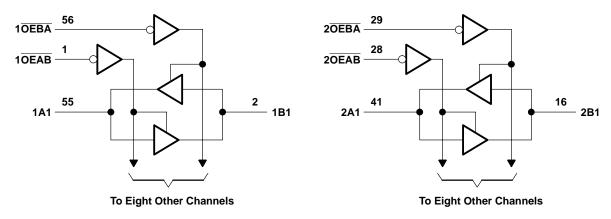
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCES060B - DECEMBER 1995 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage r	ange, V _{CC}	
Input voltage rar	nge, V _I : Except I/O ports (see Note 1)	
	I/O ports (see Notes 1 and 2)	
Output voltage ra	ange, VO (see Notes 1 and 2)	
Input clamp curr	ent, I _{IK} (V _I < 0)	
Output clamp cu	rrent, I _{OK} (V _O < 0)	
Continuous outp	ut current, IO	±50 m/s
Continuous curre	ent through each V _{CC} or GND	±100 m
Package therma	I impedance, θ_{JA} (see Note 3): DGG p	package 81°C/V
		ckage
Storage tempera	ature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
ViH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	Lligh lovel output ourrent	V _{CC} = 2.3 V		-12	mA	
IOH	High-level output current	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		4		
1	Low lovel output ourrent	V _{CC} = 2.3 V		12	A	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
	VOH	$I_{OH} = -6 \text{ mA}$	2.3 V	2				
Vон			2.3 V	1.7			V	
	I _{OH} = -12 mA	2.7 V	2.2					
		3 V	2.4					
		I _{OH} = -24 mA	3 V	2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA	1.65 V			0.45		
\/		I _{OL} = 6 mA	2.3 V			0.4	.,	
VOL		1 40 4	2.3 V			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
IĮ		V _I = V _{CC} or GND	3.6 V			±5	μΑ	
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V	2.3 V	45				
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ	
` ´		V _I = 0.8 V	3 V	75				
		V _I = 2 V	3 V	-75				
		V _I = 0 to 3.6 V [‡]	3.6 V			±500		
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
ΔI _{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5		n.E	
Ci	Data inputs	Al = ACC OF GIAD	3.3 V		6		pF	
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	§	1	4.1		4	1	3.4	ns
t _{en}	OEAB or OEBA	A or B	§	1	5.7		5.8	1	4.7	ns
^t dis	OEAB or OEBA	A or B	§	1.3	5.5		4.7	1.4	4.2	ns

[§] This information was not available at the time of publication.



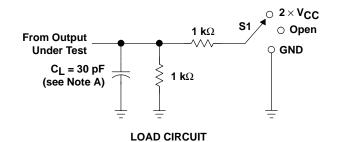
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

operating characteristics, T_A = 25°C

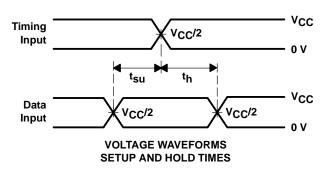
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 \text{ V}$	V _{CC} = 3.3 V	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	UNIT		
<u> </u>	Power dissipation	Outputs enabled	Cı = 50 pF. f = 10 MHz	†	21	30	pF	
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	2	3	рг	

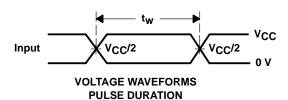
[†] This information was not available at the time of publication.

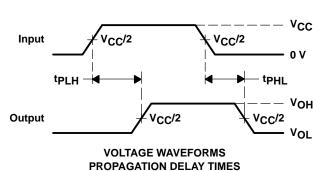
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

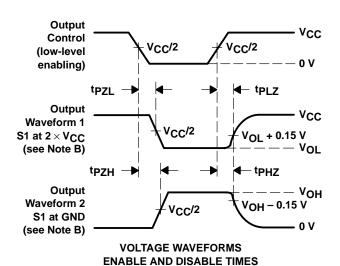










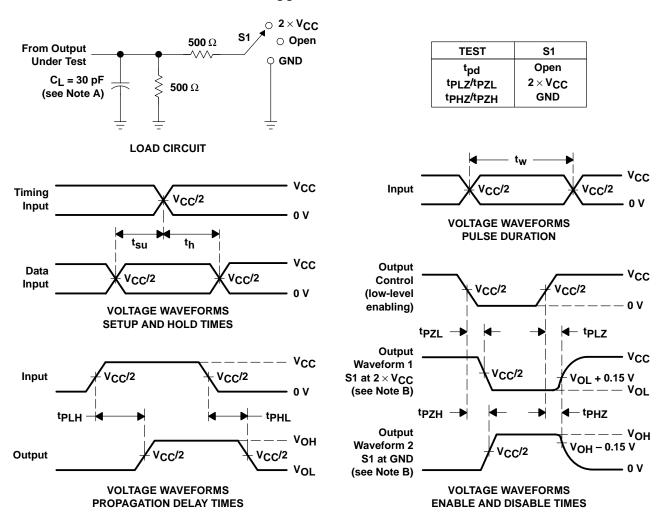


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

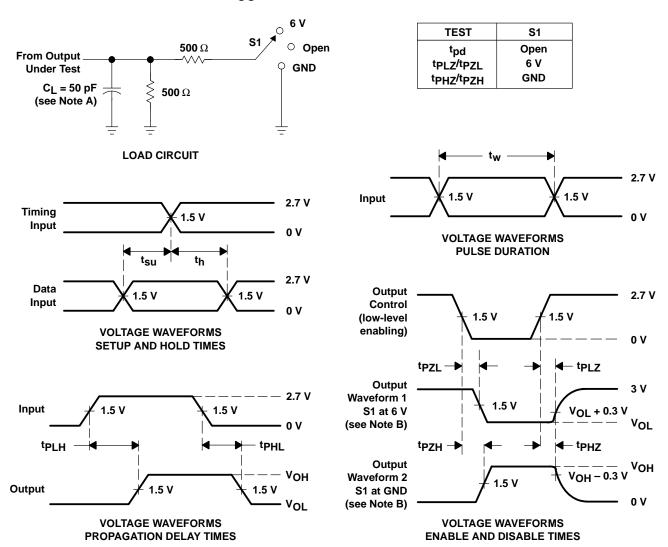


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



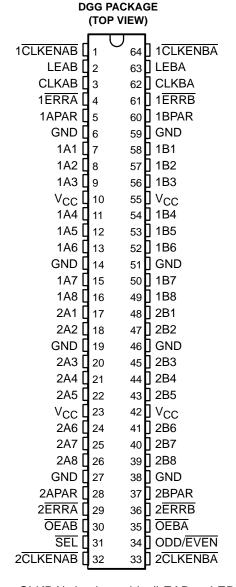
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- **Member of the Texas Instruments** Widebus+™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBT** ™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Simultaneously Generates and Checks **Parity**
- **Option to Select Generate Parity and Check** or Feed-Through Data/Parity in A-to-B or **B-to-A Directions**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- Packaged in Thin Shrink Small-Outline **Package**

description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.



The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable (CLKENAB or CLKENBA) inputs. It also provides parity-enable (SEL) and parity-select (ODD/EVEN) inputs and separate error-signal (ERRA or ERRB) outputs for checking parity. The direction of data flow is controlled by \overline{OEAB} and \overline{OEBA} . When \overline{SEL} is low, the parity functions are enabled. When \overline{SEL} is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to $\sf V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16901 is characterized for operation from –40°C to 85°C.

ISTRUMENTS

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Function Tables

FUNCTION†

	I	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Х	Z
Х	L	Н	Χ	L	L
Х	L	Н	Χ	Н	Н
Н	L	L	Χ	Χ	в ₀ ‡
L	L	L	\uparrow	L	L
L	L	L	\uparrow	Н	Н
L	L	L	L	Χ	в ₀ ‡
L	L	L	Н	Χ	В ₀ §

 $^{^\}dagger$ A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{\text{OEBA}},$ LEBA, and $\overline{\text{CLKENBA}}.$

PARITY ENABLE

	INPUTS		ODED ATION OF	OPERATION OR FUNCTION					
SEL	OEBA	OEAB	OPERATION OF	REUNCTION					
L	Н	L	Parity is checked on port A and is generated on port B.						
L	L	Н	Parity is checked on port B and is generated on port A.						
L	Н	Н	Parity is checked on port B and port A.						
L	L	L	Parity is generated on port A ar	nd B if device is in FF mode.					
Н	L	L		Q _A data to B, Q _B data to A					
Н	L	Н	Parity functions are disabled; device acts as a standard	Q _B data to A					
Н	Н	L	18-bit registered transceiver.	Q _A data to B					
Н	Н	Н	_	Isolation					

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

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Function Tables (Continued)

PARITY

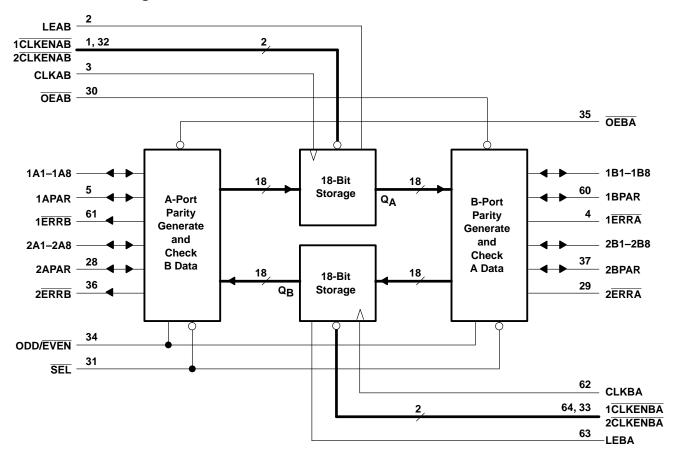
				INPUTS					OUTI	PUTS	S			
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1-A8 = H	Σ OF INPUTS B1-B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB			
L	Н	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	Н	L	Z			
L	Н	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	Н	Z			
L	Н	L	L	0, 2, 4, 6, 8	N/A	Н	N/A	N/A	L	L	Z			
L	Н	L	L	1, 3, 5, 7	N/A	Н	N/A	N/A	Н	Н	Z			
L	L	Н	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	Н			
L	L	Н	L	N/A	1, 3, 5, 7	N/A	L	Н	Z	N/A	L			
L	L	Н	L	N/A	0, 2, 4, 6, 8	N/A	Н	L	Z	N/A	L			
L	L	Н	L	N/A	1, 3, 5, 7	N/A	Н	Н	Z	N/A	Н			
L	Н	L	Н	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	Н	Z			
L	Н	L	Н	1, 3, 5, 7	N/A	L	N/A	N/A	Н	L	Z			
L	Н	L	Н	0, 2, 4, 6, 8	N/A	Н	N/A	N/A	Н	Н	Z			
L	Н	L	Н	1, 3, 5, 7	N/A	Н	N/A	N/A	L	L	Z			
L	L	Н	Н	N/A	0, 2, 4, 6, 8	N/A	L	Н	Z	N/A	L			
L	L	Н	Н	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	Н			
L	L	Н	Н	N/A	0, 2, 4, 6, 8	N/A	Н	Н	Z	N/A	Н			
L	L	Н	Н	N/A	1, 3, 5, 7	N/A	Н	L	Z	N/A	L			
L	Н	Н	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	Н	Z	Н			
L	Н	Н	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L			
L	Н	Н	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	Н	Н	Z	L	Z	L			
L	Н	Н	L	1, 3, 5, 7	1, 3, 5, 7	Н	Н	z	Н	Z	Н			
L	Н	Н	Н	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L			
L	Н	Н	Н	1, 3, 5, 7	1, 3, 5, 7	L	L	z	Н	Z	Н			
L	Н	Н	Н	0, 2, 4, 6, 8	0, 2, 4, 6, 8	Н	Н	z	Н	Z	Н			
L	Н	Н	Н	1, 3, 5, 7	1, 3, 5, 7	Н	Н	z	L	Z	L			
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z			
L	L	L	Н	N/A	N/A	N/A	N/A	РО‡	Z	PO‡	Z			

[†] Parity output is set to the level so that the specific bus side is set to even parity.

[‡] Parity output is set to the level so that the specific bus side is set to odd parity.

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functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
I/O ports (see Notes 1 and 2	
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed..
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

SCES010E - JULY 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
lou	High level output ourrent	V _{CC} = 2.3 V		-12	mA
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA
lOL	Low-level output current	V _{CC} = 2.7 V		12	IIIA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	VCC	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	VCC-0.	.2		
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
VOL		$I_{OL} = 6 \text{ mA}$		2.3 V			0.4	V
VOL		I _{OL} = 12 mA		2.3 V			0.7	V
		IOL = 12 IIIA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	- 75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3		pF
C _{io}	A or B ports	VO = VCC or GND		3.3 V		7.5		pF
Co	ERR ports	VO = VCC or GND		3.3 V		6		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency			†		125		125		125	MHz
	Pulse	CLK↑	†		3		3		3		ns
t _W	duration	LE high	†		3		3		3		110
		A, APAR or B, BPAR before CLK↑	†		1.9		2		1.7		
t _{su}	Setup time	CLKEN before CLK↑	†		2.1		2.1		1.7		ns
		A, APAR or B, BPAR before LE↓	†		1.4		1.3		1.2		
		A, APAR or B, BPAR after CLK↑	†		0.4		0.4		0.5		
t _h	Hold time	CLKEN after CLK↑	†		0.5		0.5		0.7		ns
		A, APAR or B, BPAR after LE↓	†		0.9		1.1		0.9		

[†] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =		UNIT
	(INFOT)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			†		125		125		125		MHz
	A or B	B or A		†	1	5.2		4.8	1	4.4	
	AUIB	BPAR or APAR		†	2	8.9		7.6	2	6.7	
	APAR or BPAR	BPAR or APAR		†	1	5.7		5.2	1	4.7	
	AI AIX OI DI AIX	ERRA or ERRB		†	2	9.7		8.7	2	7.5	
	ODD/EVEN	ERRA or ERRB		†	1.5	8.7		7.9	1.5	6.8	
	ODD/EVEN	BPAR or APAR		†	1.5	8.3		7.6	1.5	6.5	
	SEL	BPAR or APAR		†	1	6.1		5.9	1	5.1	
		A or B		†	1	6.4		5.8	1	5.1	
t _{pd}	CLKAB or CLKBA	BPAR or APAR parity feedthrough		†	1.5	7.1		6.3	1.5	5.6	ns
	CENAB OF CENBA	BPAR or APAR parity generated		†	2.5	10.2		8.7	2	7.7	
		ERRA or ERRB		†	2.5	10.5		8.9	2	7.9	
		A or B		†	1	6		5.5	1	4.8	
	1545 1554	BPAR or APAR parity feedthrough		†	1.5	6.7		6	1.5	5.3	
	LEAB or LEBA	BPAR or APAR parity generated		†	2.5	9.8		8.3	2	7.4	
		ERRA or ERRB		†	2.5	9.9		8.5	2	7.5	
t _{en}	OEAB or OEBA	B, BPAR or A, APAR		†	1.4	6.3		6.1	1	5.3	ns
^t dis	OEAB or OEBA	B, BPAR or A, APAR		†	1.3	6.1		5.2	1.5	4.9	ns
t _{en}	OEAB or OEBA	ERRA or ERRB		†	1.4	6.2		5.5	1	4.9	ns
t _{dis}	OEAB or OEBA	ERRA or ERRB		†	1.3	7.3		6.5	1	5.7	ns
t _{en}	SEL	ERRA or ERRB		†	1.4	6.7		6.5	1	5.5	ns
t _{dis}	SEL	ERRA or ERRB		†	1.3	6.4		5.4	1.5	4.9	ns

[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} = 3.3 V	UNIT
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONII	
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	22	27	pF
Cpd			$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	5	8	þг

[†] This information was not available at the time of publication.

VOLTAGE WAVEFORMS

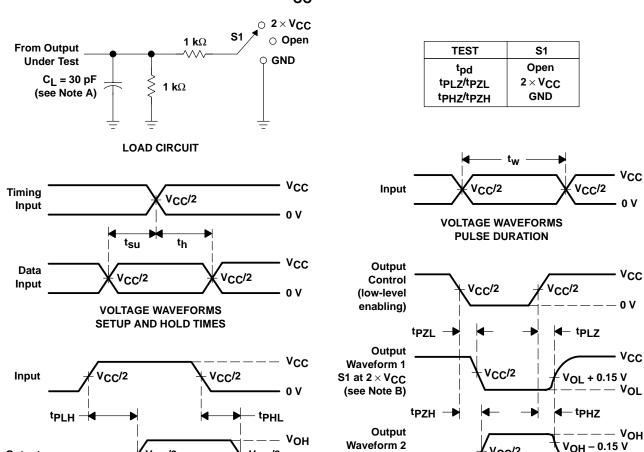
ENABLE AND DISABLE TIMES

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VCC

- 0 V

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



NOTES: A. C_L includes probe and jig capacitance.

Output

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

S1 at GND

(see Note B)

D. The outputs are measured one at a time with one transition per measurement.

 $V_{CC}/2$

E. tpLZ and tpHZ are the same as tdis.

V_{CC}/2

VOLTAGE WAVEFORMS

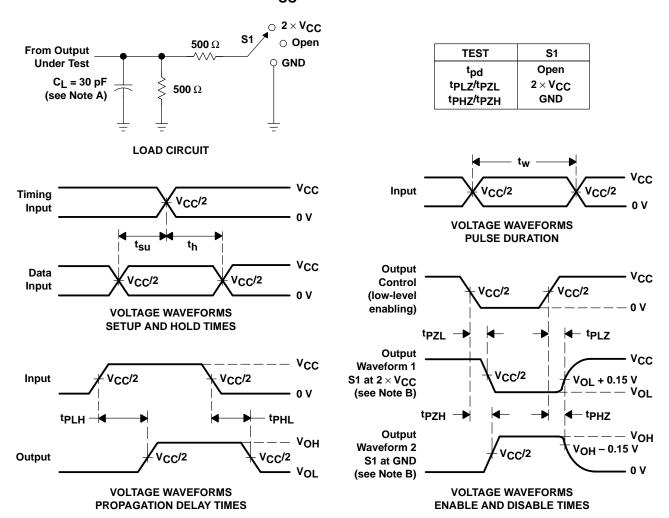
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

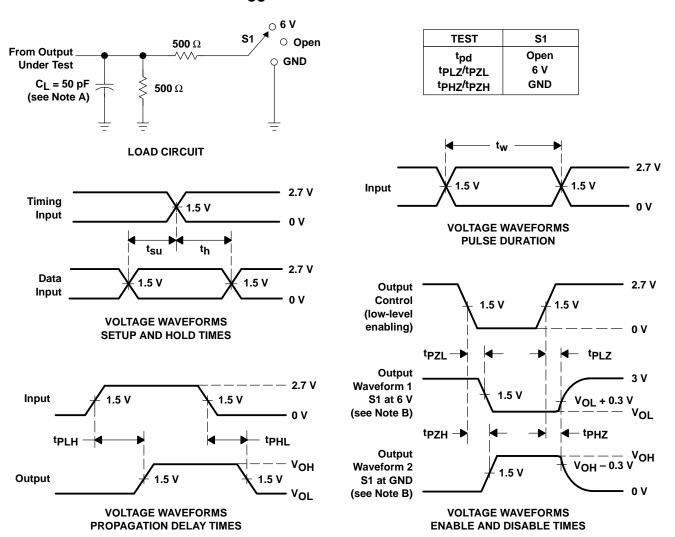


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown Resistors**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

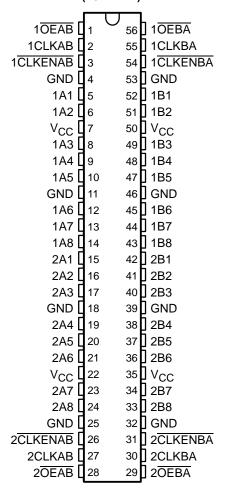
The SN74ALVCH16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. This device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16952 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



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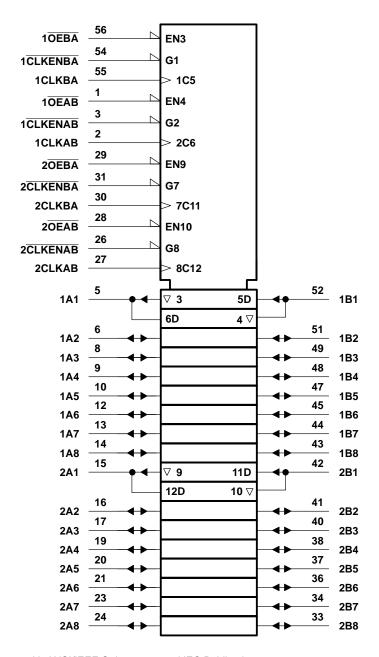
FUNCTION TABLE†

	INPUT	S		OUTPUT		
CLKENAB	CLKAB	CLKAB OEAB A				
Н	Х	L	Χ	в ₀ ‡		
Х	L	L	Χ	в ₀ ‡ в ₀ ‡		
L	\uparrow	L	L	L		
L	\uparrow	L	Н	Н		
Х	X	Н	Χ	Z		

[†] A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA, CLKBA, and OEBA.

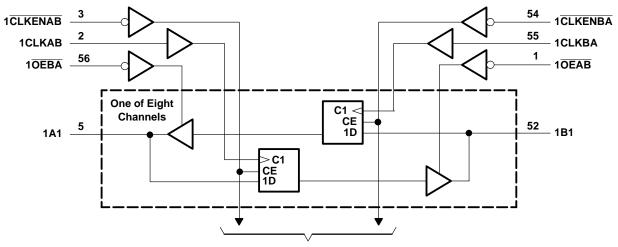
[‡]Level of B before the indicated steady-state input conditions were established

logic symbol†

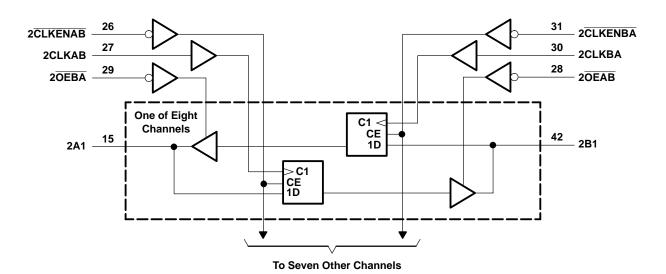


 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG	package 81°C/W
DGV p	package 86°C/W
DL pa	ckage 74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed..
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage	_	1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
1	High lavel autout august	V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Lave lavel autout august	V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	$V_{CC} = 3 V$			24	
Δt/Δν	Input transition rise or fall rate	•		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -4 mA		1.65 V	1.2			
		I _{OH} = -6 mA		2.3 V	2			
Vон				2.3 V	1.7			V
		I _{OH} = -12 mA		2.7 V	2.2			
				3 V	2.4			
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA		1.65 V			0.45	
V		I _{OL} = 6 mA		2.3 V			0.4	V
VOL		lo 12 mΛ		2.3 V			0.7	V
		I _{OL} = 12 mA		2.7 V			0.4	
		I _{OL} = 24 mA		3 V			0.55	
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_I = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ
ΔlCC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		3.5		pF
Cio	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			¶		150		150		150	MHz
tw. Pulse duration	Dulas duration	CLKEN high	¶		3.3		3.3		3.3		ns
t _W	Pulse duration	CLK high or low	¶		3.3		3.3		3.3		115
	Catua tima	Data before CLK	¶		1.7		1.9		1.5		20
^t su	Setup time	CLKEN before CLK	¶		1.2		1		1		ns
+.	th Hold time	Data after CLK	¶		0.6		0.6		0.8		20
۱ ^t h		CLKEN after CLK	¶		1.1		0.9		1.1		ns

This information was not available at the time of publication.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	V _{CC} = 1.8 V		$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \text{ V}$ 0.3 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX		
f _{max}			†		150		150		150		MHz	
^t pd	CLK	A or B		†	1	4.1		4.6	1	3.9	ns	
t _{en}	OEBA or OEAB	A or B		†	1	5.4		5.3	1	4.4	ns	
^t dis	OEBA or OEAB	A or B		†	1	5.3		4.4	1.1	4	ns	

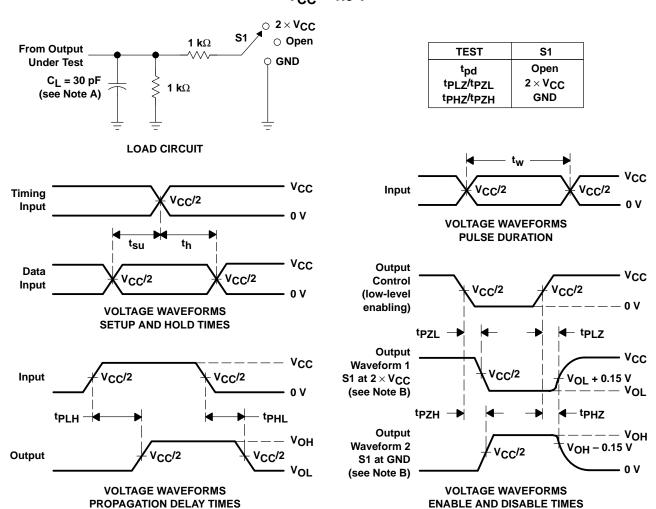
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	TANAMETER	_	TEST CONDITIONS	TYP	TYP	TYP	ONIT	
	Power dissipation	Outputs enabled	C 0	†	53	71	pF	
C _{pd}	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	34	40	l br	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$

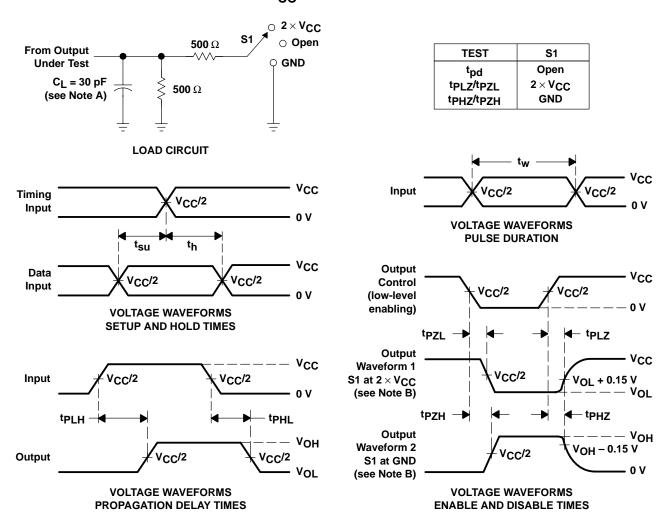


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



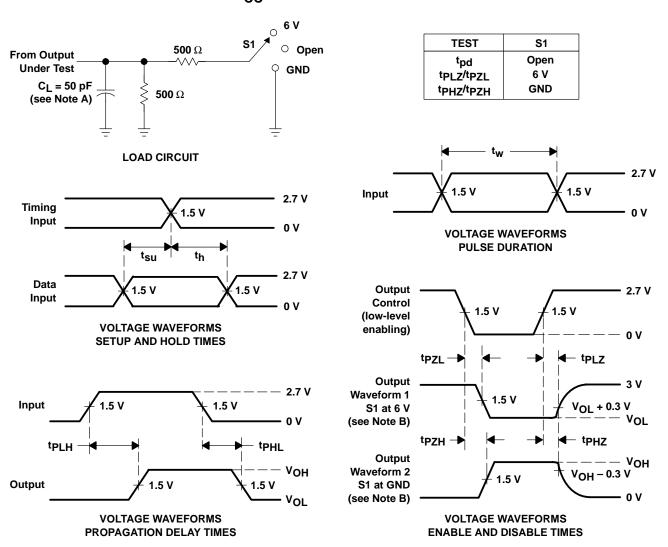
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH32501 36-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPL

SCES144A - OCTOBER 1998 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBT**™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

description

This 36-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

This device can be used as two 18-bit transceivers or one 36-bit transceiver. Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

To ensure the high-impedance state during power up or power down, $\overline{\mathsf{OEBA}}$ should be tied to V_CC through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH32501 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE[†]

	INPUTS								
OEAB	LEAB	CLKAB	Α	В					
L	Х	Х	Χ	Z					
Н	Н	Χ	L	L					
Н	Н	Χ	Н	Н					
Н	L	\uparrow	L	L					
Н	L	\uparrow	Н	Н					
Н	L	L or H	Χ	в ₀ ‡					

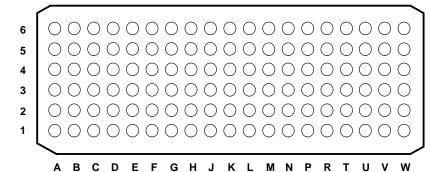
[†]A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

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[‡]Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low

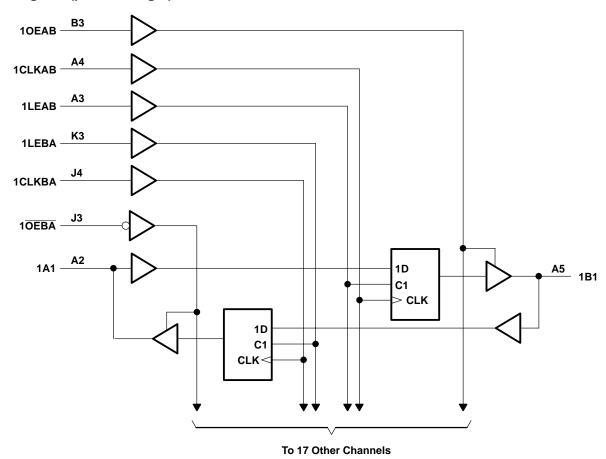
GKF PACKAGE (TOP VIEW)



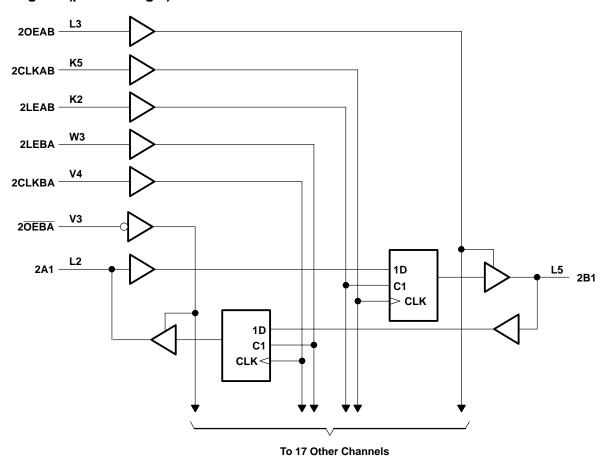
terminal assignments

6	1B2	1B4	1B6	1B8	1B10	1B12	1B14	1B15	1B17	NC	2B2	2B4	2B6	2B8	2B10	2B12	2B14	2B15	2B17
5	1B1	1B3	1B5	1B7	1B9	1B11	1B13	1B16	1B18	2CLKAB	2B1	2B3	2B5	2B7	2B9	2B11	2B13	2B16	2B18
4	1CLKAB	GND	GND	VCC	GND	GND	VCC	GND	1CLKBA	GND	GND	GND	Vcc	GND	GND	VCC	GND	2CLKBA	GND
3	1LEAB	10EAB	GND	VCC	GND	GND	VCC	GND	1OEBA	1LEBA	20EAB	GND	Vcc	GND	GND	VCC	GND	2OEBA	2LEBA
2	1A1	1A3	1A5	1A7	1A9	1A11	1A13	1A16	1A18	2LEAB	2A1	2A3	2A5	2A7	2A9	2A11	2A13	2A16	2A18
1	1A2	1A4	1A6	1A8	1A10	1A12	1A14	1A15	1A17	NC	2A2	2A4	2A6	2A8	2A10	2A12	2A14	2A15	2A17
	Α	В	С	D	Е	F	G	Н	J	K	L	М	N	Р	R	T	U	V	W

logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	39°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT		
Vcc	Supply voltage		1.65	3.6	V		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}				
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V		
	V _{IH} High-level input voltage V _{IL} Low-level input voltage V _I Input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2				
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$			
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8			
٧ı	Input voltage		0	VCC	V		
٧o	Output voltage		0	VCC	V		
		V _{CC} = 1.65 V		-4			
	I Park Toward and account	V _{CC} = 2.3 V		-12	m Λ		
ЮН	nign-iever output current	V _{CC} = 2.7 V		-12	mA		
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	V _{CC} = 3 V		-24			
		V _{CC} = 1.65 V		4			
la.	Low lovel output ourrent	V _{CC} = 2.3 V		12	mA		
IOL	Low-level output current	V _{CC} = 2.7 V		12			
		V _{CC} = 3 V		24			
Δt/Δν	Input transition rise or fall rate			10	ns/V		
TA	Operating free-air temperature		-40	85	°C		

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	V _{CC} -0	.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3 V	2			
Vон			2.3 V	1.7			V
		$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 4 mA	1.65 V			0.45	
1/		I _{OL} = 6 mA	2.3 V			0.4	V
VOL		10 1	2.3 V			0.7	V
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
lį		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	4.05.1/	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	227	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	2.1/	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V [‡]	3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μА
ΔlCC		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V				pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\colored}$ For I/O ports, the parameter IOZ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequence	су										MHz	
too	Pulse duration	LE high										ns	
t _W		CLK high or low										115	
		Data before CLK↑											
t _{su}	Setup time	Data before LE	CLK high									ns	
		Data before LE↓ CLK low	CLK low										
4.	I laid time	Data after CLK↑										20	
t _h	Hold time	Data after LE↓	CLK high or low									ns	

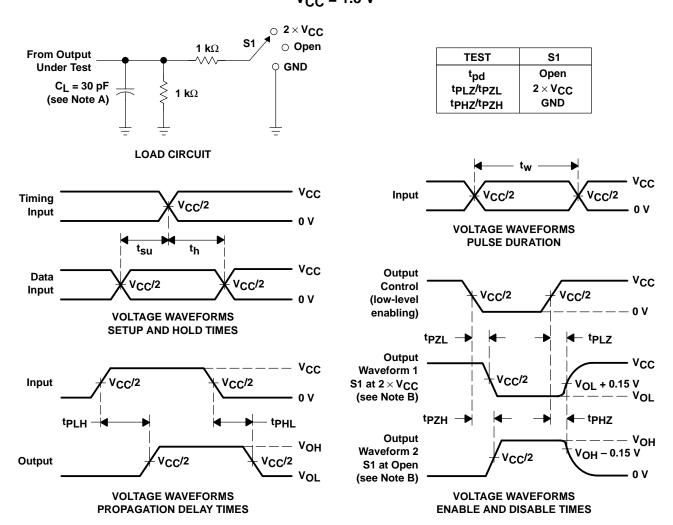
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
	A or B	B or A									
t _{pd}	LE										ns
	CLK	A or B									
t _{en}	OEAB	В									ns
t _{dis}	OEAB	В									ns
t _{en}	OEBA	А									ns
t _{dis}	OEBA	Α									ns

operating characteristics, T_A = 25°C

ſ	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	V _{CC} = 3.3 V	UNIT	
			TEST CONDITIONS	TYP	TYP TYP			
Γ	<u> </u>	Power dissipation	Outputs enabled	Cı = 0. f = 10 MHz				pF
	Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$				рΓ

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

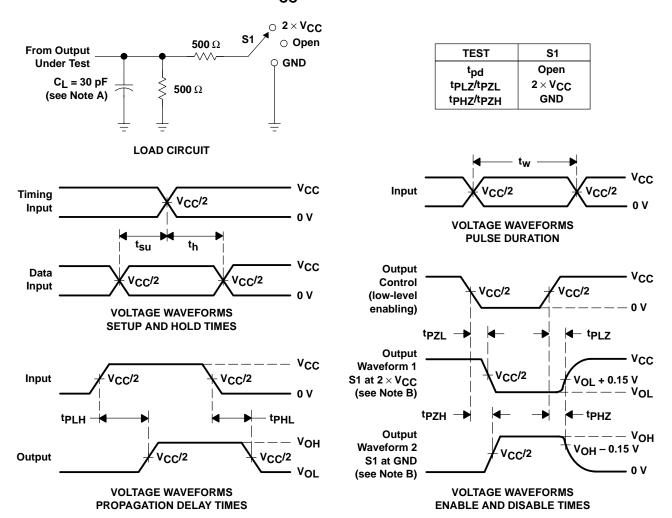


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns. $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



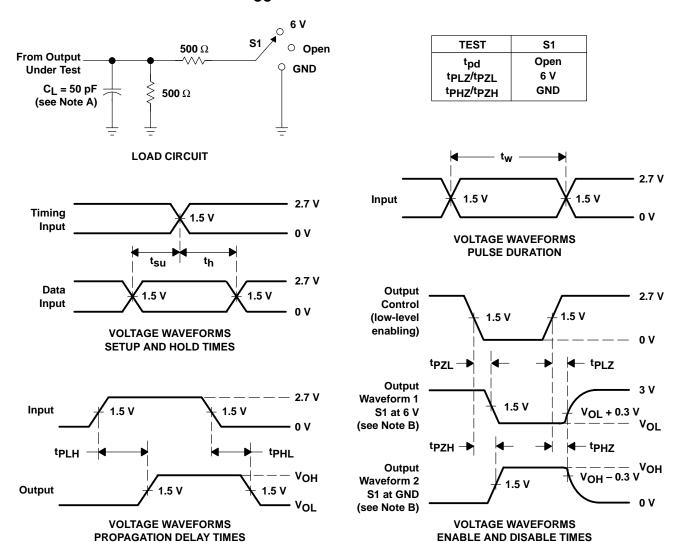
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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DGG OR DL PACKAGE

(TOP VIEW)

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 1.65-V to $3.6\text{-V}\ \text{V}_{CC}$ operation.

The SN74ALVCH162244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low outputenable (\overline{OE}) inputs.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162244 is characterized for operation from -40°C to 85°C.

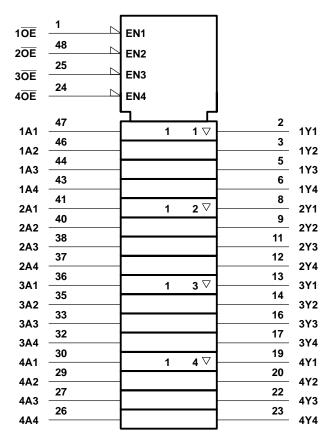
1OE 48 20E 47 1 1A1 1Y1 🛮 2 1Y2 🛮 3 46∏ 1A2 GND []4 45 GND 1Y3 **∏** 5 44**∏** 1A3 1Y4 **[**] 6 43 1A4 42 V_{CC} v_{cc} [2Y1 **[**] 8 41 **∏** 2A1 2Y2 **1**9 40 2A2 GND 🛮 10 39 GND 2Y3 38 2A3 11 2Y4 [] 12 37 D 2A4 3Y1 II 13 36 II 3A1 3Y2 [14 35 🛮 3A2 GND 🛮 15 34 GND 3Y3 **∏** 16 33 II 3A3 3Y4 [17 32 | 3A4 ∨cc 🏻 18 31 V_{CC} 4Y1 **1**19 30 4A1 4Y2 **∏** 20 29**∏** 4A2 GND [] 21 28 GND 4Y3 **∏** 22 27 T 4A3 4Y4 **[**] 23 26 **1** 4A4 40E **1**24 25 3OE

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FUNCTION TABLE (each 4-bit buffer)

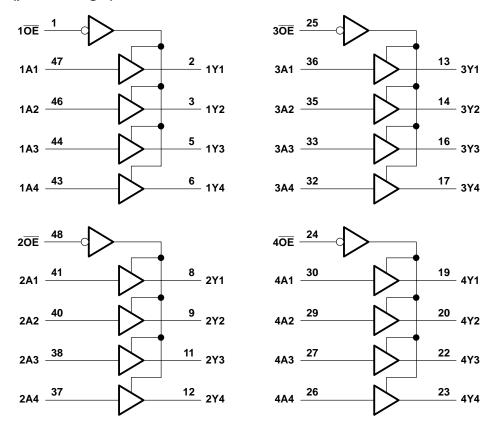
INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
	LP-sh level vertext come of	V _{CC} = 1.65 V		-2		
1		V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
la.	Low-level output current	V _{CC} = 2.3 V		6	mA	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		8	IIIA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		VCC	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -4 mA		2.3 V	1.9			
Vон		I _{OH} = -6 mA		2.3 V	1.7			V
		IOH = -0 IIIA		3 V	2.4			
		I _{OH} = –8 mA		2.7 V	2			
		I _{OH} = -12 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.4	
VOL		1 C A		2.3 V			0.55	V
		$I_{OL} = 6 \text{ mA}$		3 V			0.55	
		I _{OL} = 8 mA		2.7 V			0.6	
		I _{OL} = 12 mA		3 V			0.8	
IĮ		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ
, ,		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75	-		
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μА
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs			227		3		~F
Ci				3.3 V		6		pF
Со	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	§	1	4.9		4.7	1	4.2	ns
t _{en}	ŌĒ	Y	§	1	6.8		6.7	1	5.6	ns
^t dis	ŌĒ	Υ	§	1	6.3		5.7	1	5.5	ns

[§] This information was not available at the time of publication.



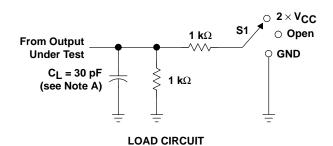
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

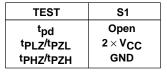
operating characteristics, $T_A = 25^{\circ}C$

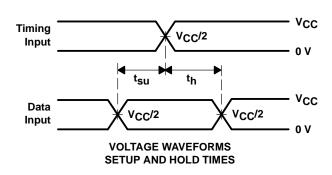
	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
	. Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	16	19	n.E
L	pd capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	5	pF

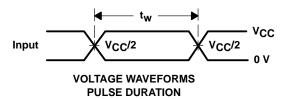
[†] This information was not available at the time of publication.

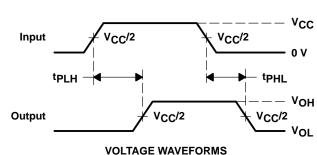
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



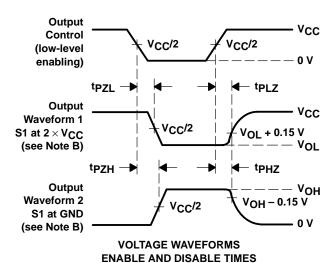








PROPAGATION DELAY TIMES

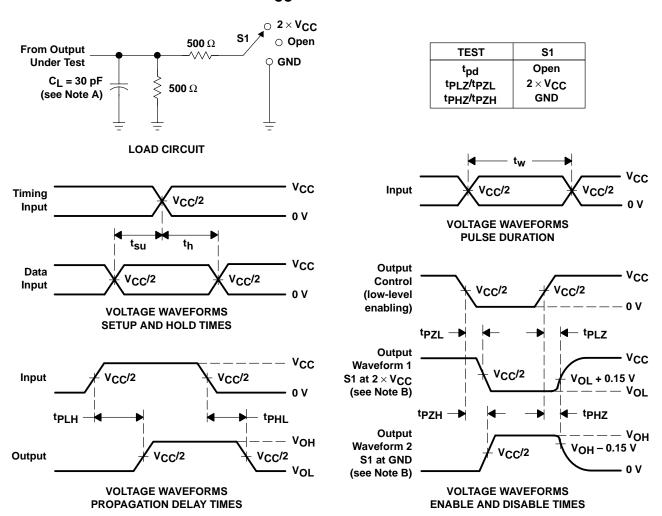


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



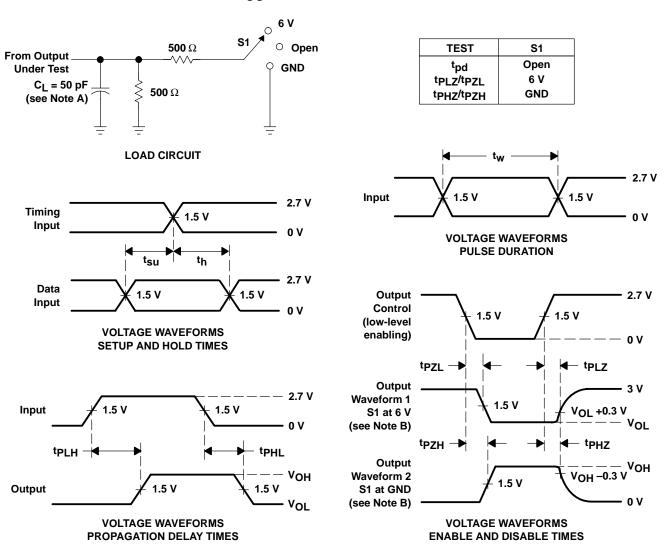
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns.}$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For order entry:

The DGG package is abbreviated to G.

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V $\rm V_{CC}$ operation.

The SN74ALVCHR162245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162245 is characterized for operation from -40°C to 85°C.

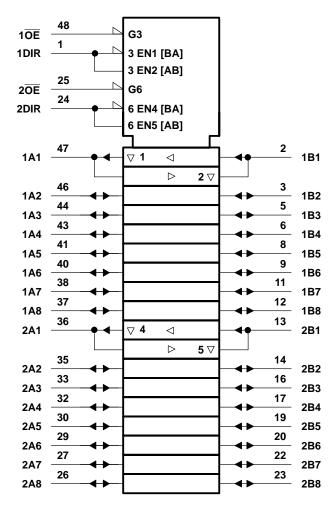
48 1 1 OE 1DIR L 1B1 📙 2 47 1 1A1 46 1 1A2 1B2 | 3 GND L 4 45 GND 1B3 🛮 5 44 🛮 1A3 1B4 🛮 6 43 1 1A4 42 V_{CC} V_{CC} **Ц** 7 1B5 🛮 8 41 1 1A5 1B6 🛮 9 40 L 1A6 39 GND GND | 10 1B7 [11 38 🛮 1A7 1B8 🛮 12 37 L 1A8 2B1 13 36 2A1 2B2 1 14 35 2A2 GND II 15 34 II GND 2B3 16 33 2A3 2B4 🛮 17 32 D 2A4 V_{CC} Ц 18 31 V_{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 🛮 22 27 2A7 2B8 🛮 23 26 2A8 25 20E 2DIR | 24

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FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION			
OE	DIR	OPERATION			
L	L	B data to A bus			
L	Н	A data to B bus			
Н	Χ	Isolation			

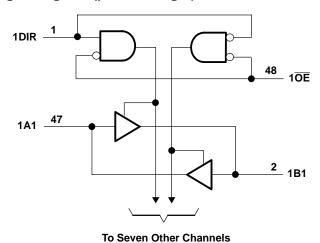
logic symbol†

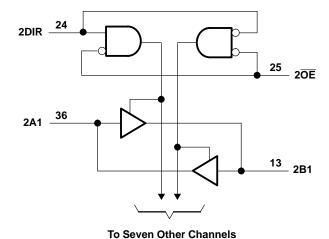


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
lau	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-6	mA	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8		
V _{IL}		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
la.	Low-level output current	V _{CC} = 2.3 V		6	4	
OL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		8	mA	
		V _{CC} = 3 V		12	1	
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -4 mA		2.3 V	1.9			
Vон		I _{OH} = -6 mA		2.3 V	1.7			V
		IOH = -0 IIIA		3 V	2.4			
		I _{OH} = -8 mA		2.7 V	2			
		I _{OH} = -12 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		$I_{OL} = 2 \text{ mA}$		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.4	
VOL		I _{OL} = 6 mA		2.3 V			0.55	V
				3 V			0.55	
		$I_{OL} = 8 \text{ mA}$		2.7 V			0.6	
		$I_{OL} = 12 \text{ mA}$		3 V			0.8	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.05 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.5 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V]	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ
∆lcc		One input at V_{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		9		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	¶	1	4.9		4.7	1	4.2	ns
^t en	ŌĒ	B or A	¶	1	6.8		6.7	1	5.6	ns
^t dis	ŌĒ	B or A	¶	1	6.3		5.7	1	5.5	ns

 $[\]P$ This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

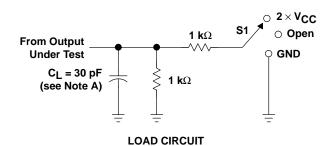
 $[\]mbox{\$}$ For I/O ports, the parameter $\mbox{I}_{\mbox{OZ}}$ includes the input leakage current.

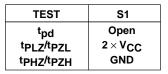
operating characteristics, $T_A = 25^{\circ}C$

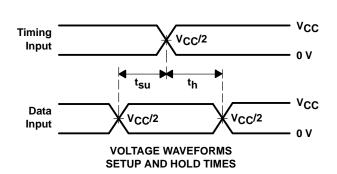
		PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
	· .	Power dissipation	Outputs enabled	C. FO. T. 1 10 MILE	†	24	32	~F	
L	pd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	5	pF	

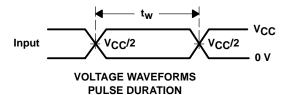
[†] This information was not available at the time of publication.

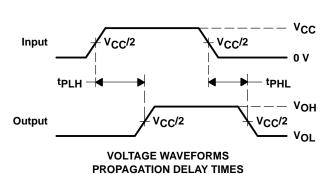
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

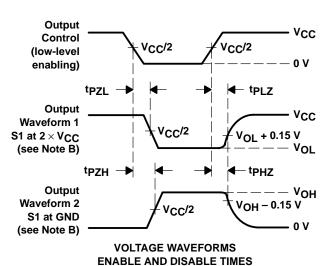










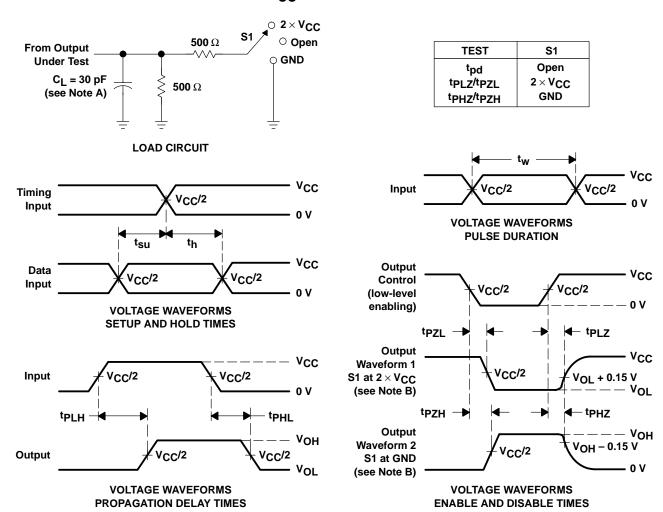


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



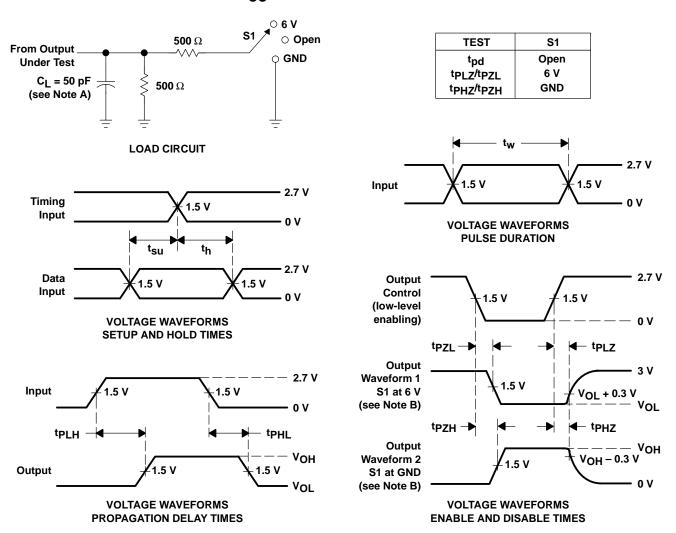
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpz and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{r} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

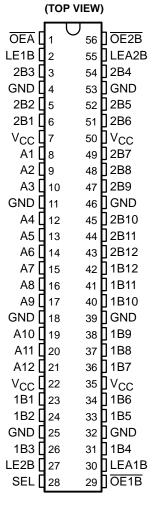
SCAS570G - MARCH 1996 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω
 Series Resistors, So No External Resistors
 Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic Shrink Small-Outline (DL) Packages

description

This 12-bit to 24-bit multiplexed D-type latch is designed for 1.65-V to 3.6- V_{CC} operation.

The SN74ALVCH162260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory-interleaving applications.



Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162260 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

Function Tables

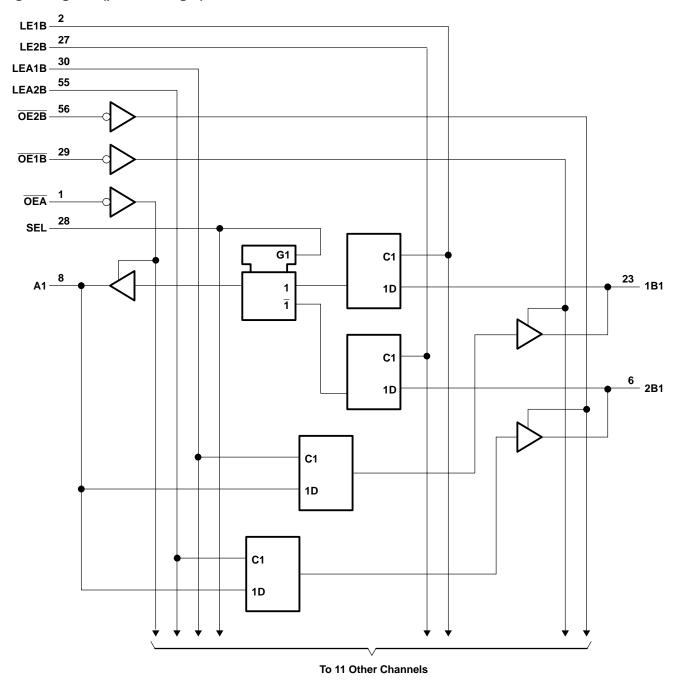
B TO A (OEB = H)

	INPUTS						
1B	2B	SEL	LE1B	LE2B	OEA	Α	
Н	Х	Н	Н	Х	L	Н	
L	Χ	Н	Н	X	L	L	
Х	Χ	Н	L	Χ	L	A ₀	
Х	Н	L	X	Н	L	Н	
Х	L	L	X	Н	L	L	
Х	Χ	L	Χ	L	L	A ₀	
Х	Χ	Χ	X	X	Н	Z	

A TO B (OEA = H)

	(02.1 – 1.1)							
			OUTI	PUTS				
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B		
Н	Н	Н	L	L	Н	Н		
L	Н	Н	L	L	L	L		
Н	Н	L	L	L	Н	2B ₀		
L	Н	L	L	L	L	2B ₀		
Н	L	Н	L	L	1B ₀	Н		
L	L	Н	L	L	1B ₀	L		
Х	L	L	L	L	1B ₀	2B ₀		
Х	Χ	Χ	Н	Н	Z	Z		
Х	Χ	Χ	L	Н	Active	Z		
Х	Χ	Χ	Н	L	Z	Active		
Х	X	X	L	L	Active	Active		

logic diagram (positive logic)





SN74ALVCH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package	
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS570G - MARCH 1996 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	٧
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-4	
	High-level output current (A port)	V _{CC} = 2.3 V		-12	mA
	High-level output current (A port)	$V_{CC} = 2.7 \text{ V}$		-12	
la		V _{CC} = 3 V		-24	
IOH		V _{CC} = 1.65 V		-2	
	High-level output current (B port)	V _{CC} = 2.3 V		-6	
		$V_{CC} = 2.7 V$		-8	
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		4	
	Low level output ourrent (A port)	V _{CC} = 2.3 V		12	
	Low-level output current (A port)	$V_{CC} = 2.7 \text{ V}$		12	
la.		V _{CC} = 3 V		24	A
lOL		V _{CC} = 1.65 V		2	mA
	Low-level output current (B port)	V _{CC} = 2.3 V		6	
	Low-level output current (B port)	$V_{CC} = 2.7 V$		8	
	V _{CC} = 3 V			12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -6 \text{ mA}$	2.3 V	2				
	A port		2.3 V	1.7				
		I _{OH} = -12 mA	2.7 V	2.2				
			3 V	2.4				
.,		I _{OH} = -24 mA	3 V	2			.,	
Vон		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2		V	
		I _{OH} = -2 mA	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
	B port		2.3 V	1.7				
		IOH = -6 mA	3 V	2.4				
		I _{OH} = -8 mA		2				
		I _{OH} = -12 mA	3 V	2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
A port		I _{OL} = 4 mA	1.65 V			0.45		
		I _{OL} = 6 mA	2.3 V			0.4		
	A port		2.3 V			0.7	1	
		$I_{OL} = 12 \text{ mA}$	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
VOL		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V	
		I _{OL} = 2 mA	1.65 V			0.45		
		I _{OL} = 4 mA	2.3 V			0.4		
	B port		2.3 V			0.55		
		I _{OL} = 6 mA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6		
		I _{OL} = 12 mA	3 V			0.8		
lį	•	V _I = V _{CC} or GND	3.6 V			±5	μΑ	
-		V _I = 0.58 V		25			<u> </u>	
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V		45				
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ	
.()		V _I = 0.8 V		75				
		V _I = 2 V	3 V	-75				
		V _I = 0 to 3.6 V [‡]	3.6 V			±500		
loz§		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
ICC		$V_{I} = V_{CC}$ or GND, $I_{O} = 0$	3.6 V			40	<u>.</u> μΑ	
ΔlCC		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	<u>.</u> μΑ	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5		pF	
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		4.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		†		150		150		150	MHz
t _W	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	†		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B	†		1.4		1.1		1.1		ns
th	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B	†		1.6		1.9		1.5		ns

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPOT)		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А	В		†	1	5.9		5.8	1.2	4.9	
	В	А		†	1	5.7		5.1	1.2	4.3	ns
^t pd	LE	Α		†	1	5.6		5.2	1	4.4	
	LE	В		†	1	6.1		5.9	1	5	
	SEL	Α		†	1	6.9		6.6	1.1	5.6	
+		Α		†	1	6.7		6.4	1	5.4	no
^t en	ŌĒ	В		†	1	7.2		7.1	1	6	ns
+	<u> </u>	А		†	1	5.7		5	1.3	4.6	no
^t dis	ŌĒ	В		†	1	6.2		5.5	1.3	5.1	ns

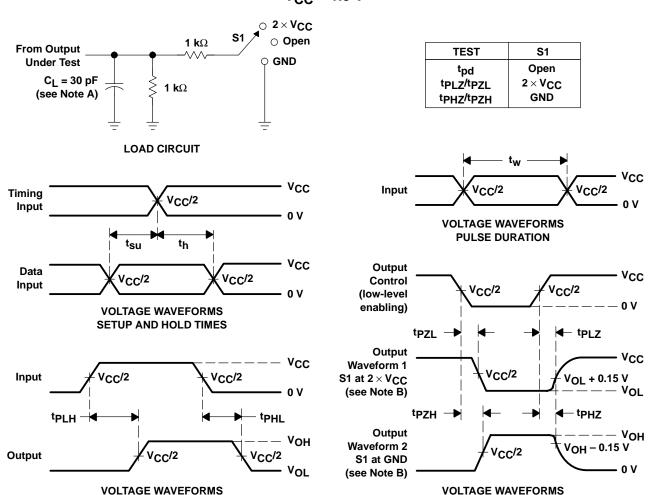
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V _{CC} = 1.8 V	V _{CC} = 2.5 V	VCC = 3.3 V	UNIT	
	FARAMETER		TEST CONDITIONS		TYP	TYP	TYP	UNII	
	Power dissipation	All outputs enabled	C. F0 pF	f 10 MH-	†	37	41	~ F	
C _{pd}	capacitance	All outputs disabled	$C_L = 50 pF$,	f = 10 MHz	†	4	7	pF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

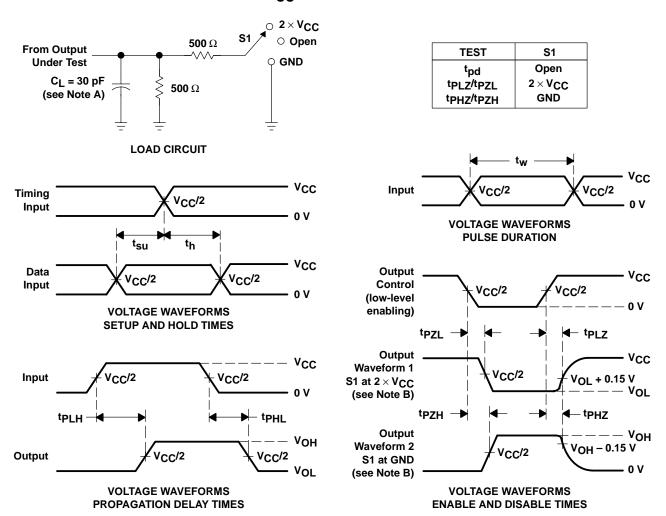
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



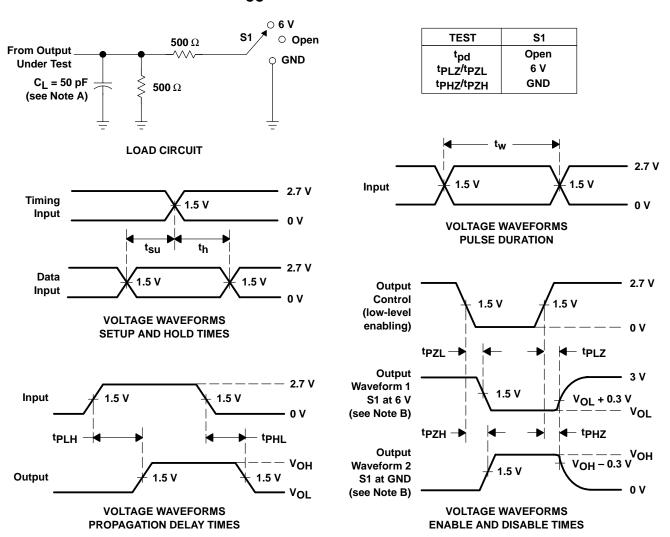
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl H and tpHI are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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42 1B12

41 **∏** 1B11

40 **∏** 1B10

39 | GND

30 CLKENA1

29 TCLK

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- B-Port Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Shrink** Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162268 is used for applications in which data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

(TOP VIEW) 56 OEB **OEA** CLKEN1B 2 55 CLKENA2 2B3 **∏**3 54**∏**2B4 53 GND GND ∏4 2B2 🛮 5 52 **∏** 2B5 51 2B6 2B1 **[**] 6 V_{CC} **□**7 50 VCC A1 **∏**8 49 **∏** 2B7 A2 🛮 9 48 2B8 A3 110 47 **∏** 2B9 GND 11 46∏GND 45 2B10 A4 🛮 12 44 **∏** 2B11 A5 | 13 43 2B12 A6 🛮 14

DGG OR DL PACKAGE

A10 **∏** 19 38**∏**1B9 37 1B8 A11 1 20 A12 21 36 🛮 1B7 V_{CC} [] 22 35 V_{CC} 1B1 **[**] 23 34**∏**1B6 1B2 [] 24 33 🛮 1B5 GND II 25 32 | GND 1B3 **∏**26 31 **1** 1B4

A7 🛮 15

A8 ∏ 16

A9 🛮 17

GND ∏18

CLKEN2B 27

SEL [

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of these inputs allows two seguential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include equivalent $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to OE being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162268 is characterized for operation from -40°C to 85°C.

Function Tables OUTPUT ENABLE

	INPUTS	OUTPUTS			
CLK	OEA	OEB	Α	1B, 2B	
1	Н	Н	Z	Z	
1	Н	L	Z	Active	
1	L	Н	Active	Z	
↑	L	L	Active	Active	

A-TO-B STORAGE (OEB = L)

	OUTPUTS				
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ ‡	2B ₀ ‡
L	L	\uparrow	L	L†	Х
L	L	\uparrow	Н	H [†]	Х
Х	L	\uparrow	L	Х	L
Х	L	\uparrow	Н	Х	Н

[†]Two CLK edges are needed to propagate data.

B-TO-A STORAGE (OEA = L)

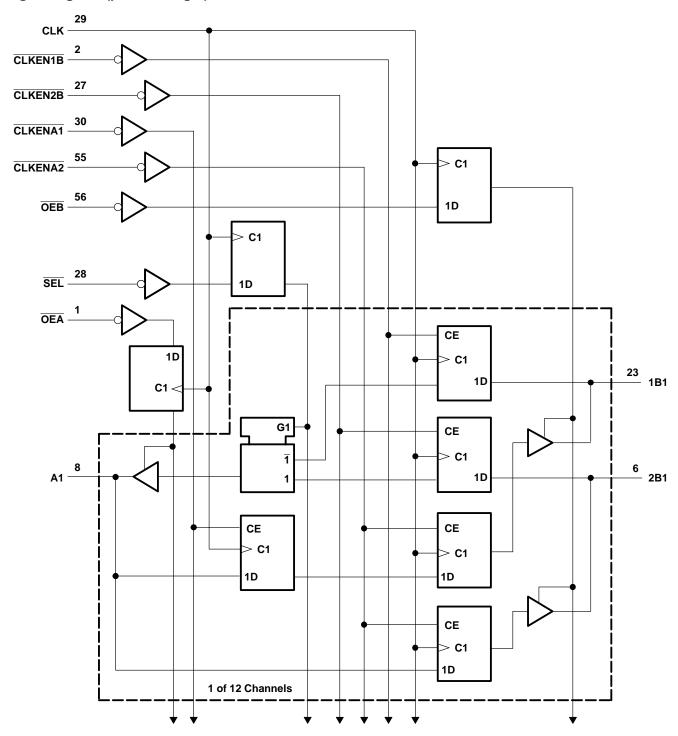
		-	-			
	OUTPUT					
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	Α
Н	Х	Χ	Н	Χ	Х	A ₀ ‡
X	Н	Χ	L	Χ	Χ	A ₀ ‡
L	L	\uparrow	Н	L	Χ	L
L	L	\uparrow	Н	Н	X	Н
Х	L	\uparrow	L	Χ	L	L
Х	L	\uparrow	L	Χ	Н	Н

[‡]Output level before the indicated steady-state input conditions were established



[‡]Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)





SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES018F - AUGUST 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	٧	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
\vee_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧I	Input voltage		0	VCC	٧	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	High-level output current (A port)	V _{CC} = 2.3 V		-12	mA	
	High-level output current (A port)	V _{CC} = 2.7 V		-12		
1		V _{CC} = 3 V		-24		
ЮН		V _{CC} = 1.65 V		-2		
	High-level output current (B port)	V _{CC} = 2.3 V		6		
		V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		4		
	Low lovel output ourrent (A port)	V _{CC} = 2.3 V		12		
	Low-level output current (A port)	V _{CC} = 2.7 V		12		
1		V _{CC} = 3 V		24	A	
lOL		V _{CC} = 1.65 V		2	mA	
	Law lavel autout august (Disagt)	V _{CC} = 2.3 V		6		
	Low-level output current (B port)	V _{CC} = 2.7 V		8		
	VCC = 3 V			12		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	VCC	MIN TYP	† MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2		
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
		I _{OH} = -6 mA	2.3 V	2		
	A port		2.3 V	1.7		
		I _{OH} = -12 mA	2.7 V	2.2		
			3 V	2.4		
,,		I _{OH} = -24 mA	3 V	2		.,
VOH		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2		V
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2		
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9		
	B port		2.3 V	1.7		
		IOH = -6 mA	3 V	2.4		
		$I_{OH} = -8 \text{ mA}$	2.7 V	2		
		I _{OH} = -12 mA	3 V	2		
		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
		I _{OL} = 4 mA	1.65 V		0.45	
		I _{OL} = 6 mA	2.3 V		0.4	
A port		2.3 V		0.7		
		I _{OL} = 12 mA	2.7 V		0.4	
		I _{OL} = 24 mA	3 V		0.55	
VOL		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	V
		I _{OL} = 2 mA	1.65 V		0.45	
		I _{OL} = 4 mA	2.3 V		0.4	
	B port	J C	2.3 V		0.55	
		IOL = 6 mA	3 V		0.55	
		I _{OL} = 8 mA	2.7 V		0.6	
		I _{OL} = 12 mA	3 V		0.8	
IĮ		V _I = V _{CC} or GND	3.6 V		±5	μΑ
		V _I = 0.58 V	4.05.1/	25		
		V _I = 1.07 V	1.65 V	-25		
		V _I = 0.7 V	221/	45		
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45		μΑ
		V _I = 0.8 V	0.1/	75		
		V _I = 2 V	3 V	-75		
		V _I = 0 to 3.6 V [‡]	3.6 V		±500	
l _{OZ} §		$V_O = V_{CC}$ or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔlCC		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	3.	5	pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		9	pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V			V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency			†		120		125		150	MHz
t _W	Pulse durati	on, CLK high or low	†		3.3		3.3		3.3		ns
		A data before CLK↑	†		4.5		4		3.4		
		B data before CLK↑	†		0.8		1.2		1		ns
	Setup time	SEL before CLK↑	†		1.4		1.6		1.3		
t _{su}		CLKENA1 or CLKENA2 before CLK↑	†		3.6		3.4		2.8		
		CLKENB1 or CLKENB2 before CLK↑	†		3.2		3		2.5		
		OE before CLK↑	†		4.2		3.9		3.2		
		A data after CLK↑	†		0		0		0.2		
		B data after CLK↑	†		1.3		1.2		1.3		
	l lalal dias s	SEL after CLK↑	†		1		1		1		
t _h	Hold time	CLKENA1 or CLKENA2 after CLK↑	†		0.1		0.1		0.4		ns
		CLKENB1 or CLKENB2 after CLK↑	†		0.1		0		0.5		
		OE after CLK↑ after CLK↑	†		0		0		0.2		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(INFO1)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		125		150		MHz
		В		†	1.6	6.1		5.9	1.8	5.4	
. .		A (1B)		†	1.6	5.8		5.4	1.7	4.8	no
^t pd	CLK	A (2B)		†	1.6	5.8		5.3	1.8	4.8	ns
		A (SEL)		†	2.5	7.3		6.5	2.4	5.8	
t _{en}	CLK	В		†	2.7	7.2		6.8	2.6	6.1	ns
^t dis	CLK	В		†	2.8	7.2		6.1	2.5	5.9	ns
^t en	CLK	А		†	2	6.2		5.6	1.8	5.1	ns
^t dis	CLK	А		†	2	6.5		5.4	2.1	5	ns

[†] This information was not available at the time of publication.

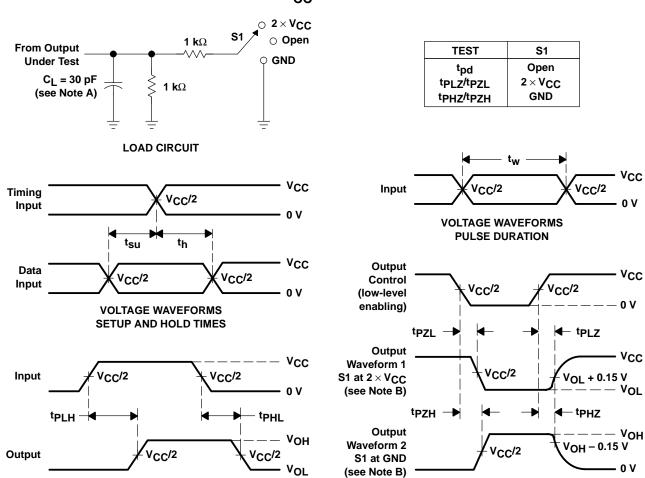
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	†	87	120	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	80.5	118	pr

[†] This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

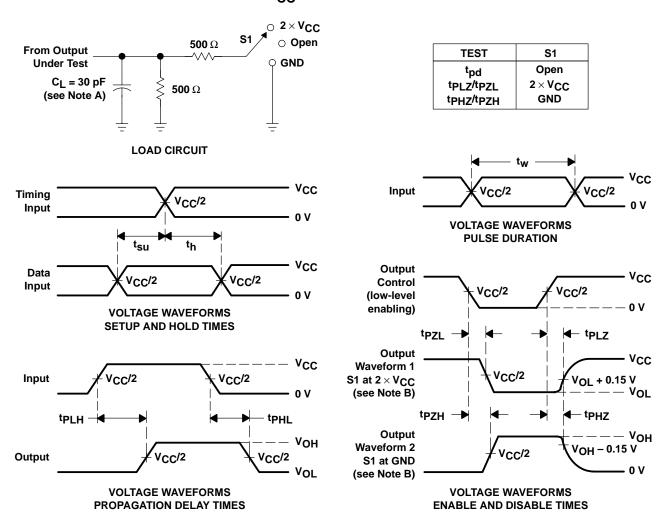
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

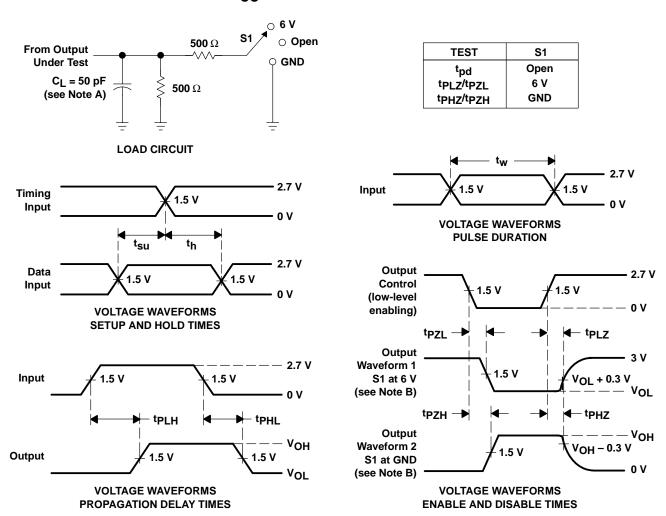


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCHR162282 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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EPIC™ (Enhanced-Performance Implanted **CMOS) Sub-Micron Process**

- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **Member of the Texas Instruments** Widebus™ Family
- **Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown** Resistors
- **Packaged in Thin Shrink Small-Outline Package**

NOTE: For order entry:

The DBB package is abbreviated to G.

description

The SN74ALVCHR162282 is an 18-bit to 36-bit registered bus exchanger designed for 1.65-V to 3.6-V V_{CC} operation.

This part is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, select (SEL) line selects 1B or 2B data for the A outputs.

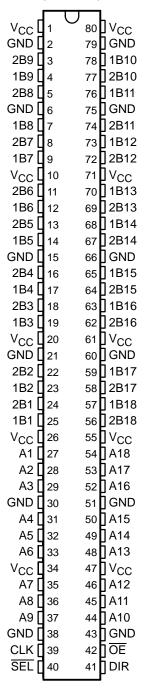
For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable (\overline{OE}) and the control (DIR) input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

The outputs, which are designed to sink up to 12mA, include 26- Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162282 is characterized for operation from -40°C to 85°C.

DBB PACKAGE (TOP VIEW)



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Function Tables

A-TO-B STORAGE (OE = L, DIR = H)

INPUTS			OUTPUTS		
SEL	CLK	Α	1B	2B	
Н	Х	Х	1B ₀ † L‡	2B ₀ †	
L	\uparrow	L	L‡	X	
L	\uparrow	Н	н‡	Χ	

[†]Output level before the indicated steady-state input conditions are established

B-TO-A STORAGE (OE = L, DIR = L)

	INPUTS			
CLK	SEL	1B	2B	Α
1	Н	Х	L	L§
1	Н	X	Н	н§
1	L	L	Χ	L
↑	L	Н	Χ	Н

[§] Two clock edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

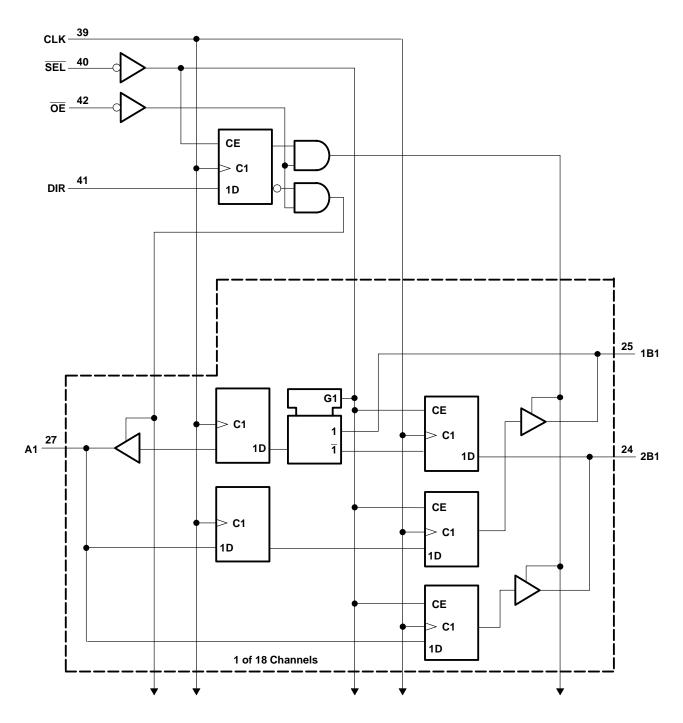
OUTPUT ENABLE

	INPUTS	OUTPUTS			
CLK	OE	DIR	Α	1B, 2B	
1	Н	Х	Z	Z	
1	L	L	Z	Active	
1	L	Н	Active	Z	



[‡]Two CLK edges are needed to propagate the data.

logic diagram (positive logic)



SN74ALVCHR162282 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3).	0.84 W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
	H High-level input voltage V V V V V V V V V	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage	·	0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
1	IPak lasak satast samat	V _{CC} = 2.3 V		-6	A	
IOH	nigh-level output current	V _{CC} = 2.7 V		-8	mA	
	Supply voltage 1.65 3.1 High-level input voltage VCC = 1.65 V to 1.95 V 0.65 × V _{CC} Low-level input voltage VCC = 1.65 V to 1.95 V 0.35 × V Low-level input voltage VCC = 2.3 V to 2.7 V 0.35 × V Input voltage 0 VCC Output voltage VCC = 1.65 V	-12				
		V _{CC} = 1.65 V		2		
1	Law level output ourrent	V _{CC} = 2.3 V		6	Λ	
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	Vcc	MIN	TYP†	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2			
		I _{OH} = -4 mA		2.3 V	1.9			
Vон		I _{OH} = -6 mA		2.3 V	1.7			V
		IOH = -0 IIIA		3 V	2.4			
		I _{OH} = -8 mA		2.7 V	2			
		I _{OH} = -12 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		$I_{OL} = 2 \text{ mA}$		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.4	
VOL		I _{OL} = 6 mA		2.3 V			0.55	V
		IOL = 0 IIIA		3 V			0.55	
		I _{OL} = 8 mA		2.7 V			0.6	
		$I_{OL} = 12 \text{ mA}$		3 V			0.8	
Ц		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.05 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _{I(hold)}		V _I = 1.7 V		2.5 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V]	-75			
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at $V_{\hbox{\footnotesize CC}}$ or GND	3 V to 3.6 V			750	μΑ
C _i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V				pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V				pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]S$ For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCHR162282 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency										MHz
t _W	Pulse duration, CLK h	igh or low									ns
	Setup time	A data before CLK↑									
l.		B data before CLK↑									ns
t _{su}		DIR before CLK↑									
		SEL before CLK↑									
		A data after CLK↑									
	Hald the e	B data after CLK↑									
^t h	<u> </u>	DIR after CLK↑									ns
		SEL after CLK↑									

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM	FROM TO (OUTPUT)	V _{CC} =	V _{CC} = 1.8 V V _{CC} = ± 0		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}											MHz
+ .	CLK	Α									ns
^t pd	CLK	В									115
4	ŌĒ	А									no
^t en	ŌĒ	В									ns
^t dis	ŌĒ	А									no
	ŌĒ	В									ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER			ONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled Outputs disabled	C _L = 0,	f = 10 MHz				pF

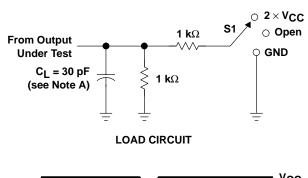


VCC

0 V

V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

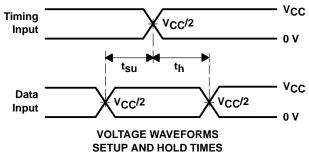


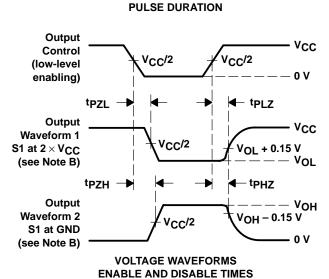
TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

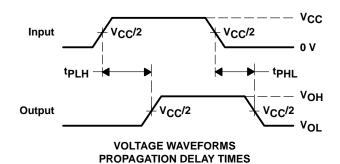
V_{CC}/2

VOLTAGE WAVEFORMS

Input



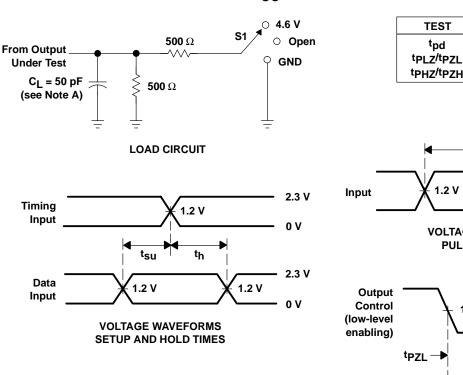




NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpz and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms





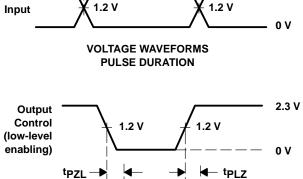
S1

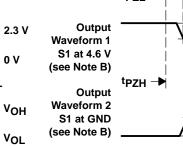
Open

4.6 V

2.3 V

2.3 V





V_{OL} + 0.3 V v_{OL} ^tPHZ V_{OH} - 0.3 V 0 V **VOLTAGE WAVEFORMS**

ENABLE AND DISABLE TIMES

NOTES: A. C_I includes probe and jig capacitance.

1.2 V

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time with one transition per measurement.

1.2 V

0 V

VOH

VOL

^tPHL

E. tpLz and tpHz are the same as tdis.

1.2 V

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



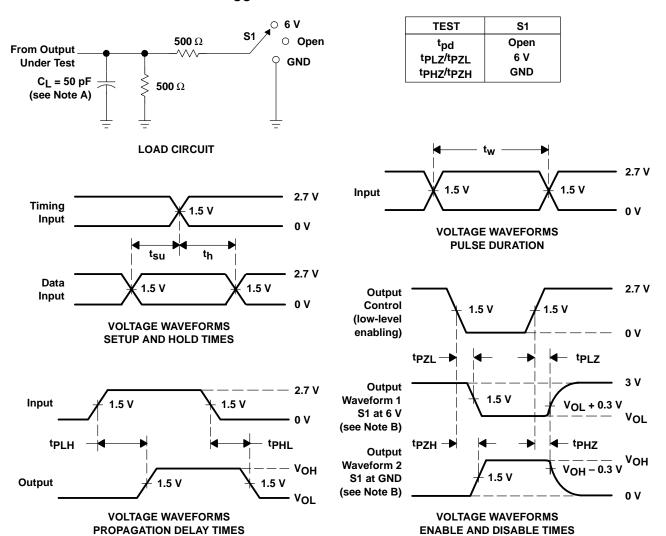
PRODUCT PREVIEW

Input

Output

^tPLH

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpZL and tpZH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

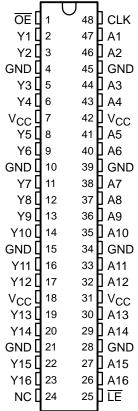
- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Ideal for Use in PC100 Register DIMM
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

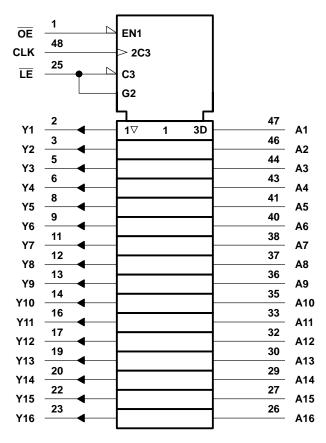
The SN74ALVC162334 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	UTS		OUTPUT
OE	LE	Υ		
Н	Х	Х	Χ	Z
L	L	Χ	L	L
L	L	X	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

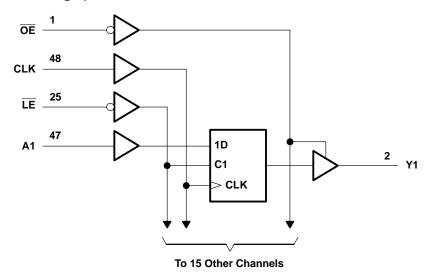
logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		. -0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

SN74ALVC162334 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
lau	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-6	mA
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low-level output current	V _{CC} = 2.3 V		6	mA
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		8	IIIA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2		
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
VOH	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
∨он		lour 6 mA	2.3 V	1.7			V
		IOH = -6 mA	3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		$I_{OH} = -12 \text{ mA}$	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		$I_{OL} = 2 \text{ mA}$	1.65 V			0.45	
Vol	I _{OL} = 4 mA	2.3 V			0.4		
VOL		I _{OL} = 6 mA	2.3 V			0.55	V
		IOL = 0 IIIA	3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
Ц		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	Vi – Voc or CND	221/		5		n.E
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5.5		pF
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	Pulse duration LE low			‡		3.3		3.3		3.3		20
t _W				‡		3.3		3.3		3.3		ns
		Data before CLK↑		‡		1.4		1.7		1.5		
t _{su}	Setup time	Data hafana IEA	CLK high	‡		1.2		1.6		1.3		ns
		Data before LE ↑	CLK low	‡		1.4		1.5		1.2		
	Hold time	Data after CLK↑		‡		0.9		0.9		0.9		
th		Data after LE ↑	CLK high or low	‡		1.1		1.1		1.1		ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1) (OO	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	4.4		4.5	1.1	3.9	
^t pd	LE	Y		†	1	5.8		6	1.3	5	ns
·	CLK			†	1	5.2		5.4	1	4.9	
t _{en}	ŌĒ	Υ		†	1	6.4		6.4	1.1	5.4	ns
t _{dis}	ŌĒ	Y		†	1	4.7		5.1	1.7	5	ns

[†]This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		UNIT
	(INFOT)	(001F01)	MIN	MAX	
	A	Y	1.2	3.8	no
^t pd	CLK	Υ	1.1	4.8	ns

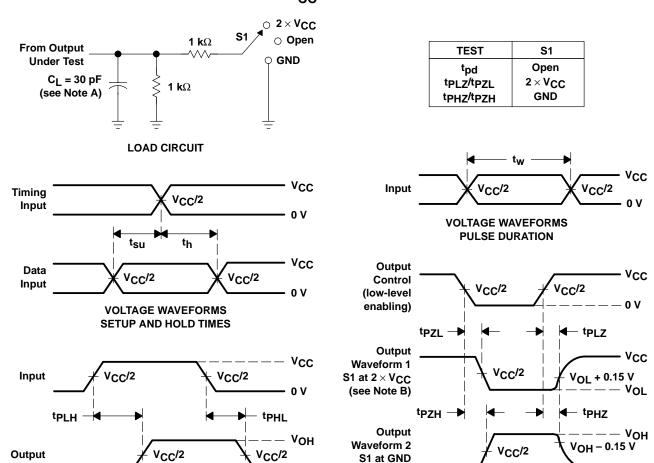
operating characteristics, $T_A = 25^{\circ}C$

Ī		PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
		PARAMETER		1E31 CONDITIONS	TYP	TYP	TYP	CINIT	
ſ	<u> </u>	Power dissipation	Outputs enabled	C ₁ = 0. f = 10 MHz	†	31	36	ρF	
	Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	7	11	ρг	

[†] This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

 v_{OL}

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

(see Note B)

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

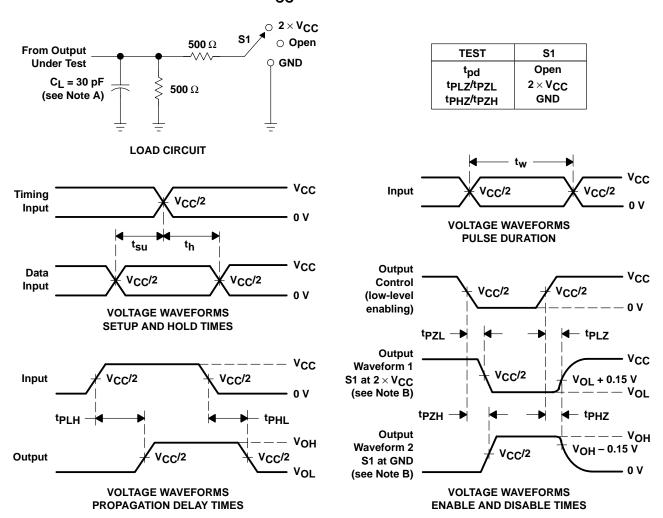
Figure 1. Load Circuit and Voltage Waveforms

- 0 V

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



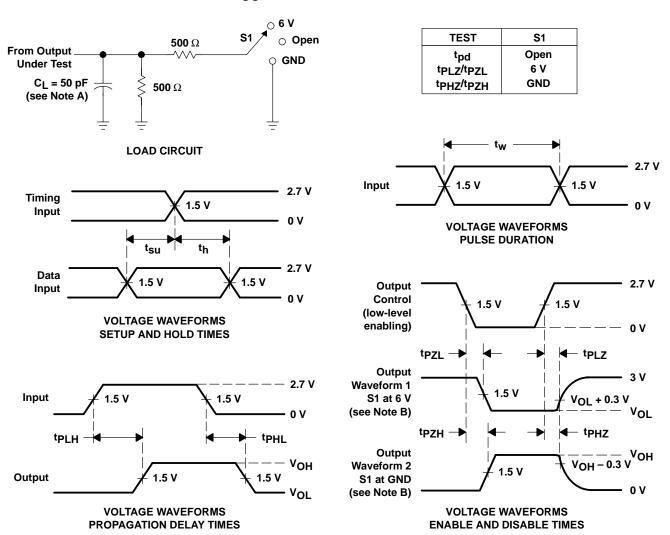
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq 2 \ ns$, $t_f \leq 2 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Port Has Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **Designed to Comply With JEDEC 168-Pin** and 200-Pin SDRAM Buffered DIMM Specification
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE})

(TOP VIEW) 48 CLK <u>oe</u> [47 A1 Y1 🛮 2 46 A2 Y2 | 3 GND 4 45 GND Y3 🛮 5 44 A3 Y4 🛮 6 43 🛮 A4 V_{CC} [] 7 42 V_{CC} 41 🛮 A5 Y5 | 8 Y6 🛮 9 40 A6 **GND** 10 39 GND 38 🛮 A7 Y7 🛚 11 37 A8 Y8 🛮 12 36 🛮 A9 Y9 ∐ 13 35 A10 Y10 🛭 14 GND 15 34 GND Y11 1 16 33 A11 Y12 [] 17 32 A12 V_{CC} **↓** 18 31 V_{CC} Y13 🛮 19 30 🛮 A13 29 A14 Y14 20 GND 21 28 GND Y15 🛮 22 27 🛮 A15 26 🛮 A16 Y16 23 NC 24 25 🛮 LE

DGG, DGV, OR DL PACKAGE

NC - No internal connection

input is low. When $\overline{\mathsf{LE}}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{\mathsf{LE}}$ is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{\mathsf{OE}}$ is high, the outputs are in the high-impedance state.

The output port includes equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

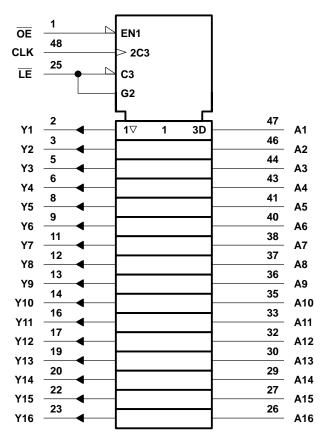
The SN74ALVCH162334 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS						
OE	LE	CLK	Α	Υ			
Н	Х	Х	Χ	Z			
L	L	Χ	L	L			
L	L	X	Н	Н			
L	Н	\uparrow	L	L			
L	Н	\uparrow	Н	Н			
L	Н	L or H	Χ	Y ₀ †			

[†] Output level before the indicated steady-state input conditions were established

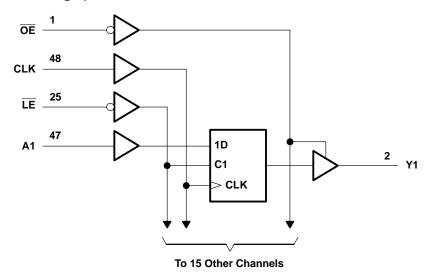
logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
	V _{IL} Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
1	High-level output current	V _{CC} = 2.3 V		-6	A	
ЮН		V _{CC} = 2.7 V		-8	mA	
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Lour lovel output outront	V _{CC} = 2.3 V		6	A	
IOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12	1	
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT	
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.	.2			
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		I _{OH} = -4 mA	2.3 V	1.9				
Vон		Jan. 6 mA	2.3 V	1.7			V	
		IOH = -6 mA	3 V	2.4				
		I _{OH} = -8 mA	2.7 V	2				
		I _{OH} = -12 mA	3 V	2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		I _{OL} = 2 mA	1.65 V			0.45		
		I _{OL} = 4 mA	2.3 V			0.4		
VOL		1- C A	2.3 V			0.55	V	
		IOL = 6 mA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6		
		$I_{OL} = 12 \text{ mA}$	3 V			8.0		
lį		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V	2.3 V	45				
I _I (hold)		V _I = 1.7 V	2.3 V	-45			μΑ	
		V _I = 0.8 V	3 V	75				
		V _I = 2 V	3 V	-75				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500		
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
∆lcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or G	ND 3 V to 3.6 V			750	μΑ	
C.	Control inputs	VI = VCC or GND	3.3 V		5.5		pF	
C _i Data inputs			3.5 V	6		<u> </u>		
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency				†		150		150		150	MHz	
	Pulse duration	LE low		†		3.3		3.3		3.3		ns	
t _W	Puise duration	CLK high or low		†		3.3		3.3		3.3		115	
		Data before CLK↑		†		1.4		1.7		1.5			
t _{su}	Setup time	tup time Data before LE↑	CLK high	†		1.2		1.6		1.3		ns	
			CLK low	†		1.4		1.5		1.2			
		Data after CLK↑		†		0.9		0.8		0.9			
th	t _h Hold time	Hold time	Hold time Data after <u>LE</u> ↑	CLK high or low	†		1.2		1.1		1.1		ns

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	3.9		4.5	1.1	3.9	
t _{pd}	LE	Y		†	1	5		6	1.3	5	ns
·	CLK			†	1	4.9		5.4	1	4.9	
t _{en}	ŌĒ	Y		†	1	5.4		6.4	1.1	5.4	ns
^t dis	ŌĒ	Y		†	1	5		5.1	1.7	5	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

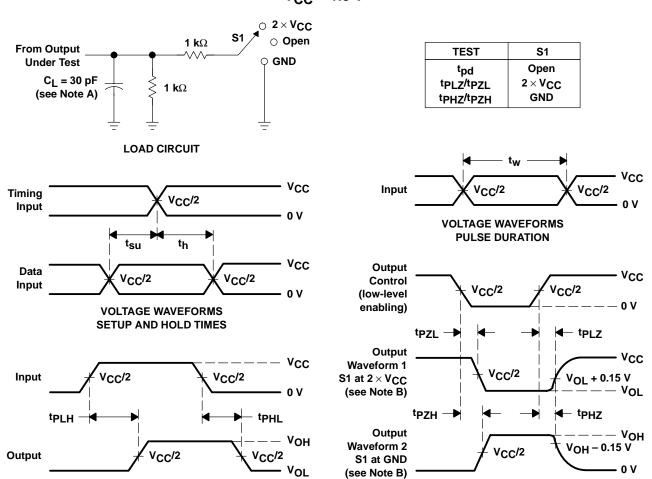
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
			TEST CONDITIONS	TYP	TYP	TYP		
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 0, f = 10 MHz	†	32	37	PF	
^C pd capad	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	7	11.5	pr	

[†] This information was not available at the time of publication.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.

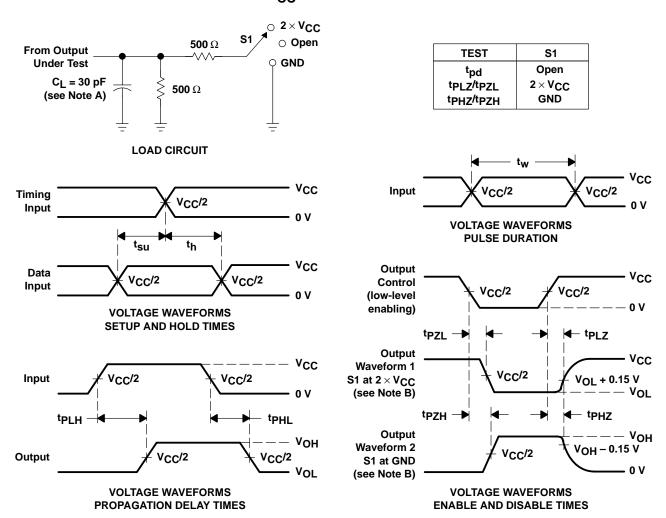
VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



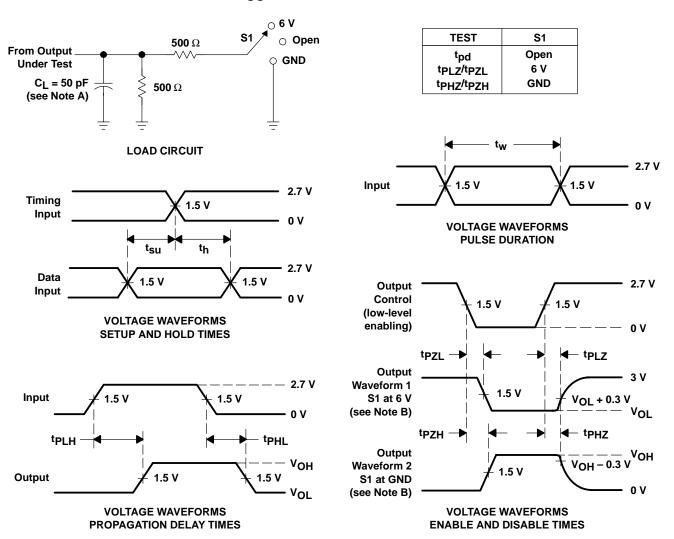
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DGG), Thin Shrink Small-Outline (DL), and Thin Very Small-Outline (DGV) Packages

description

This 1-bit to 4-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162344 is used in applications in which four separate memory locations must be addressed by a single address.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162344 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

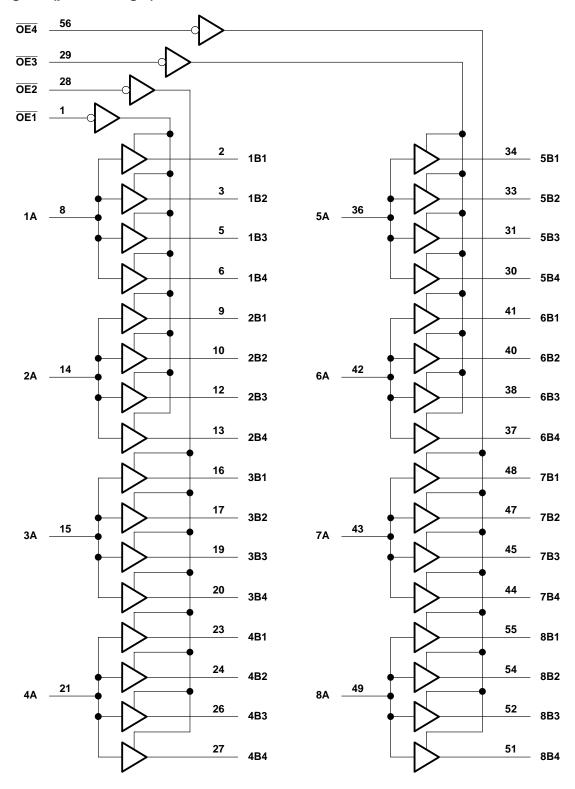
	_		_	1
OE1	1	\cup	56	OE4
1B1 [2		55	8B1
1B2 [54	8B2
GND [4		53	GND
1B3 [5		52] 8B3
1B4 [6		51] 8B4
V _{CC} [7		50]v _{cc}
1A [8		49]8A
2B1	9		48	7B1
2B2				7B2
GND [11			GND
2B3	12		45] 7B3
2B4	13		44	
2A [1		43]7A
3A [15]6A
3B1 [16] 6B1
3B2 [6B2
GND [18			GND
3B3 [19			B3
3B4 [20		37	
4A [1		36]5A
V _{CC}	22		35	- 00
4B1	23			5B1
4B2 L	24] 5B2
GND [25] GND
4B3 [26		31] 5B3
4B4	27		30	E
OE2	28		29	OE3

A-TO-B FUNCTION TABLE

	INP	JTS	OUTPUT
	OE	Α	Bn
Γ	L	Н	Н
	L	L	L
	Н	Χ	Z

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logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package .	
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
ViH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
VI	Input voltage		0	VCC	V	
۷o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
	High lovel output ourrent	V _{CC} = 2.3 V		-6	m ^	
ЮН	nign-iever output current	V _{CC} = 2.7 V		-8	mA	
	V _I Input voltage	V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Low lovel output ourrent	V _{CC} = 2.3 V		6	A	
IOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDIT	IONS	VCC	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		I _{OH} = -2 mA		1.65 V	1.2				
		I _{OH} = -4 mA		2.3 V	1.9			ı	
Vон		Lav. 6 mA		2.3 V	1.7			V	
		$I_{OH} = -6 \text{ mA}$		3 V	2.4			ļ	
		$I_{OH} = -8 \text{ mA}$	2.7 V	2					
		I _{OH} = -12 mA	3 V	2					
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 2 mA		1.65 V			0.45		
		I _{OL} = 4 mA		2.3 V			0.4	ı	
VOL		La. 6 m A		2.3 V			0.55	V	
		IOL = 6 mA		3 V			0.55		
		I _{OL} = 8 mA		2.7 V			0.6	ļ	
		I _{OL} = 12 mA	3 V			0.8	ļ		
lį		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		V _I = 0.7 V		2.3 V	45				
I _I (hold)		V _I = 1.7 V		2.3 V	-45			μΑ	
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	- 75			ļ	
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$ 3.6 V			±500	1				
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O =$	0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V, Othe	r inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	4		221/	2.5		n.E		
Ci	Data inputs	$V_I = V_{CC}$ or GND		3.3 V	3.5			pF	
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		4		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V} $ $V_{CC} = 2.7 \text{ V}$		V _{CC} = 2.7 V		V _{CC} =	3.3 V 3 V	UNIT
	(IIVFOT)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	А	В	§	1	4.9		5.1	1.4	4.4	ns
^t en	ŌĒ	В	§	1	6.4		6.6	1.2	5.7	ns
^t dis	ŌĒ	В	§	1	5.4		4.7	1.2	4.5	ns
t _{sk(o)} ¶									0.35	ns
^t sk(o) [#]									0.5	ns

[§] This information was not available at the time of publication.

[#] Skew between outputs of all banks of same package (A1–A8 tied together).



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

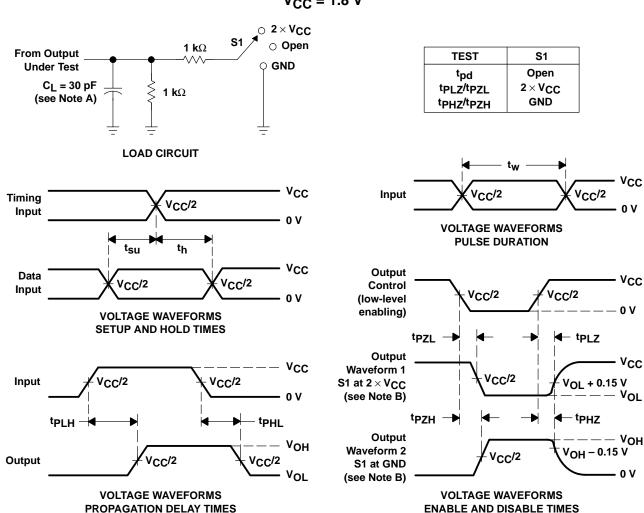
 $[\]P$ Skew between outputs of the same bank and same package (same transition).

operating characteristics, T_A = 25°C

	PARAMETER		TER TEST CONDITIONS			V _{CC} = 3.3 V	UNIT	
			TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	Power dissipation	Outputs enabled	C: -0 f - 10 MHz	†	68	82	pF	
Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	12	14	рг	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

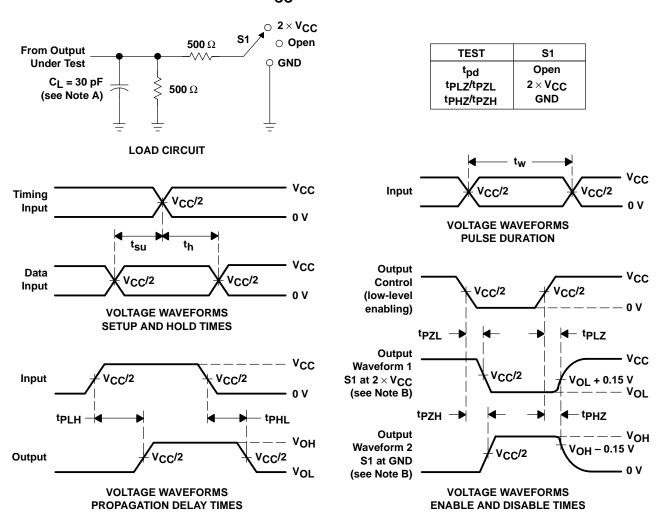


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

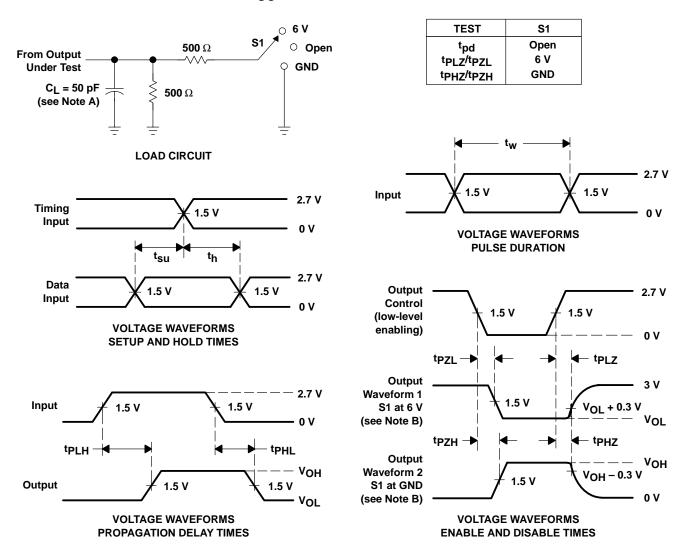


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



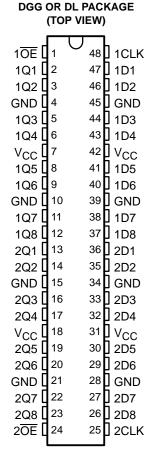
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- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.



The output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

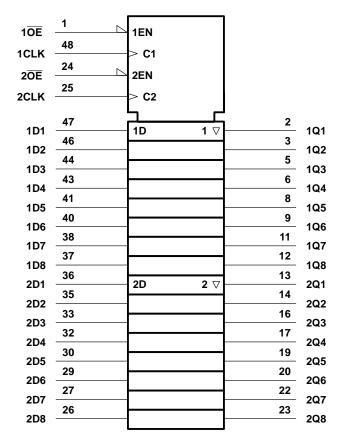
The SN74ALVCH162374 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

FUNCTION TABLE (each flip-flop)

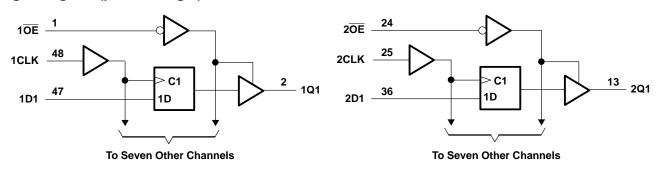
	INPUTS	ОИТРИТ			
OE	CLK	D	Q		
L	1	Н	Н		
L	\uparrow	L	L		
L	H or L	Χ	Q_0		
Н	X	Χ	Z		

logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	٧	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
	High lavel autout august	V _{CC} = 1.65 V		-2		
lou		V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8	MA	
	V _I Input voltage V _O Output voltage IOH High-level output current IOL Low-level output current Δt/Δv Input transition rise or fall rate	V _{CC} = 3 V		-12		
		$V_{CC} = 1.65 \text{ V}$		2		
lou	Low lovel output current	V _{CC} = 2.3 V		6	mΛ	
IOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -2 mA		1.65 V	1.2			
		I _{OH} = -4 mA		2.3 V	1.9			
Vон		1 6 mA		2.3 V	1.7			V
		IOH = -6 mA		3 V	2.4			
		I _{OH} = -8 mA		2.7 V	2			
		I _{OH} = -12 mA	3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.4	
VOL		1 C A		2.3 V			0.55	V
		I _{OL} = 6 mA		3 V		-	0.55	
		I _{OL} = 8 mA	I _{OL} = 8 mA				0.6	
		I _{OL} = 12 mA	3 V			0.8		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
·		V _I = 0.7 V		2.3 V	45			
I _I (hold)		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs			221/		3		n.E
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V	6		pF	
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \pm 0.2 \text{ V}$		2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		2.1		2.2		1.9		ns
th	Hold time, data after CLK↑	§		0.6		0.5		0.5		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	5.4		5.4	1	4.6	ns
t _{en}	ŌĒ	Q		†	1	6.5		6.4	1	5.2	ns
^t dis	ŌĒ	Q		†	1	5.6		5	1.2	4.5	ns

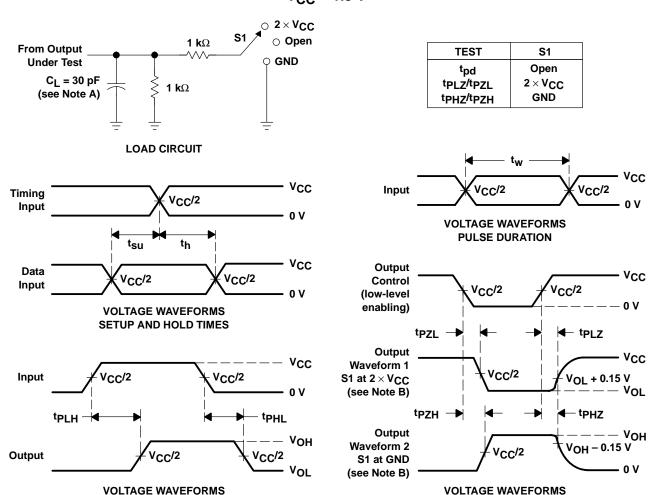
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	TANAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONT	
<u> </u>	Power dissipation	Outputs enabled	Cı = 0. f = 10 MHz	†	28	31	pF	
Cpd	capacitance	Outputs disabled	$C_L = 0, \qquad f = 10 \text{ MHz}$	†	10	11	рг	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

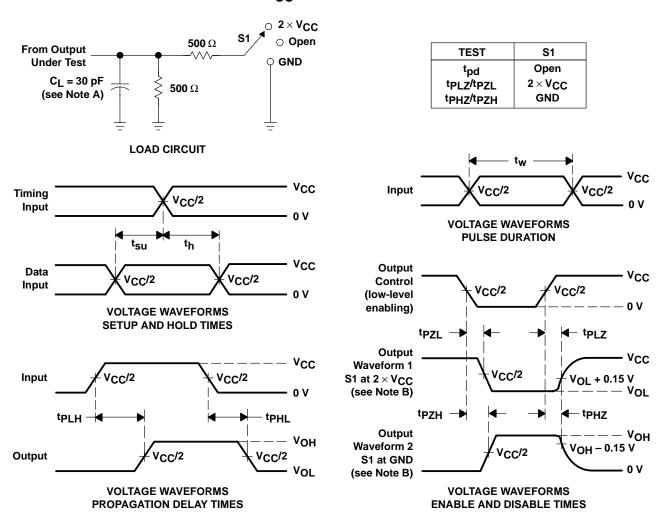
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



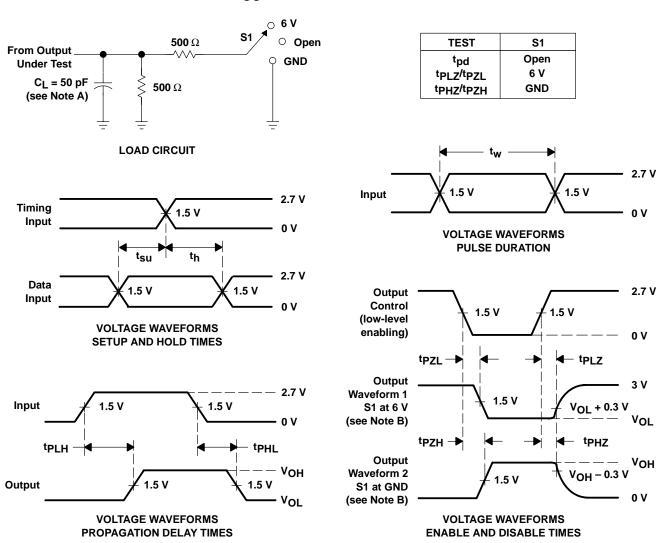
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DGG OR DL PACKAGE

(TOP VIEW)

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Member of the Texas Instruments Widebus+™ Family

- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω
 Series Resistors, So No External Resistors
 Are Required
- UBE™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

PRE 56 CLK SEL0 2 55 SELEN 1A1 **1**3 54**∏** 1B1 GND 4 53 GND 1A2 🛮 5 52**∏** 1B2 51 1B3 1A3 🛮 6 50 [] V_{CC} V_{CC} 47 1A4 🛮 8 49 🛮 1B4 1A5 🛮 9 48 1 1B5 47 1 1B6 1A6 10 11 GND 46 ∏ GND 1A7 | 12 45 1B7 1A8 🛮 44 🛮 1B8 13 43 1B9 1A9 14 2A1 15 42 **∏** 2B1 2A2 🛮 16 41 **∏** 2B2 2A3 [17 40 **∏** 2B3 GND [39 | GND 18 2A4 [] 19 38 **1** 2B4 2A5 Π 20 37**∏** 2B5 36**∏** 2B6 2A6 21 V_{CC} **□** 22 35 🛮 V_{CC} 2A7 23 34 2B7 2A8 Π 24 33 **∏** 2B8 GND ∏25 32 **∏** GND 2A9 Π 26 31 **1** 2B9 SEL1 27 30 SEL4 SEL2 28 29 **∏** SEL3

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

When preset (PRE) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both PRE and SELEN must be low and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down, \overline{PRE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162409 is characterized for operation from –40°C to 85°C.

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Function Tables

I	NPUTS	OUTPUT			
CLK	SEND PORT	RECEIVE PORT			
Х	X	_{В0} †			
Х	L	L			
Х	Н	Н			
1	L	L			
1	Н	Н			
Н	X	в ₀ †			
L	Χ	_{B0} †			

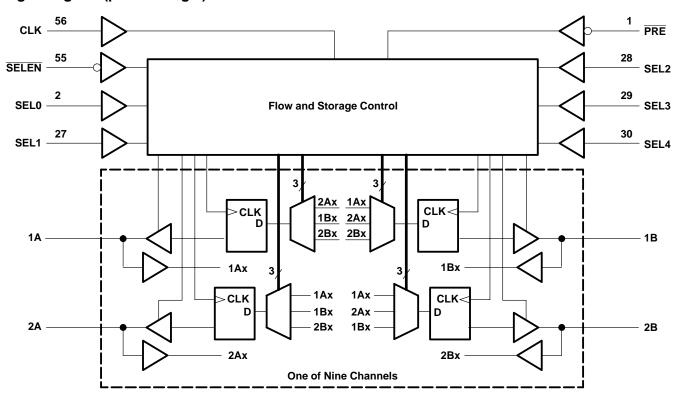
[†] Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

			INPL	JTS				
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
Н	Х	Х	Х	Х	Х	Х	Х	All outputs disabled
L	Н	\uparrow	X	X	X	X	Х	No change
L	L	1	0	0	0	0	0	None, all I/Os off
L	L	\uparrow	0	0	0	0	1	Not used
L	L	1	0	0	0	1	0	Not used
L	L	1	0	0	0	1	1	Not used
L	L	1	0	0	1	0	0	Not used
L	L	\uparrow	0	0	1	0	1	Not used
L	L	1	0	0	1	1	0	Not used
L	L	\uparrow	0	0	1	1	1	Not used
L	L	1	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	\uparrow	0	1	0	0	1	2A to 1A
L	L	1	0	1	0	1	0	2B to 1B
L	L	\uparrow	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	\uparrow	0	1	1	0	1	1A to 2A
L	L	1	0	1	1	1	0	1B to 2B
L	L	\uparrow	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	\uparrow	1	0	0	0	1	1A to 1B
L	L	1	1	0	0	1	0	2A to 2B
L	L	\uparrow	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	\uparrow	1	0	1	0	1	1B to 1A
L	L	1	1	0	1	1	0	2B to 2A
L	L	\uparrow	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	\uparrow	1	1	0	0	1	1B to 2A
L	L	1	1	1	0	1	0	2B to 1A
L	L	\uparrow	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	1	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	\uparrow	1	1	1	0	1	1A to 2B
L	L	1	1	1	1	1	0	2A to 1B
L	L	1	1	1	1	1	1	1A to 2B and 2A to 1B



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	
Storage temperature range, T _{stq}	—65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		V _{CC} = 2.7 V to 3.6 V	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		V _{CC} = 2.7 V to 3.6 V		0.8		
VI	Input voltage	•	0	Vcc	V	
۷o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-4		
	High lavel autout august (A a sut)	V _{CC} = 2.3 V		-12	ı	
	High-level output current (A port)	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24	mA	
ІОН		V _{CC} = 1.65 V		-2		
	High-level output current (B port)	V _{CC} = 2.3 V		-6		
		V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		4		
	Laureland autout aurorat (Amari)	V _{CC} = 2.3 V		12		
	Low-level output current (A port)	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
lOL		V _{CC} = 1.65 V		2		
	Law law law to when the company (D. marth)	V _{CC} = 2.3 V		6		
	Low-level output current (B port)	V _{CC} = 2.7 V		8		
	V _{CC} = 3 V			12		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT	
		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	V _{CC} -0.2	<u>)</u>			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
		I _{OH} = -6 mA	2.3 V	2				
	A port		2.3 V	1.7				
		I _{OH} = -12 mA	2.7 V	2.2				
			3 V	2.4				
1/		I _{OH} = -24 mA	3 V	2			V	
VOH		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	V _{CC} -0.2)		V	
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
	B port	la 6 mA	2.3 V	1.7				
		IOH = -6 mA	3 V	2.4				
		$I_{OH} = -8 \text{ mA}$	2.7 V	2				
	I _{OH} = -12 mA	3 V	2					
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA	1.65 V			0.45		
	A nort	I _{OL} = 6 mA	2.3 V			0.4		
	A port	Ja. 12 mA	2.3 V			0.7		
		I _{OL} = 12 mA	2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55		
VOL		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V	
		I _{OL} = 2 mA	1.65 V			0.45		
		I _{OL} = 4 mA	2.3 V			0.4		
	B port	lou - 6 mA	2.3 V			0.55		
		I _{OL} = 6 mA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6		
		I _{OL} = 12 mA	3 V			0.8		
Ц		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.05 V	-25				
		$V_{I} = 0.7 \text{ V}$	2.3 V	45				
I _{I(hold)}		V _I = 1.7 V	2.5 V	-45			μΑ	
		V _I = 0.8 V	3 V	75				
	V _I = 2 V		-75	· · ·				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500		
l _{OZ} §		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
∆lcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND	3.3 V				pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V				pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency										MHz	
t _W	Pulse duration, CLK high or low										ns	
		A or B before CLK↑										
١.	0:	SEL before CLK↑									ns	
t _{su}	Setup time	SELEN before CLK↑										
		PRE before CLK↑										
		A or B after CLK↑										
th	Hold time	SEL after CLK↑									ns	
		SELEN after CLK↑										

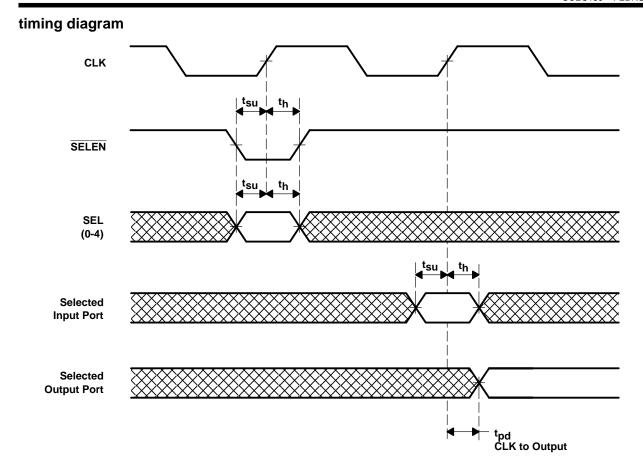
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT	
	(IIVFOT)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX		
f _{max}											MHz	
t _{pd}	CLK	A or B									ns	
t _{en}	CLK	A or B									ns	
^t dis	CLK	A or B									ns	
	PRE	AUB										

operating characteristics, $T_A = 25^{\circ}C$

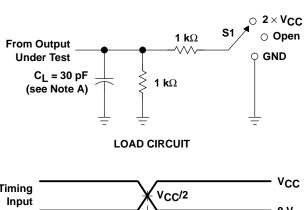
	PARAMET	ER	TEST CONDITIONS		V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V	UNIT
<u> </u>	Power dissipation	All outputs enabled	C 50 pE	f = 10 MHz				ρF
C _{pd}	capacitance	All outputs disabled	$C_L = 50 pF$,	1 = 10 WITZ				рг

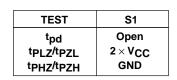






PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

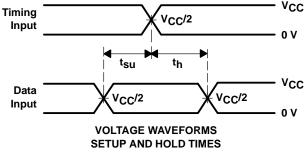


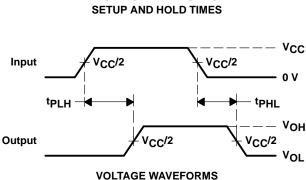


VCC

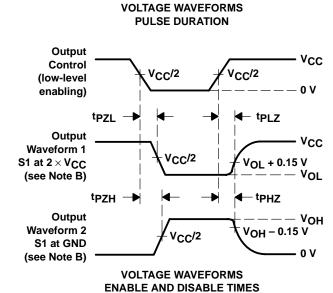
0 V

V_{CC}/2





PROPAGATION DELAY TIMES



V_{CC}/2

Input

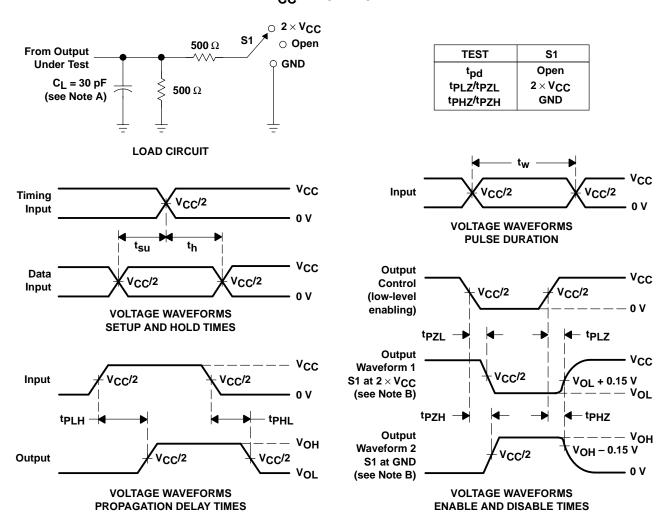
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



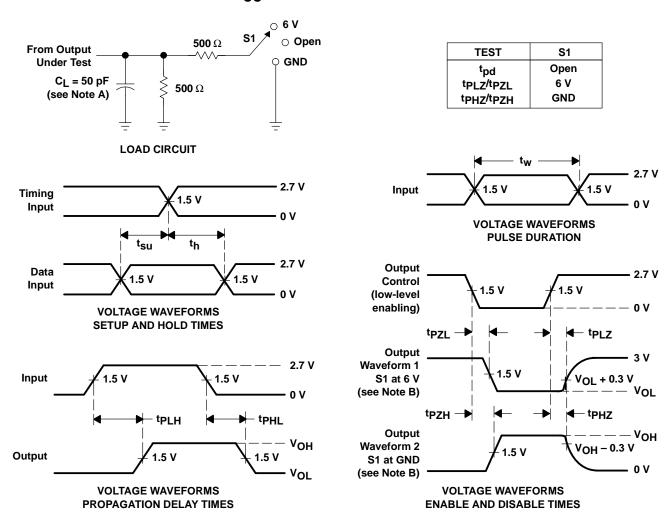
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2 ns. $t_{f} \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SCES056F - SEPTEMBER 1995 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus+™ Family
- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω
 Series Resistors, So No External Resistors
 Are Required
- UBE™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For order entry:

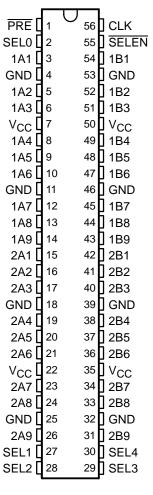
The DGG package is abbreviated to G.

description

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

DGG OR DL PACKAGE (TOP VIEW)



The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω series resistors to reduce overshoot and undershoot.

When preset (PRE) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both PRE and SELEN must be low and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down, \overline{PRE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162409 is characterized for operation from -40°C to 85°C.

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Function Tables

l	INPUTS	OUTPUT				
CLK	SEND PORT	RECEIVE PORT				
Х	X	В ₀ †				
Х	L	L				
Х	Н	Н				
\uparrow	L	L				
\uparrow	Н	Н				
Н	X	В ₀ †				
L	X	_{B0} †				

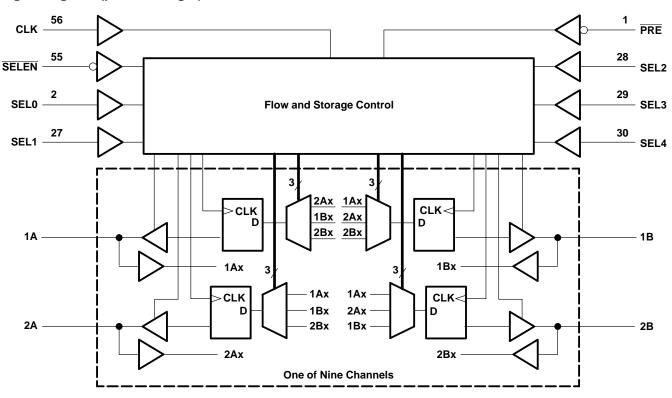
[†] Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

			INPL	ITS				
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
Н	Х	Χ	Х	Х	Х	Х	Х	All outputs disabled
L	Н	\uparrow	X	X	Х	X	Х	No change
L	L	1	0	0	0	0	0	None, all I/Os off
L	L	\uparrow	0	0	0	0	1	Not used
L	L	1	0	0	0	1	0	Not used
L	L	\uparrow	0	0	0	1	1	Not used
L	L	1	0	0	1	0	0	Not used
L	L	\uparrow	0	0	1	0	1	Not used
L	L	1	0	0	1	1	0	Not used
L	L	\uparrow	0	0	1	1	1	Not used
L	L	1	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	\uparrow	0	1	0	0	1	2A to 1A
L	L	1	0	1	0	1	0	2B to 1B
L	L	\uparrow	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	\uparrow	0	1	1	0	1	1A to 2A
L	L	1	0	1	1	1	0	1B to 2B
L	L	\uparrow	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	\uparrow	1	0	0	0	1	1A to 1B
L	L	1	1	0	0	1	0	2A to 2B
L	L	\uparrow	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	\uparrow	1	0	1	0	1	1B to 1A
L	L	1	1	0	1	1	0	2B to 2A
L	L	\uparrow	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	1	1	1	0	0	1	1B to 2A
L	L	1	1	1	0	1	0	2B to 1A
L	L	1	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	1	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	1	1	1	1	0	1	1A to 2B
L	L	1	1	1	1	1	0	2A to 1B
L	L	\uparrow	1	1	1	1	1	1A to 2B and 2A to 1B



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
1	High level output ourrent	V _{CC} = 2.3 V		-6	A	
ЮН	High-level output current	V _{CC} = 2.7 V		-8	mA	
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Law lavel output ourrent	V _{CC} = 2.3 V		6	A	
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT	
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2			
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
Voн	I _{OH} = -6 mA	2.3 V	1.7			V	
	10H = -0 IIIA	3 V	2.4				
	$I_{OH} = -8 \text{ mA}$	2.7 V	2				
	$I_{OH} = -12 \text{ mA}$	3 V	2				
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2		
	$I_{OL} = 2 \text{ mA}$	1.65 V			0.45		
	$I_{OL} = 4 \text{ mA}$	2.3 V			0.4		
V _{OL}	la. 6 mA	2.3 V			0.55	V	
	$I_{OL} = 6 \text{ mA}$	3 V			0.55		
	$I_{OL} = 8 \text{ mA}$	2.7 V			0.6		
	$I_{OL} = 12 \text{ mA}$	3 V			0.8		
Ц	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
	V _I = 0.58 V	1 GE V	25				
	V _I = 1.07 V	1.65 V	-25				
	$V_{I} = 0.7 V$	2.3 V	45				
II(hold)	V _I = 1.7 V	2.3 V	-45			μΑ	
	$V_{I} = 0.8 V$	3 V	75				
	V _I = 2 V	3 V	-75				
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500		
loz§	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
ΔlCC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ	
C _i Control inputs	V_{I} Control inputs $V_{I} = V_{CC}$ or GND			4		pF	
C _{io} A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	VCC =		VCC =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			†		120		120		120	MHz
t _W Pulse duration, CLK high or low		†		4.2		4.2		3		ns	
		A or B before CLK↑	†		1.9		1.9		1.4		
١.	0	SEL before CLK↑	†		5.1		4.2		3.5		ns
t _{su}	Setup time	SELEN before CLK↑	†		2.5		2.5		1.8		
		PRE before CLK↑	†		1		1		0.7		
		A or B after CLK↑	†		0.8		0.8		1		
th	Hold time	SEL after CLK↑	†		0		0		0		ns
		SELEN after CLK↑	†		0.5		0.5		0.8		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

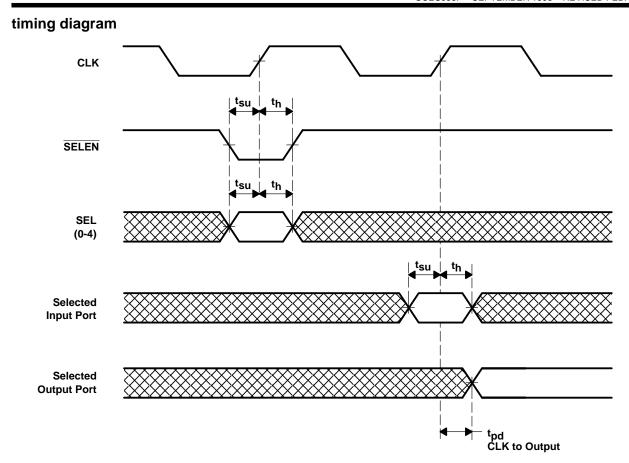
PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		(INPOT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	i
f _{max}				†		120		120		120		MHz
t _{pd}		CLK	A or B		†	1.5	6.9		7	1.5	6.2	ns
t _{en}		CLK	A or B		†	2.4	7.8		7.6	2	6.8	ns
^t dis	CLK	A or B		†	2.3	7.1		6.4	2	6.1	no	
	PRE	AUIB		†	2.8	7.7		7	2.5	6.4	ns	

[†] This information was not available at the time of publication.

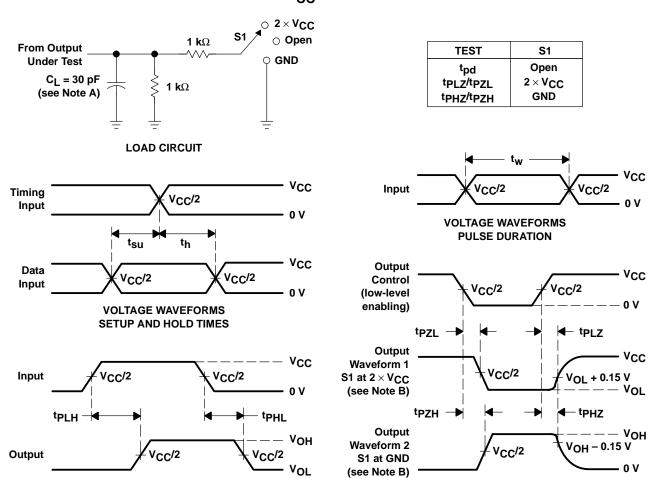
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
PARAMETER		TYP			TYP	TYP	ONIT	
<u> </u>	Power dissipation	sipation All outputs enabled		f = 10 MHz	†	60	60	PΓ
Cpd	capacitance	All outputs disabled	$C_L = 50 pF$,	1 = 10 NIM2	†	60	60	þΓ

[†] This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

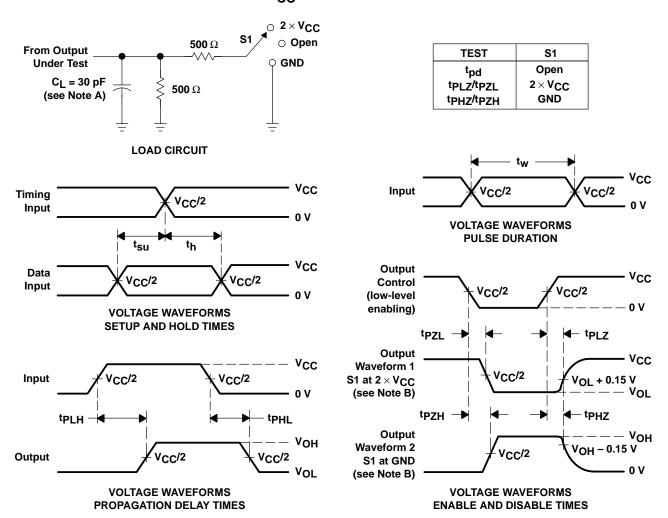
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



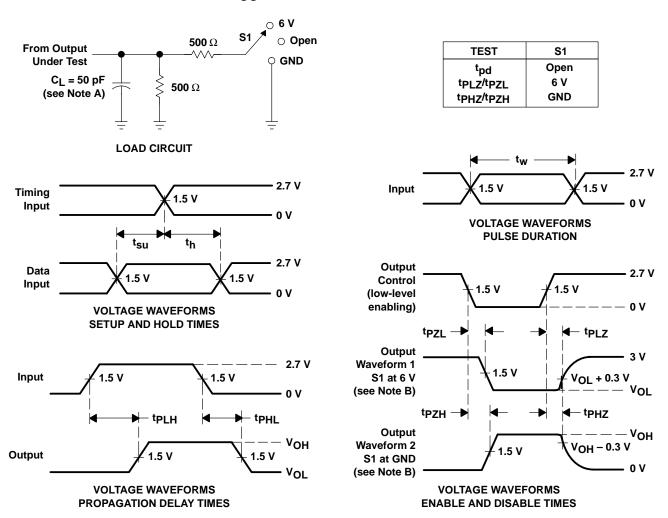
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Q} = 50 Ω , $t_{f} \leq$ 2 ns. $t_{f} \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



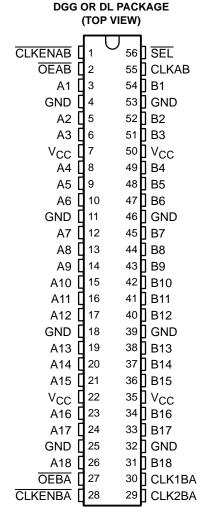
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- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω
 Series Resistors, So No External Resistors
 Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock-enable (CLKENAB and CLKENBA) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select (SEL) input.



Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162525 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

Function Tables

A-TO-B STORAGE (OEAB = L)

I	OUTPUT		
CLKENAB	CLKAB	Α	В
Н	Х	Х	в ₀ †
L	\uparrow	L	L
L	\uparrow	Н	Н

[†] Output level before the indicated steady-state input conditions were established

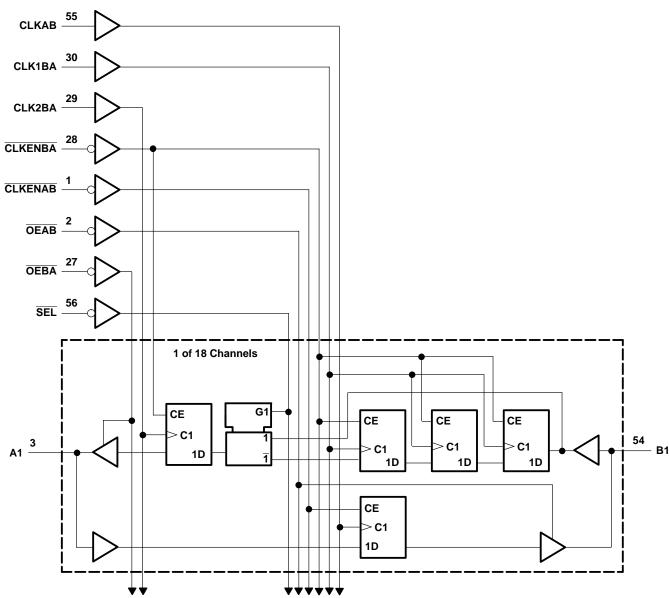
B-TO-A STORAGE (OEBA = L)

		-	-		
	OUTPUT				
CLKENBA	CLK2BA	CLK1BA	SEL	В	Α
Н	Х	Х	Х	Χ	A ₀ †
L	\uparrow	Χ	Н	L	L
L	\uparrow	Χ	Н	Н	Н
L	1	\uparrow	L	L	L‡
L	1	\uparrow	L	Н	H [‡]

[†] Output level before the indicated steady-state input conditions were established

[‡]Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

logic diagram (positive logic)



SN74ALVCH162525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH162525 **18-BIT REGISTERED BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCES058D - NOVEMBER 1995 - REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	High-level output current (A port)	V _{CC} = 2.3 V		-12		
	High-level output current (A port)	V _{CC} = 2.7 V		-12		
Іон		V _{CC} = 3 V		-24	mA	
		V _{CC} = 1.65 V		-2	IIIA	
	High-level output current (B port)	V _{CC} = 2.3 V		-6		
	High-level output current (B port)	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		4		
	Low-level output current (A port)	V _{CC} = 2.3 V		12		
	Low-level output current (A port)	V _{CC} = 2.7 V		12		
lai		V _C C = 3 V		24	mA	
lOL		V _{CC} = 1.65 V		2	IIIA	
	Low-level output current (B port)	V _{CC} = 2.3 V		6		
	Low-level output outlett (b port)	$V_{CC} = 2.7 \text{ V}$		8		
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN TYPT	MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2		
		I _{OH} = -4 mA	1.65 V	1.2		
		I _{OH} = -6 mA	2.3 V	2		
	A port		2.3 V	1.7		
		I _{OH} = -12 mA	2.7 V	2.2		
			3 V	2.4		
\		I _{OH} = -24 mA	3 V	2		\ /
VOH		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2		V
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2		
		I _{OH} = -4 mA	2.3 V	1.9		
	B port	0.00	2.3 V	1.7		
		IOH = -6 mA	3 V	2.4		
		I _{OH} = -8 mA	2.7 V	2		
		I _{OH} = -12 mA	3 V	2		
		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
		I _{OL} = 4 mA	1.65 V		0.45	
	1	I _{OL} = 6 mA	2.3 V		0.4	
	A port		2.3 V		0.7	
		I _{OL} = 12 mA	2.7 V		0.4	
		I _{OL} = 24 mA	3 V		0.55	
VOL		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	V
		I _{OL} = 2 mA	1.65 V		0.45	
		I _{OL} = 4 mA	2.3 V		0.4	
	B port		2.3 V		0.55	
		I _{OL} = 6 mA	3 V		0.55	
		I _{OL} = 8 mA	2.7 V		0.6	
		I _{OL} = 12 mA	3 V		0.8	
lį	•	V _I = V _{CC} or GND	3.6 V		±5	μΑ
		V _I = 0.58 V	4.05.1/	25		
		V _I = 1.07 V	1.65 V	-25		
		V _I = 0.7 V	221/	45		
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45		μΑ
, ,		V _I = 0.8 V	0.14	75		
		V _I = 2 V	3 V	-75		
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500	
loz§		$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ
∆lcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	3		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V	7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		VCC =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			†		120		125		150	MHz
t _W	Pulse duration, C	Pulse duration, CLK high or low			3.2		3.2		3		ns
		A data before CLKAB↑	†		1.3		1.3		1.3		
		B data before CLK2BA↑	†		2.1		1.8		1.7		
t _{su} Setup time	B data before CLK1BA↑	†		1.3		1.2		1.1			
	Setup time	SEL before CLK2BA↑	†		3.3		3.3		3.3		ns
		CLKENAB before CLKAB↑	†		2.1		1.9		1.6		
		CLKENBA before CLK1BA↑	†		2.7		2.5		2.1		
		CLKENBA before CLK2BA↑	†		2.7		2.5		2.2		
		A data after CLKAB↑	†		0.7		0.4		0.9		
		B data after CLK2BA↑	†		0.4		0		0.6		
		B data after CLK1BA↑	†		0.8		0.4		1		
t _h	Hold time	SEL after CLK2BA↑	†		0		0		0.1		ns
		CLKENAB after CLKAB↑	†		0.1		0.3		0.3		
		CLKENBA after CLK1BA↑	†		0		0		0.1		
		CLKENBA after CLK2BA↑	†		0		0		0		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(001701)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		125		150		MHz
4 .	CLKAB	В		†	1	5.5		5.4	1	4.7	no
^t pd	CLK2BA	А		†	1	4.5		4.4	1	4.2	ns
,	OEBA	А		†	1	6.1		6.1	1	5.1	
^t en	OEAB	В		†	1	6.7		6.8	1	5.7	ns
+	OEBA	А		†	1	6.3		5.4	1	4.9	no
^t dis	OEAB	В		†	1	6.3		5.4	1	4.9	ns

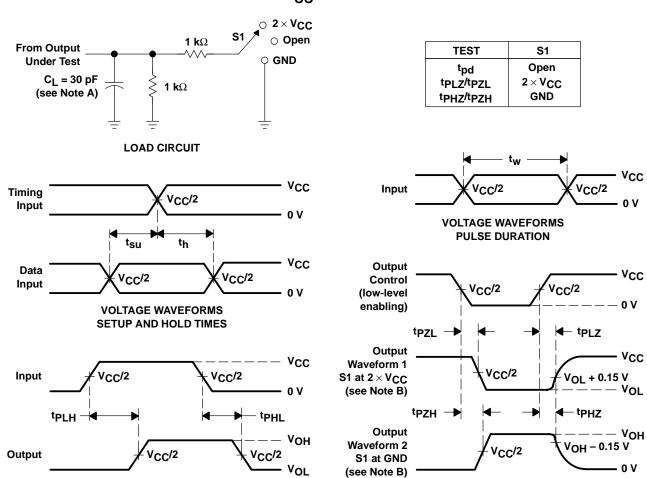
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONIT
	Power dissipation	Outputs enabled	C. FO. f. 10 MU.	†	160	160	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	160	160	рг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

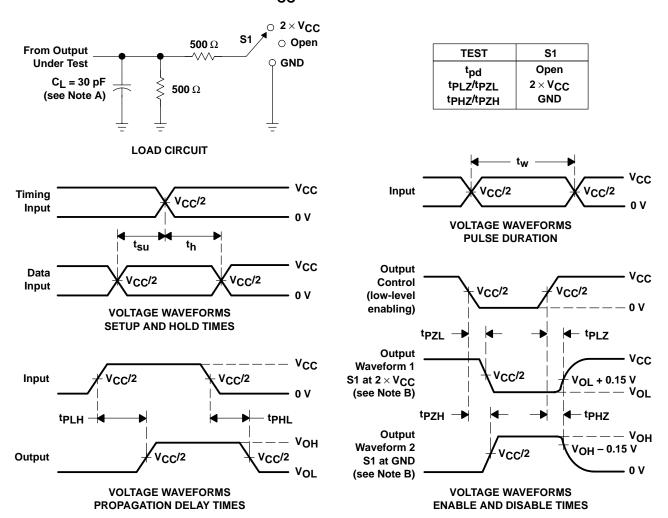
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



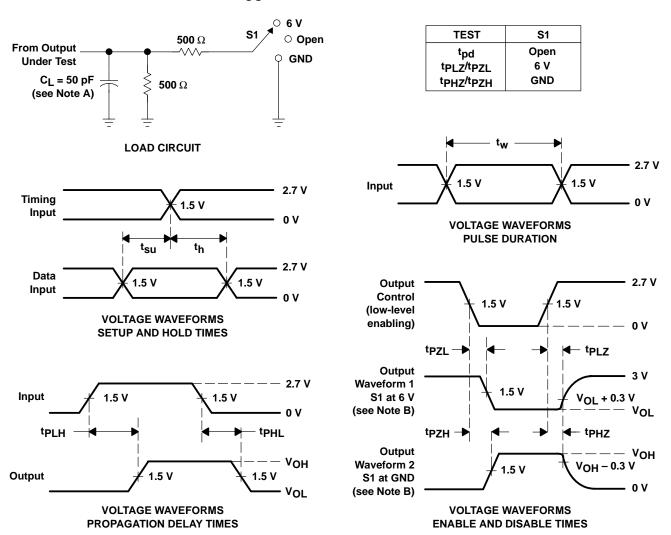
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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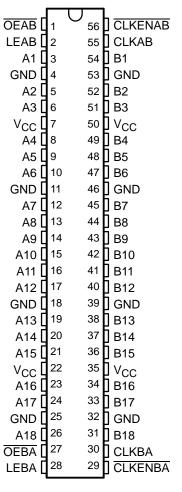
- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBT** ™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- **B-Port Outputs Have Equivalent 26-** Ω Series Resistors, So No External Resistors Are Required
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

DGG OR DL PACKAGE (TOP VIEW)



Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The B-port outputs include equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162601 is characterized for operation from -40°C to 85°C.

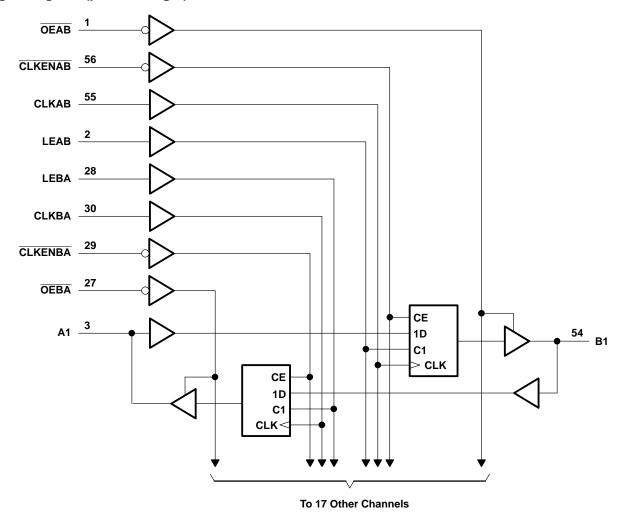
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FUNCTION TABLE†

	I	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Χ	Z
Х	L	Н	Χ	L	L
Х	L	Н	Χ	Н	Н
Н	L	L	X	Χ	в ₀ ‡
Н	L	L	X	Χ	в ₀ ‡ в ₀ ‡
L	L	L	\uparrow	L	L
L	L	L	\uparrow	Н	Н
L	L	L	L or H	Χ	в ₀ ‡

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
	High level output ourrent (A north)	V _{CC} = 2.3 V		-12		
	High-level output current (A port)	V _{CC} = 2.7 V		-12		
1		V _{CC} = 3 V		-24	mA	
ЮН		V _{CC} = 1.65 V		-2	mA	
	High level output outroot (P port)	V _{CC} = 2.3 V		-6		
	High-level output current (B port)	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		4		
	Low-level output current (A port)	V _{CC} = 2.3 V		12		
	Low-level output current (A port)	V _{CC} = 2.7 V		12		
la.		V _{CC} = 3 V		24	mA	
lOL		V _{CC} = 1.65 V		2	IIIA	
	Low-level output current (B port)	V _{CC} = 2.3 V		6		
	Low-level output current (b port)	V _{CC} = 2.7 V		8		
		VCC = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP† MA	x	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2		
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
	A port		2.3 V	1.7	-		
		I _{OH} = -12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
VOH		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2		V
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
	B port		2.3 V	1.7			
		IOH = -6 mA	3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V		C	.2	
		I _{OL} = 4 mA	1.65 V		0.4	45	
	. .	I _{OL} = 6 mA	2.3 V		C	.4	
	A port		2.3 V		C	.7	
		$I_{OL} = 12 \text{ mA}$	2.7 V		C	.4	
		I _{OL} = 24 mA	3 V		0.	55	
VOL		I _{OL} = 100 μA	1.65 V to 3.6 V		C	.2	V
		I _{OL} = 2 mA	1.65 V		0.4	45	
		I _{OL} = 4 mA	2.3 V		C	.4	
	B port		2.3 V		0.	55	
		I _{OL} = 6 mA	3 V		0.	55	
		I _{OL} = 8 mA	2.7 V		C	.6	
		I _{OL} = 12 mA	3 V		C	.8	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	4.05.1/	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	0.01/	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
,		V _I = 0.8 V	0.1/	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V [‡]	3.6 V		±5	00	
I _{OZ} §		$V_O = V_{CC}$ or GND	3.6 V		±	10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
∆lcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		7:	50	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		4		pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF
			-				

 $[\]S$ For I/O ports, the parameter IOZ includes the input leakage current.



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequenc	у			†		140		150		150	MHz
	Pulse	LE high		†		3.3		3.3		3.3		20
t _W	duration	CLK high or low		†		3.3		3.3		3.3		ns
	Catua tima	Data before CLK↑		†		2.3		2.4		2.1		
١.		Data before LE↓	CLK high	†		2		1.6		1.6		20
t _{su}	Setup time	Data before LEV	CLK low	†		1.3		1.2		1.1		ns
		CLKEN before CLK↑		†		2		2		1.7		
		Data after CLK↑		†		0.7		0.7		0.8		
4.	I lold time	Data after LE↓	CLK high	†		1.3		1.6		1.4		20
чh	t _h Hold time	Data after LE↓	CLK low	†		1.7		2		1.7		ns
		CLKEN after CLK↑		†		0.3		0.5		0.6		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFO1)	(OUTFUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		140		150		150		MHz
	А	В		†	1.3	4.8		5.2	1.6	4.5	
	В	А		†	1	4.3		4.6	1	4.1	
	LEAB	В		†	1	5.5		5.9	1.5	5.1	no
^t pd	LEBA	А		†	1	5		5.3	1	4.7	ns
	CLKAB	В		†	1.5	6.1		6.3	1.6	5.5	
	CLKBA	А		†	1.3	5.6		5.8	1.4	5	
t _{en}	OEAB	В		†	1.6	6.1		6.7	1.6	5.7	ns
^t dis	OEAB	В		†	1.8	5.7		5.3	1.8	4.8	ns
t _{en}	OEBA	А		†	1.1	5.5		6.1	1.1	5.2	ns
^t dis	OEBA	Α		†	1.3	5.2		4.8	1.6	4.4	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

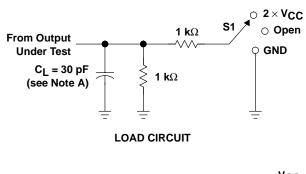
	PARAMETER		TEST CONDITIONS		V _{CC} = 2.5 V		UNIT
			IYP	TYP TYP TYP † 41 50			
<u> </u>	Power dissipation	Outputs enabled	C _I = 50 pF, f = 10 MHz	†	41	50	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	6	6	рг

[†] This information was not available at the time of publication.

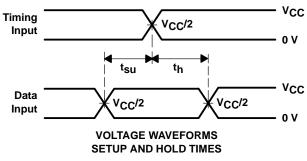
VCC

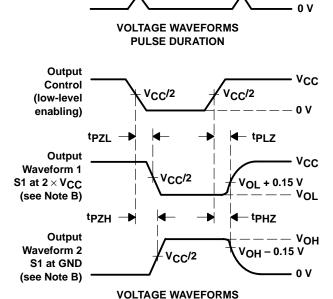
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



TEST	S 1
t _{pd}	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND

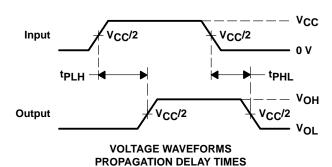




ENABLE AND DISABLE TIMES

V_{CC}/2

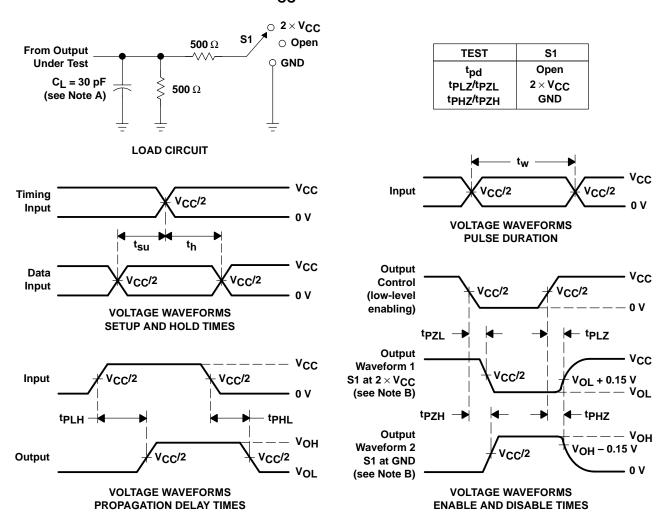
Input



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

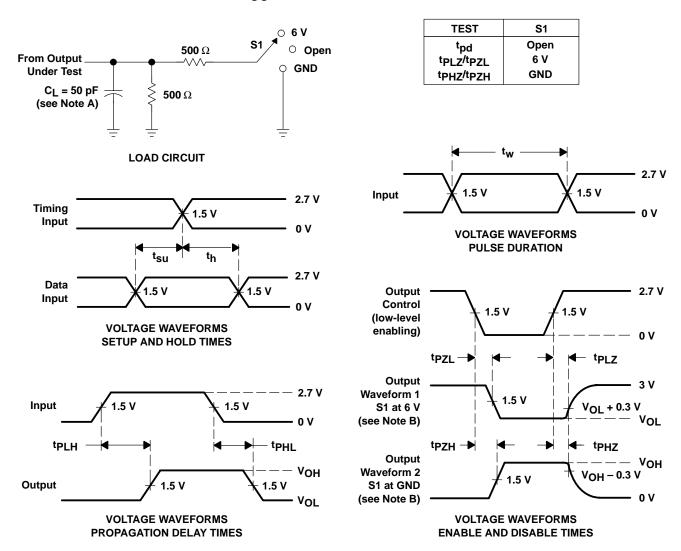
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **UBT**™ (Universal Bus Transceiver) **Combines D-Type Latches and D-Type** Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Thin** Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

NOTE: For order entry:

The DGG package is abbreviated to G, the DGV package is abbreviated to V, and the DL package is abbreviated to L.

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The outputs include equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

56 T CLKENAB OEAB LEAB 2 55 CLKAB 54 🛮 B1 A1 🛮 3 GND ∏4 53 **∏** GND 52 | B2 A2 🛮 5 АЗ П6 51 **N** B3 50 🛮 V_{CC} V_{CC} **∐** 7 A4 ∏8 49 **∏** B4 A5 [] 9 48 ∏ B5 A6 🛮 10 47 **∏** B6 GND [] 11 46 🛛 GND А7 🛭 45 **∏** B7 12 44 **∏** B8 A8 [] 13 A9 🛮 14 43 B9 15 42 **∏** B10 А10 П A11 16 41 **∏** B11 A12 🛮 17 40 **∏** B12 GND [18 39 **[**] GND A13 🛮 19 38 **П** В13 A14 🛮 20 37 **|** B14 A15 [] 21 36 N B15 V_{CC} **□** 22 35 🛮 V_{CC} A16 🛮 23 34 🛮 B16 A17 **□**24 33 **∏** B17 GND [] 25 32 | GND A18 [26 31 **|** B18 <u>OEBA</u> **1**27 30 T CLKBA

28

LEBA [

29 T CLKENBA

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

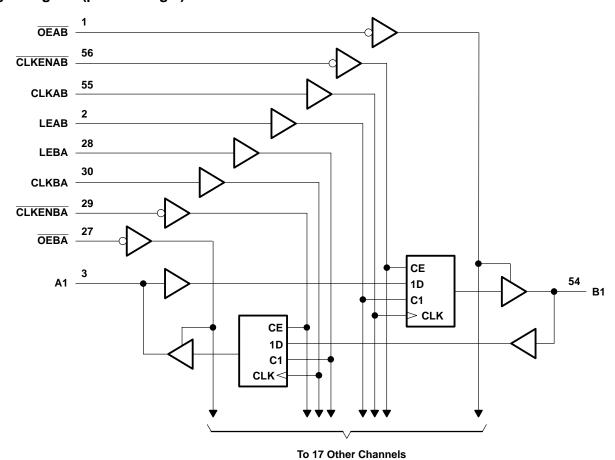
The SN74ALVCHR16601 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE†

	INPUTS									
CLKENAB	OEAB LEAB CLKAB A			В						
Х	Н	Х	Х	Χ	Z					
Х	L	Н	Χ	L	L					
Х	L	Н	Χ	Н	Н					
Н	L	L	Χ	Χ	в ₀ ‡					
L	L	L	\uparrow	L	L					
L	L	L	\uparrow	Н	Н					
L	L	L	L or H	Χ	в ₀ ‡					

[†]A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

logic diagram (positive logic)



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[‡] Output level before the indicated steady-state input conditions were established

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG	package 81°C/W
DGV p	package 86°C/W
DL pa	ckage 74°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	_
1	I limb lavel autout avenue	V _{CC} = 2.3 V		-6	
ЮН	High-level output current	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
1	Low lovel output ourrest	V _{CC} = 2.3 V		6	^
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN74ALVCHR16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	NDITIONS	vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2				
		I _{OH} = -4 mA		2.3 V	1.9				
Vон		Jan - 6 mA		2.3 V	1.7			V	
		$I_{OH} = -6 \text{ mA}$		3 V	2.4				
		I _{OH} = -8 mA		2.7 V	2				
		I _{OH} = -12 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 2 \text{ mA}$		1.65 V			0.45		
		$I_{OL} = 4 \text{ mA}$		2.3 V			0.4		
VOL		I _{OL} = 6 mA		2.3 V 0.55			V		
		IOL = 0 IIIA		3 V			0.55		
		I _{OL} = 8 mA		2.7 V			0.6		
		I _{OL} = 12 mA		3 V			0.8		
IĮ		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.03 V	-25				
		V _I = 0.7 V		2.3 V	45				
I _I (hold)		V _I = 1.7 V		2.5 V	-45			μΑ	
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_{\parallel} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
loz§		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ	
Δl _{CC}		One input at V _{CC} – 0.6 V,	Other inputs at $V_{\hbox{\footnotesize CC}}$ or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		4		pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 $[\]mbox{\$}$ For I/O ports, the parameter $\mbox{I}_{\mbox{\scriptsize OZ}}$ includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			VCC =	1.8 V	V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency			†		150		150		150	MHz	
	Pulse LE high			†		3.3		3.3		3.3		ns
t _W	duration	CLK high or low		†		3.3		3.3		3.3		110
		Data before CLK↑		†		2.3		2.4		2.1		
١.	Setup time	etup time Data before LE↓	CLK high	†		2		1.6		1.6		
t _{su}	Setup time	Data before LEV	CLK low	†		1.3		1.2		1.1		ns
		CLKEN before CLK↑		†		2		2		1.7		
		Data after CLK↑		†		0.7		0.7		0.8		
. .	Hold time	CLK high † 1.3 1.6		1.4]						
th	noia time	Data after LE↓	CLK low	†		1.7		2		1.7		ns
		CLKEN after CLK↑		t		0.3		0.5		0.6		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	A or B			†	1	4.8		5.1	1	4.4	
^t pd	LEAB or LEBA	B or A		†	1	5.5		5.8	1	5.1	ns
	CLKAB or CLKBA			†	1.2	5.9		6.3	1.4	5.4	
t _{en}	OEAB or OEBA	B or A		†	1.1	6.3		6.6	1.1	5.6	ns
^t dis	OEAB or OEBA	B or A		†	1	4.2		5.1	1.6	4.7	ns

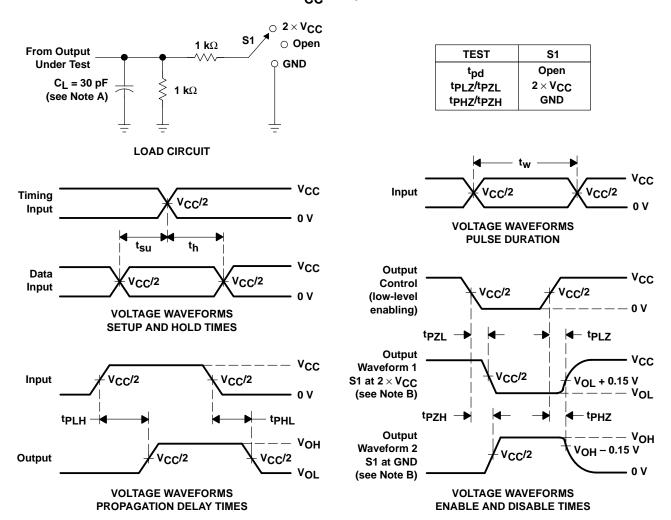
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	CINIT		
	Power dissipation	Outputs enabled	Cı = 0. f = 10 MHz	†	56	63	pF	
Cp	d capacitance	Outputs disabled	$C_L = 0$, $f = 10 MHz$	†	12	13	рΓ	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



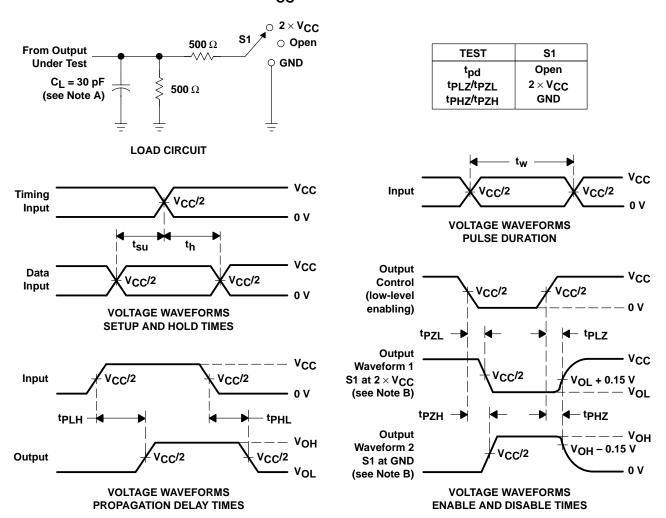
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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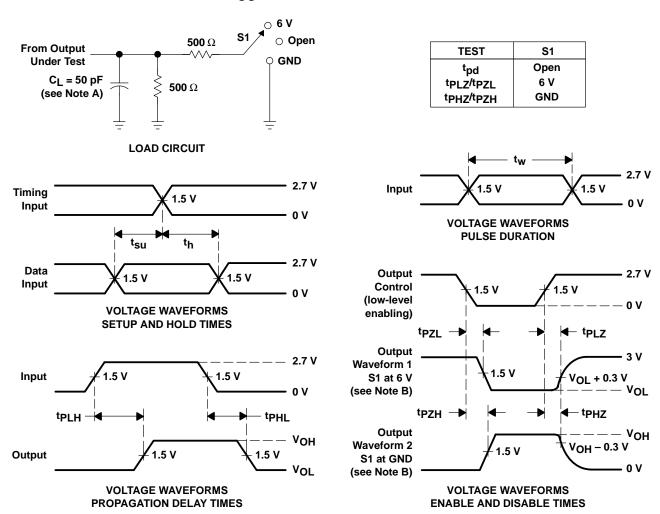
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **Package Options Include Plastic Thin** Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

NOTE: For order entry:

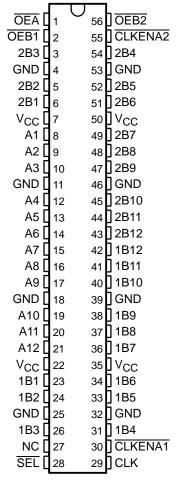
The DGG package is abbreviated to G, and the DGV package is abbreviated to V.

description

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR16269A is used in applications in which two ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (\overline{OEA} , $\overline{OEB1}$, and $\overline{OEB2}$).

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to OE being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

ISTRUMENTS

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description (continued)

All outputs are designed to sink up to 12 mA and include equivalent $26-\Omega$ resistors to reduce overshoot and undershoot.

The SN74ALVCHR16269A is characterized for operation from -40°C to 85°C.

Function Tables

OUTPUT ENABLE

	INPUTS		OUTPUTS			
CLK	CLK OEA OEB		Α	1B, 2B		
1	Н	Н	Z	Z		
1	Н	L	Z	Active		
\uparrow	L	Н	Active	Z		
1	L	L	Active	Active		

A-TO-B STORAGE (OEB = L)

	INPUTS						
CLKENA1	LKENA1 CLKENA2 CLK A			1B	2B		
L	Н	↑	L	L	2B ₀ †		
L	Н	\uparrow	Н	Н	2B ₀ †		
L	L	\uparrow	L	L	L		
L	L	\uparrow	Н	Н	Н		
Н	L	\uparrow	L	1B ₀ †	L		
Н	L	\uparrow	Н	1B ₀ †	Н		
Н	Н	Χ	Χ	1B ₀ †	2B ₀ †		

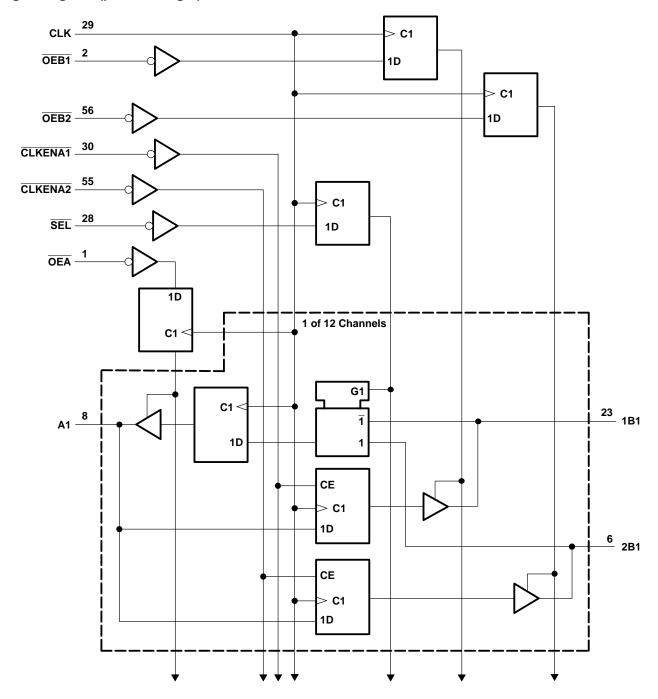
[†]Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEA = L)

	INP	ОИТРИТ		
CLK	SEL	1B	2B	Α
Х	Н	Χ	Х	A ₀ †
Х	L	Χ	Χ	А _О Т А _О †
1	Н	L	X	L
1	Н	Н	X	Н
1	L	Χ	L	L
1	L	Χ	Н	Н

[†] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	/IH High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
la	High-level output current	V _{CC} = 2.3 V		-6	mA	
ЮН		$V_{CC} = 2.7 \text{ V}$		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
lOL	Low level output ourrent	V _{CC} = 2.3 V		6	1 .	
	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST CO	ONDITIONS	vcc	MIN	TYP†	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2			
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2				
		I _{OH} = -4 mA		2.3 V	1.9				
Vон		I _{OH} = -6 mA		2.3 V	1.7			V	
VOH		IOH = -0 IIIA		3 V	2.4				
		I _{OH} = -8 mA		2.7 V	2				
		I _{OH} = -12 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		$I_{OL} = 2 \text{ mA}$		1.65 V			0.45		
		I _{OL} = 4 mA		2.3 V			0.4		
VOL		I _{OL} = 6 mA	2.3 V			0.55	V		
		IOL = 0 IIIA	3 V			0.55			
		$I_{OL} = 8 \text{ mA}$	2.7 V			0.6			
		I _{OL} = 12 mA		3 V			0.8		
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.03 V	-25				
		V _I = 0.7 V	/ _I = 0.7 V]	
II(hold)		V _I = 1.7 V	/ _I = 1.7 V		-45			μΑ	
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 7	-75]	
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
l _{OZ} §		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ	
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at $V_{\hbox{\footnotesize CC}}$ or GND	3 V to 3.6 V			750	μΑ	
C _i C	control inputs	$V_I = V_{CC}$ or GND		3.3 V		5		pF	
C _{io} A	or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V} $ $V_{CC} = 2.7 \text{ V}$		V _{CC} = 3.3 V ± 0.3 V		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock freque	ncy		†		95		115		135	MHz
t _W	Pulse duration	on, CLK high or low	†		5.2		4.3		3.3		ns
		A data before CLK↑	†		1.4		1.4		1		
		B data before CLK↑	†		1.6		1.5		1.1		
t _{su}	Setup time	SEL before CLK↑	†		0.8		1.1		1.3		ns
		CLKENA1 or CLKENA2 before CLK↑	†		0.8		1		0.8		
		OE before CLK↑	†		1.7		1.6		1.2		
		A data after CLK↑	†		0.9		0.9		1.2		
		B data after CLK↑	†		0.8		0.6		1		
^t h	Hold time	SEL after CLK↑	†		1.1		0.8		1.7		ns
		CLKENA1 or CLKENA2 after CLK↑	†		1.4		1		1.6		
		OE after CLK↑	†		0.9		0.8		1.2		

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		95		115		135		MHz
	CLK	В		†	2.3	7.7		6.9	2.2	5.8	ns
^t pd	CLK	А		†	1.9	6.4		5.8	2	5.2	115
	CLK	В		†	2.5	7.7		6.9	2.3	5.8	ne
^t en	CLK	Α		†	2.2	6.7		6	2.1	5.3	ns
4	CLK	В		†	3.3	8.1		6.7	2.4	6	ne
^t dis	CLK	Α		†	2.7	8		6.2	2.1	6	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

DADAMETED			PARAMETER TEST CONDITIONS				TEST CONDITIONS V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} = 3.3 V	UNIT
	FARAMETER	•	1E31 CONDITIONS	TYP	TYP	TYP	ONIT			
<u> </u>	Power dissipation	All outputs enabled	Cı = 0. f = 10 MHz	†	142	172	PF			
^C pd capacita	capacitance	All outputs disabled	$C_L = 0$, $f = 10 MHz$	†	115	129	рг			

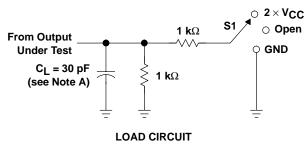
[†] This information was not available at the time of publication.

VCC

0 V

V_{CC}/2

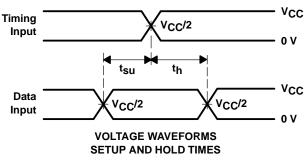
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

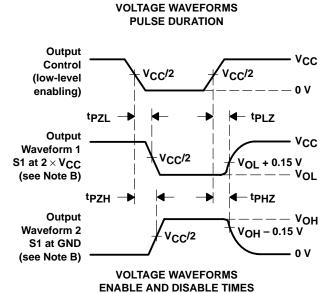


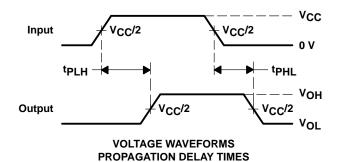
TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

V_{CC}/2

Input





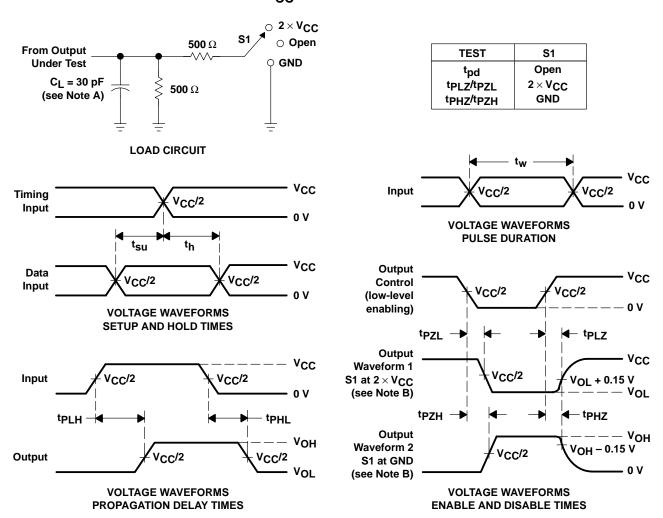


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

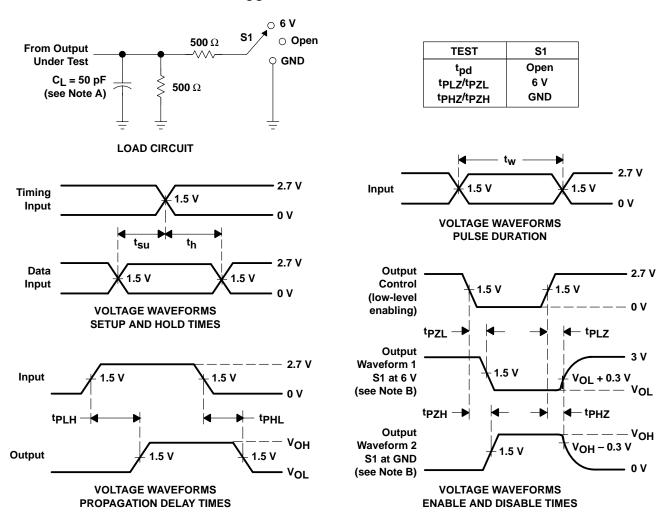


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DGG OR DL PACKAGE

(TOP VIEW)

- Member of the Texas Instruments Widebus™ Family
- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit flip-flop is designed for low-voltage 1.65-V to 3.6-V V_{CC} operation.

The 20 flip-flops of the SN74ALVCH162721 are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (\overline{OE}) input places the 20 outputs in either a normal logic state (high or low level) or the high-impedance state. In the high-impedance state, the outputs neither load

<u>oe</u> [56 CLK 55 D1 Q1 2 Q2 **П**3 54 D2 GND 4 53 GND Q3 🛮 5 52 N D3 Q4 🛮 6 51 D4 50 V_{CC} V_{CC} 47 Q5 8 49 N D5 Q6 🛮 9 48 D6 Q7 10 47 D7 46 GND GND 11 45 D8 Q8 🛮 12 Q9 1 13 44 **∏** D9 Q10 114 43 D10 Q11 15 42 D11 41 D12 Q12 I 16 40 **□** D13 Q13 17 GND 18 39 GND 38 D14 Q14 119 37 D15 Q15 Π 20 36 D16 Q16 21 V_{CC} 122 35 V_{CC} Q17 **2**3 34 D17 Q18 24 33 D18 GND ∏25 32 I GND 31 D19 Q19 26 30 D20 Q20 27

NC - No internal connection

NC **1**28

29 CLKEN

nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

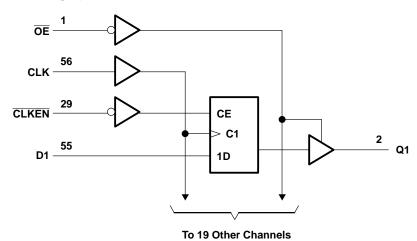
The SN74ALVCH162721 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

FUNCTION TABLE (each flip-flop)

	OUTPUT			
OE	CLKEN	CLK	D	Q
L	Н	Х	Χ	Q ₀ H
L	L	\uparrow	Н	Н
L	L	\uparrow	L	L
L	L	L or H	Χ	Q ₀ Z
Н	X	X	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	٧
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
lou	High lovel output ourrent	V _{CC} = 2.3 V		-6	mA
IOH	High-level output current	V _{CC} = 2.7 V		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low-level output current	V _{CC} = 2.3 V		6	mA
lOL	Low-level output current	V _{CC} = 2.7 V		8	IIIA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	.2		
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
Voн	I _{OH} = -6 mA	2.3 V	1.7			V
	10H = -0 111A	3 V	2.4			
	$I_{OH} = -8 \text{ mA}$	2.7 V	2			
	$I_{OH} = -12 \text{ mA}$	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 2 mA	1.65 V			0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
V _{OL}	I _{OL} = 6 mA	2.3 V			0.55	V
	IOL = 6 IIIA	3 V			0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
	I _{OL} = 12 mA	3 V			0.8	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	V _I = 0 to 3.6 V [‡]	3.6 V			±500	
loz	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
C _i	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF
Co	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			§		150		150		150	MHz
t _W	Pulse duration, CLK high or low		§		3.3		3.3		3.3		ns
	0.4	Data before CLK↑	§		4		3.6		3.1		20
tsu	Setup time	CLKEN before CLK↑	§		3.4		3.1		2.7		ns
4.	11.112	Data after CLK↑	§		0		0		0		20
th	Hold time	CLKEN after CLK↑	§		0		0		0		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
^t pd	CLK	Q		†	1	6.7		6.2	1	5.3	ns
^t en	OE	Q		†	1	7.2		7	1	5.8	ns
^t dis	OE	Q		†	1	6.3		5.4	1	5	ns

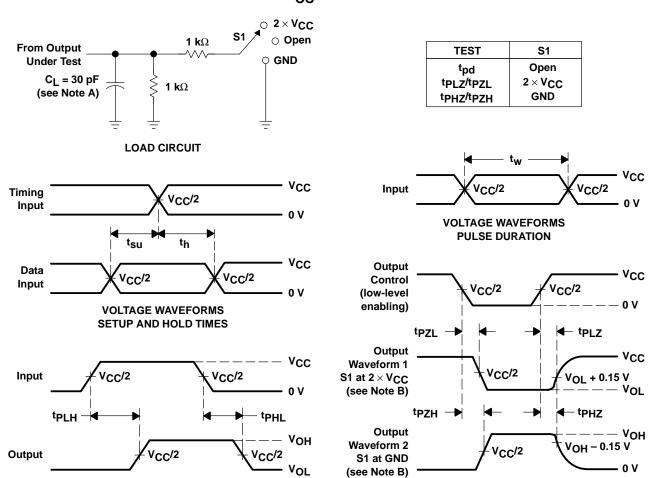
[†] This information was not available at the time of publication.

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER			NDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FARAMETER	1231 00	NDITIONS	TYP	TYP	TYP	ONIT	
	Power dissipation	Outputs enabled	C 50 nE	f = 10 MHz	†	55	59	pF
Cpd	capacitance	Outputs disabled	$C_L = 50 pF$,	1 = 10 NIMZ	†	46	49	рΓ

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

VOLTAGE WAVEFORMS

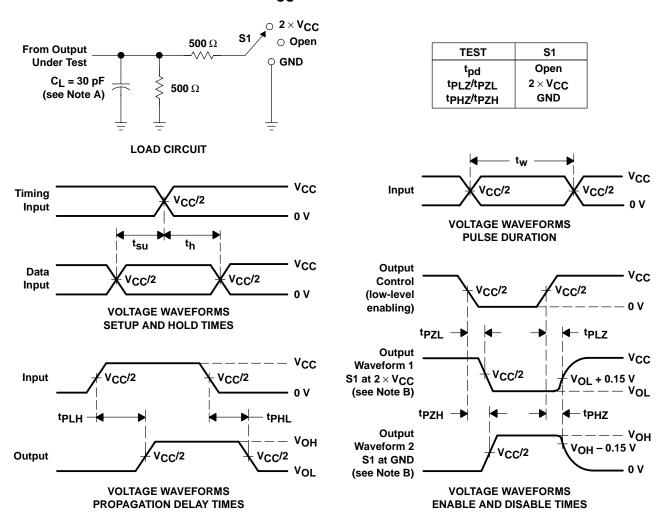
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

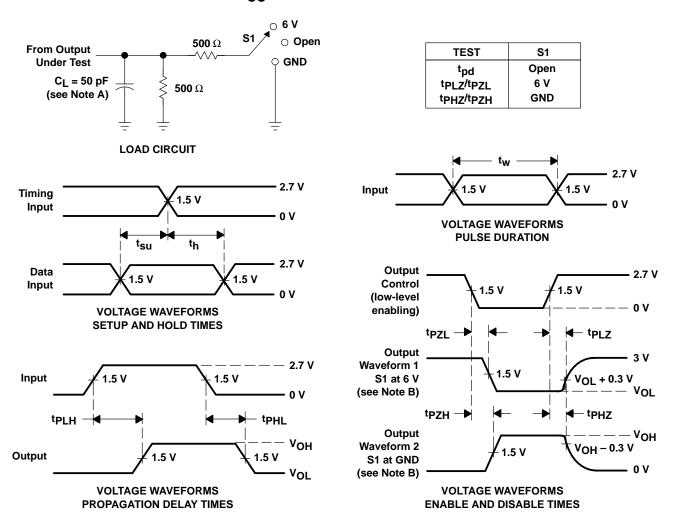


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

SCES012E - JULY 1995 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Shrink** Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

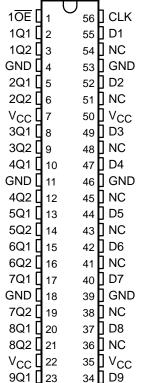
description

testing of all parameters.

This 10-bit flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

SN74ALVCH162820 flip-flops edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.



NC - No internal connection

33 NC

32 GND

31 D10

30 NC

29 NC

9Q2 🛮 24

GND [] 25

10Q1 26

10Q2 [] 27

20E 28

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162820 is characterized for operation from -40°C to 85°C.

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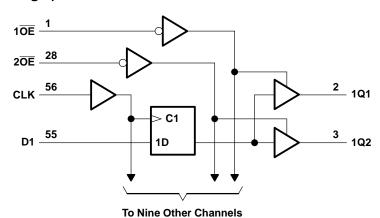
SCES012E - JULY 1995 - REVISED FEBRUARY 1999

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE _n †	CLK	Q	
L	1	Н	Н
L	\uparrow	L	L
L	L	Χ	Q_0
Н	Χ	Χ	Z

†n = 1, 2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	-0.5 V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES012E – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	٧
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
٧ıH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
1	High level output ourrest	V _{CC} = 2.3 V		-6	A
IOH	High-level output current	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low lovel cutout current	V _{CC} = 2.3 V		6	mA
lOL	Low-level output current	V _{CC} = 2.7 V		8	MA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	/ Vcc-C	.2		
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
		I _{OH} = -4 mA	2.3 V	1.9			
Vон		lour 6 mA	2.3 V	1.7			V
		$I_{OH} = -6 \text{ mA}$	3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V	/		0.2	
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.4	
VOL		La. 0.44	2.3 V			0.55	V
		IOL = 6 mA	3 V		-	0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
Ιį		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _I (hold)		V _I = 1.7 V	2.3 V	-45			μΑ
, ,		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		V _O = V _{CC} or GND	3.6 V			±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V, Other inputs	s at V _{CC} or GND 3 V to 3.6 V			750	μΑ
	Control inputs		001/		3.5		
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		6		pF
Со	Outputs	V _O = V _{CC} or GND	3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		1.7		1.8		1.4		ns
th	Hold time, data after CLK↑	§		1.1		1.1		1		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(INFOT) (COTFOT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	6.4		6.2	1	5.4	ns
t _{en}	ŌĒ	Q		†	1	6.9		6.8	1	5.6	ns
t _{dis}	ŌĒ	Q		†	1	6.2		5.5	1	5	ns

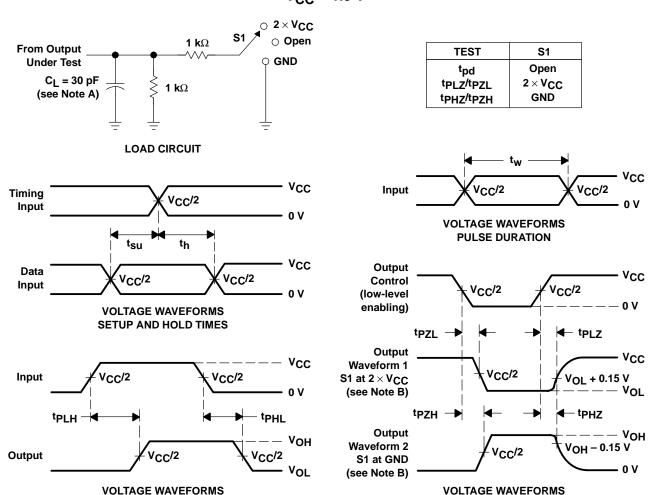
[†]This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETE	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	= 2.5 V V _{CC} = 3.3 V		
	171101111212		1201 001151110110	TYP	TYP	TYP	UNIT
	Power dissipation capacitance	All outputs enabled	C _I = 50 pF, f = 10 MHz	†	68	66	pF
C _{pd}	per flip-flop	All outputs disabled	CL = 50 pr, 1 = 10 MHZ	†	39	47	ρг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

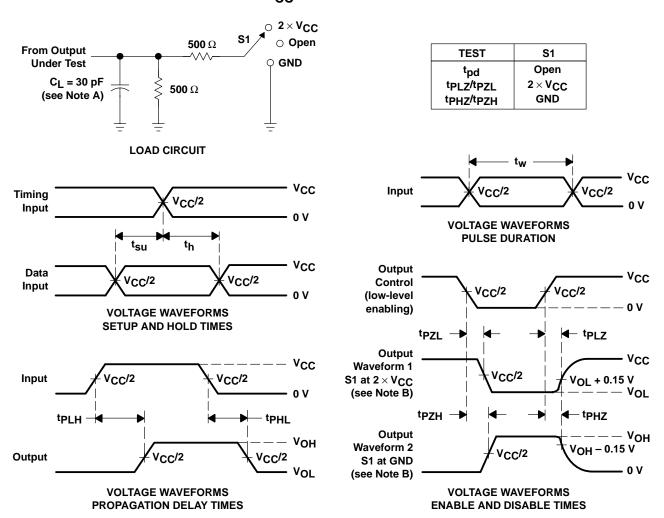
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

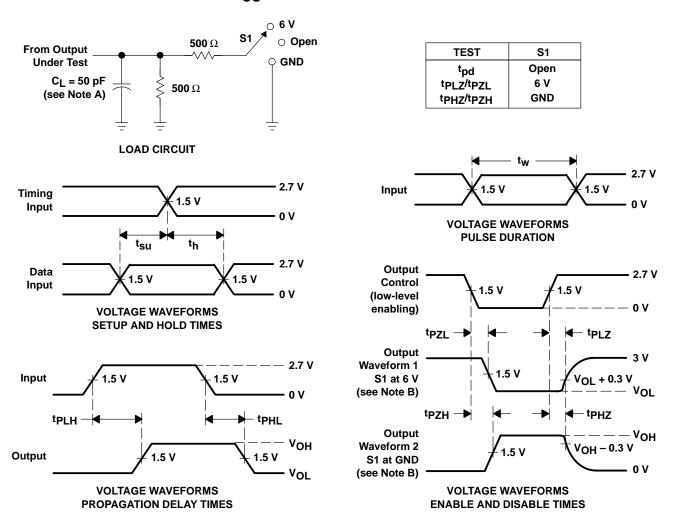


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



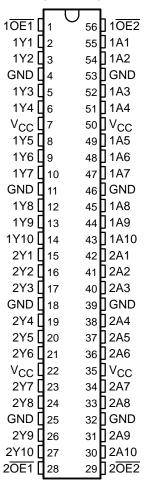
- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 20-bit noninverting buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance

DGG, DGV, OR DL PACKAGE (TOP VIEW)



The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

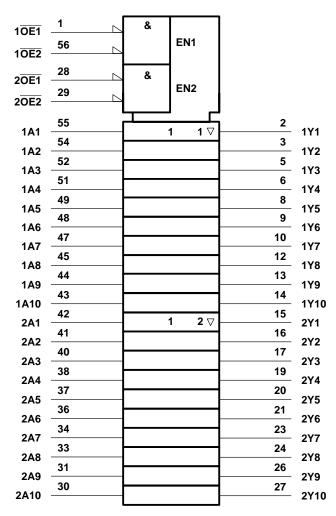
The SN74ALVCH162827 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLE (each 10-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Χ	Н	Χ	Z

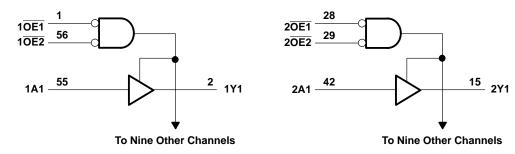
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG pack	age 81°C/W
	age 86°C/W
DL packag	ge
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	٧
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
	H High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current Input transition rise or fall rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 1.65 V		-2	
1	High level output ourrent	V _{CC} = 2.3 V		-6	A
ЮН	nign-ievei output current	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
1	Law lavel output ourrent	V _{CC} = 2.3 V		6	
IOL	Low-level output current	V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT		
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.:	2				
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2					
VOH VOL II II(hold) IOZ ICC AICC	I _{OH} = -4 mA	2.3 V	1.9						
∨он		In. 6 mA	2.3 V	1.7			V		
		IOH = -6 mA	3 V	2.4					
		I _{OH} = -8 mA	2.7 V	2					
		I _{OH} = -12 mA	3 V	2					
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2			
		I _{OL} = 2 mA	1.65 V			0.45			
		I _{OL} = 4 mA	2.3 V			0.4			
VOL		1- C A	2.3 V			0.55	V		
	VOL II II(hold) IOZ ICC ΔICC C: Control inputs	I _{OL} = 6 mA	3 V			0.55			
		I _{OL} = 8 mA	2.7 V			0.6			
		I _{OL} = 12 mA	3 V			0.8			
lį		V _I = V _{CC} or GND	3.6 V			±5	μΑ		
		V _I = 0.58 V	1.65 V	25					
		V _I = 1.07 V	1.65 V	-25					
		V _I = 0.7 V	2.3 V	45					
I _I (hold)		V _I = 1.7 V	2.3 V	-45			μΑ		
		V _I = 0.8 V	3 V	75					
		V _I = 2 V	3 V	-75					
		$V_{ } = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500			
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ		
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ		
∆lcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GN	ND 3 V to 3.6 V			750	μΑ		
	Control inputs		3.3 V		3.5		nΕ		
<u>ا</u>	Data inputs	V _I = V _{CC} or GND	3.3 V		6		pF		
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF		

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	§	1	4.4		4.4	1.5	3.8	ns
t _{en}	ŌĒ	Y	§	1.4	6.3		6.2	1.6	5.1	ns
^t dis	ŌĒ	Y	§	1.7	5.9		5.2	1.8	4.7	ns

[§] This information was not available at the time of publication.



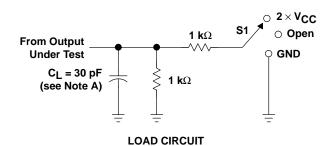
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

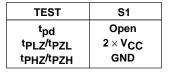
operating characteristics, $T_A = 25^{\circ}C$

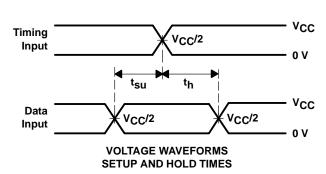
	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	ONIT
	Power dissipation	Outputs enabled	C _I = 50 pF. f = 10 MHz	†	16	18	»E
Ср	d capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	†	4	6	pF

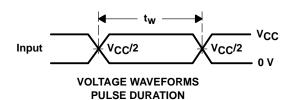
[†] This information was not available at the time of publication.

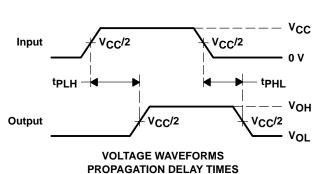
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

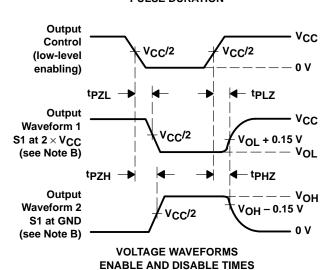












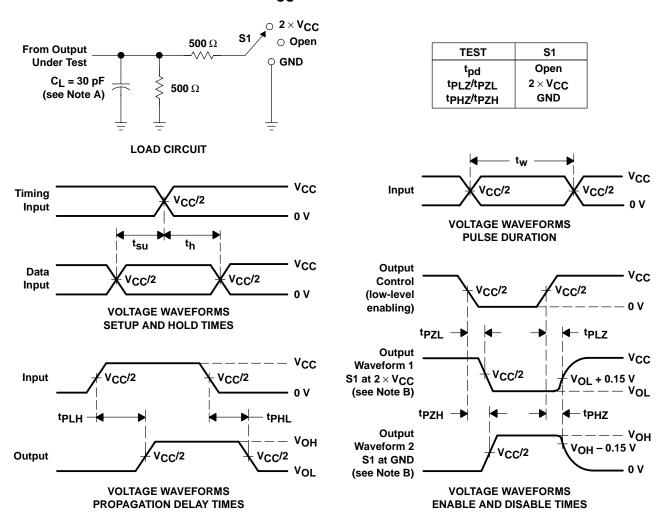
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- tpZL and tpZH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

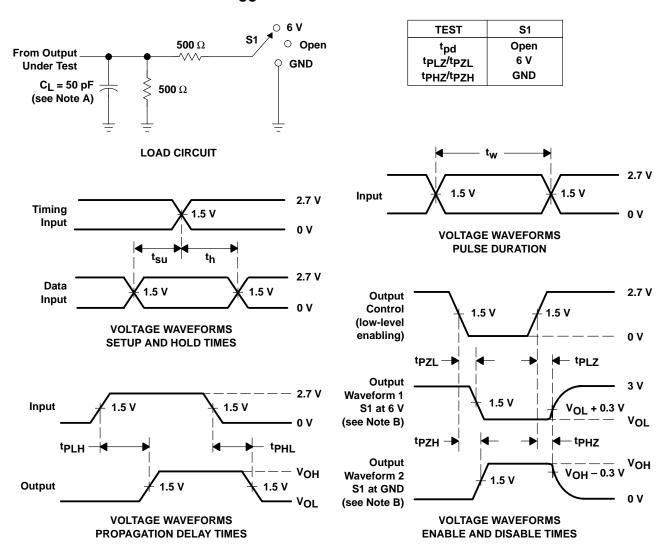


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DBB PACKAGE

(TOP VIEW)

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Packaged in Thin Very Small-Outline **Package**

description

This 1-bit to 2-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH162830 is characterized for operation from -40°C to 85°C.

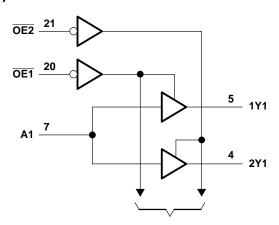
			1
2Y2 [1	\bigcup_{80}	1Y3
1Y2 [79	2Y3
GND [3	79 78	GND
2Y1 [4	77	1Y4
1Y1 [5	76	5 2Y4
V _{CC} [6	75	V _{CC}
A1 [7	74	1Y5
A2 [8	73	2Y5
GND [9	72	GND
A3 [10	71	1Y6
A4 [11	70	2Y6
GND [12	69	GND
A5 [13	68	1Y7
A6 [14	67	2Y7
V _{CC} [15	66	Vcc
A7 [16	65	1Y8
A8 [17	64	2Y8
GND [18	63	GND
A9 [19	62	1Y9
OE1	20	61	2Y9
OE2	21	60	[] 1Y10
A10 [22	59	[] 2Y10
GND [23	58	GND
A11 [24	57	1Y11
A12 [25	56	2Y11
Vcc [26	55	Vcc
A13 [27	54	ቨ 1Y12
A14 [28	53	7 2Y12
GND [29	52	GND
A15 [30	51	[1Y13
A16 [31	50	5 2Y13
GND [32	49	GND
A17 [33	48	[] 1Y14
A18 [34	47] 2Y14
Vcc [35	46] V _{CC}
2Y18 [36	45] 1Y15
1Y18 [37	44	2Y15
GND [38	43	GND
2Y17 [39	42] 1Y16
1Y17 [40	41	2Y16
			-

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FUNCTION TABLE

	INPUTS	OUTI	PUTS	
OE1	OE2	Α	1Yn	2Yn
L	Н	Н	Н	Z
L	Н	L	L	Z
Н	L	Н	z	Н
Н	L	L	Z	L
L	L	Н	Н	Н
L	L	L	L	L
Н	Н	Χ	Z	z

logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
ViH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
	V _{IH} High-level input voltage V _{IL} Low-level input voltage V _I Input voltage V _O Output voltage IOH High-level output current Δt/Δv Input transition rise or fall rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ı	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
lau	High level output ourrent	V _{CC} = 2.3 V		-6	mA	
IOH	IL Low-level input voltage I Input voltage O Output voltage DH High-level output current DL Low-level output current t/∆v Input transition rise or fall rate	V _{CC} = 2.7 V		-8	IIIA	
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
la.	Low level output ourrent	V _{CC} = 2.3 V		6	m ^	
IOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
	V _{CC} = 3 V			12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT
		IOH = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -2 mA	1.65 V	1.2			
VOH VOL II	I _{OH} = -4 mA	2.3 V	1.9				
Vон		la 6 mA	2.3 V	1.7			V
		IOH = -6 mA	3 V	2.4			
		I _{OH} = -8 mA	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.4	
VOL		1- C A	2.3 V			0.55	V
V _{OL}	IOL = 6 mA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
Ц		V _I = V _{CC} or GND	3.6 V			±5	μΑ
		V _I = 0.58 V	1.65 V	25			
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ
` ´		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or G	ND 3 V to 3.6 V			750	μΑ
	Control inputs		3.3 V		4.5		~F
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5		pF
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	А	Y	§	1.2	3.8		4	1.7	3.5	ns
t _{en}	ŌĒ	Υ	§	1	5.7		5.7	1	4.8	ns
^t dis	ŌĒ	Υ	§	1.5	6.2		5.4	1.7	5.2	ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

VOLTAGE WAVEFORMS

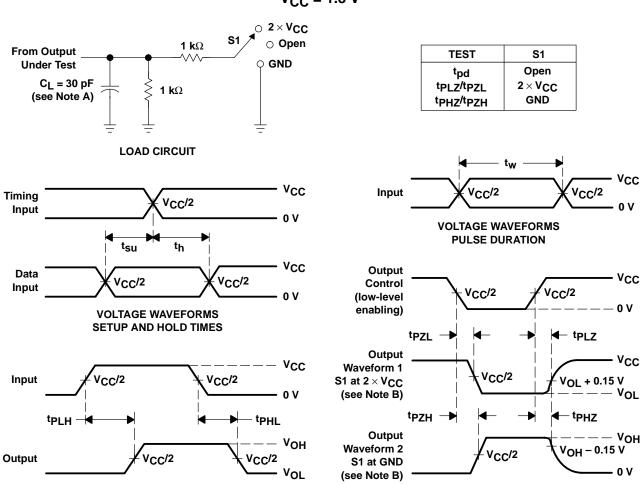
ENABLE AND DISABLE TIMES

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} = 3.3 V	UNIT		
		TEST CONDITIONS	TYP	TYP	TYP	UNIT	
	Power dissipation	All outputs enabled	Cı = 0. f = 10 MHz	†	50	54	PΓ
Cpd	capacitance	All outputs disabled	$C_L = 0$, $f = 10 MHz$	†	8	8	þг

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

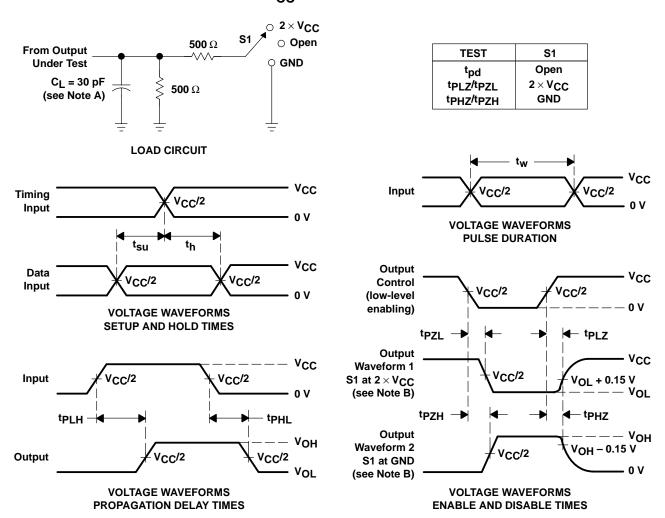
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



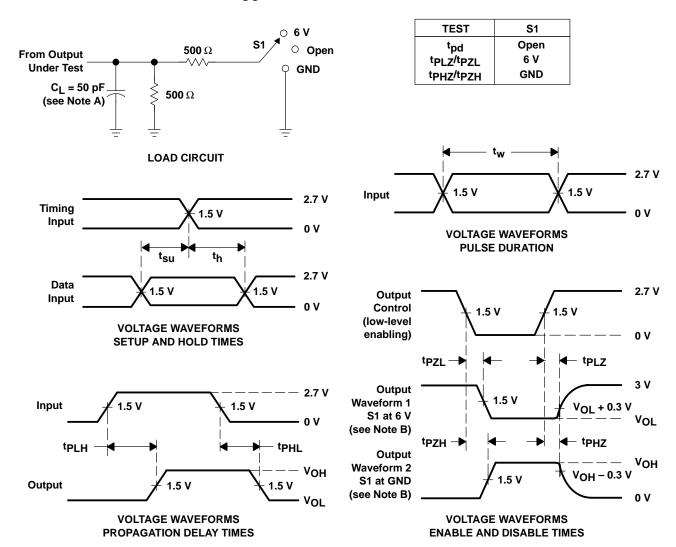
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 3. Load Circuit and Voltage Waveforms

DBB PACKAGE

SCAS605A - APRIL 1998 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Packaged in Thin Very Small-Outline **Package**

description

This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

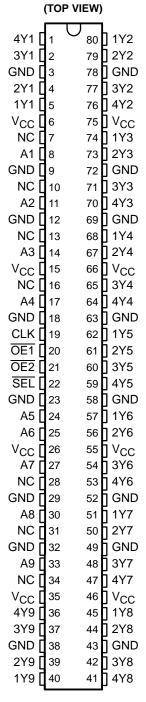
The device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVC162831 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When SEL is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (OE) inputs. Each OE controls two groups of nine outputs.

When SEL is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. OE controls operate the same as in buffer mode.

When \overline{OE} is logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is logic high, the outputs are in the high-impedance state.

SEL and OE do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



NC - No internal connection

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description (continued)

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

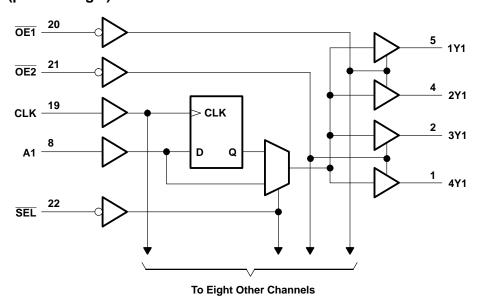
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC162831 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	OUTPUT			
OE	SEL	CLK	Α	Υ
Н	Х	Х	Х	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н

logic diagram (positive logic)





SN74ALVC162831 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OLITPLITS

SCAS605A - APRIL 1998 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
la	High-level output current	V _{CC} = 2.3 V		-6	mA
IOH		V _{CC} = 2.7 V		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		6	A
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004. SCAS605A - APRIL 1998 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CONDITIONS	VCC	MIN TY	PT MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			
		I _{OH} = −2 mA	1.65 V	1.2			
		I _{OH} = -4 mA	2.3 V	1.9			
۷он		I _{OH} = -6 mA	2.3 V	1.7		V	
		10H = -0 IIIA	3 V	2.4			
		I _{OH} = -8 mA	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2		
		$I_{OL} = 2 \text{ mA}$	1.65 V	1.65 V			
		$I_{OL} = 4 \text{ mA}$	2.3 V		0.4	V	
V_{OL}		I _{OL} = 6 mA	2.3 V		0.55		
		IOL = 0 IIIA	3 V		0.55		
		$I_{OL} = 8 \text{ mA}$	2.7 V		0.6		
		I _{OL} = 12 mA	3 V		0.8		
II		$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ	
loz		$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
∆lcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GI	ND 3 V to 3.6 V		750	μΑ	
C.	Control inputs	Vi – Voo or GND	3.3 V		4.5	nE.	
Ci	Data inputs	V _I = V _{CC} or GND	3.3 V		4.5	pF	
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5	pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		‡		150		150		150	MHz
t _W	Pulse duration, CLK high or low	‡		3.3		3.3		3.3		ns
t _{su}	Setup time, A data before CLK↑	‡		2		2		1.6		ns
t _h	Hold time, A data after CLK↑	‡		0.7		0.5		1.1		ns

[‡] This information was not available at the time of publication.

SN74ALVC162831 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

SCAS605A - APRIL 1998 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(INFOT) (COTFOT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1.1	4.7		4.8	1.5	4.3	
t _{pd}	CLK	Y		†	1	5.3		5.3	1.4	4.7	ns
·	SEL			†	1.1	6		6.2	1.5	4.8	
^t en	ŌĒ	Υ		†	1	5.9		5.9	1.1	5.1	ns
^t dis	ŌĒ	Y		†	1	5.4		5.4	1.6	5.1	ns

[†] This information was not available at the time of publication.

switching characteristics from 0° C to 65° C, $C_L = 50$ pF

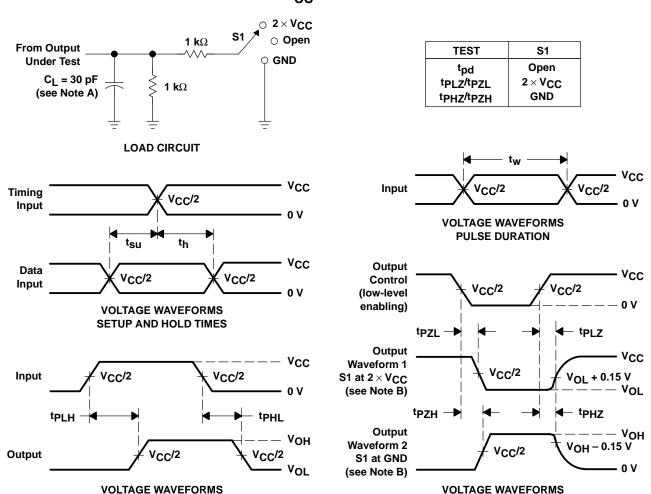
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(111 01)	(6611 61)	MIN	MAX	
^t pd	CLK	Υ	1.9	4.5	ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS -		V _{CC} = 1.8 V	V _{CC} = 2.5 V V _{CC} = 3.3 V		UNIT		
				TYP	TYP	TYP	UNIT		
	Power dissipation	Outputs enabled	C: 0		$C_1 = 0$, $f = 10 \text{ MHz}$	†	119	132	pF
Cpd	capacitance	Outputs disabled	$C_L = 0$,	f = 10 MHz	†	22	25	pr	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

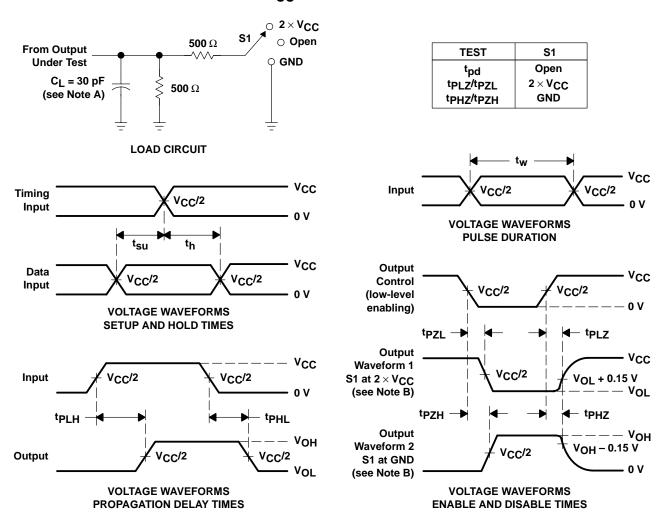
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

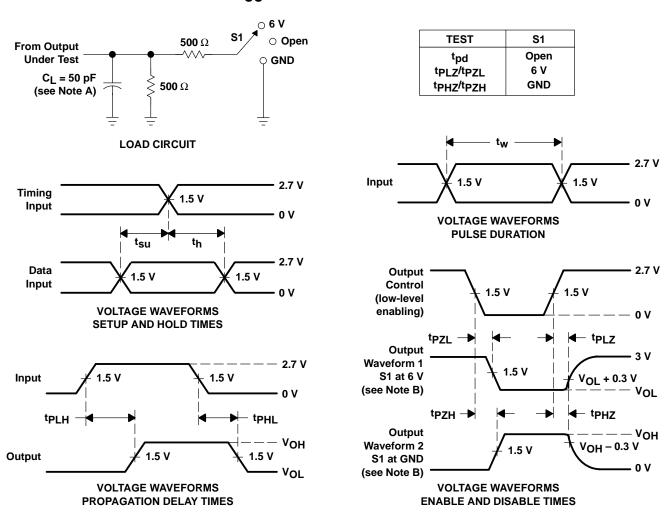


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzl and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



DBB PACKAGE

(TOP VIEW)

SCES084E - AUGUST 1996 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Packaged in Thin Very Small-Outline **Package**

description

This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

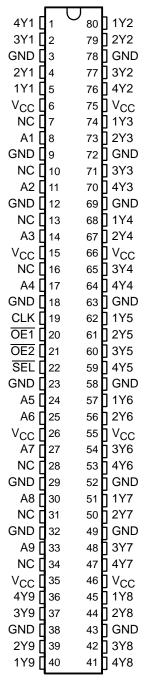
The device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVCH162831 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When SEL is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) inputs. Each OE controls two groups of nine outputs.

When SEL is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. OE controls operate the same as in buffer mode.

When \overline{OE} is logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is logic high, the outputs are in the high-impedance state.

SEL and OE do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



NC - No internal connection

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SCES084E - AUGUST 1996 - REVISED FEBRUARY 1999

description (continued)

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

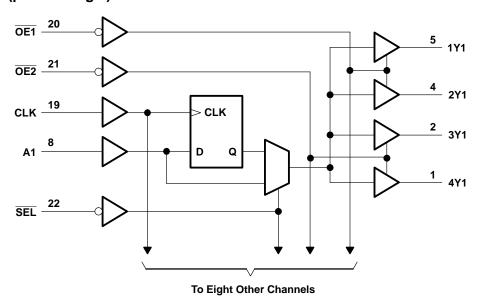
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162831 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP		OUTPUT	
OE	SEL	CLK	Α	Y
Н	Х	Х	Χ	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н

logic diagram (positive logic)





SN74ALVCH162831 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

SCES084E - AUGUST 1996 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
	V _{IH} High-level input voltage V _{IL} Low-level input voltage V _I Input voltage V _O Output voltage IOH High-level output current IOL Low-level output current Δt/Δv Input transition rise or fall rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage	·	0	Vcс	V	
۷o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
1	Link lavel autout aumont	V _{CC} = 2.3 V		-6	mA	
ЮН	nigh-level output current	$V_{CC} = 2.7 \text{ V}$		-8		
	Vo Output voltage Vo Output voltage Vo High-level output current Vo Voltage Volt	V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Law lavel autout augreet	V _{CC} = 2.3 V		6	A	
IOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SCES084E - AUGUST 1996 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} -0.	2		
		I _{OH} = -2 mA		1.65 V	1.2			
		I _{OH} = -4 mA		2.3 V	1.9			
Vон		Laure Caro		2.3 V	1.7			V
		IOH = -6 mA		3 V	2.4			
		I _{OH} = -8 mA		2.7 V	2			
		I _{OH} = -12 mA		3 V	2			
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA		1.65 V			0.45	
		I _{OL} = 4 mA		2.3 V			0.4	
VOL		1 C A		2.3 V			0.55	V
		I _{OL} = 6 mA		3 V		-	0.55	
		I _{OL} = 8 mA	2.7 V			0.6		
		I _{OL} = 12 mA		3 V			0.8	
lį		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ
		V _I = 0.58 V		1.65 V	25			
		V _I = 1.07 V		1.65 V	-25			
		V _I = 0.7 V		2.3 V	45			
I _I (hold)		V _I = 1.7 V		2.3 V	-45			μΑ
		V _I = 0.8 V		3 V	75			
		V _I = 2 V		3 V	-75			
		$V_I = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500	
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V		-	750	μΑ
	Control inputs			227		4.5		
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		5		pF
Co	Outputs	$V_O = V_{CC}$ or GND		3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		/ V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, A data before CLK↑	§		2		2		1.6		ns
th	Hold time, A data after CLK↑	§		0.7		0.5		1.1		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162831 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

SCES084E - AUGUST 1996 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1.1	4.7		4.8	1.5	4.3	
t _{pd}	CLK	Y		†	1	5.3		5.3	1.4	4.7	ns
·	SEL			†	1.1	6		6.2	1.5	4.8	
^t en	ŌĒ	Υ		†	1	5.9		5.9	1.1	5.1	ns
^t dis	ŌĒ	Y		†	1.4	6.3		5.4	1.6	5.1	ns

[†] This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C_L = 50 pF

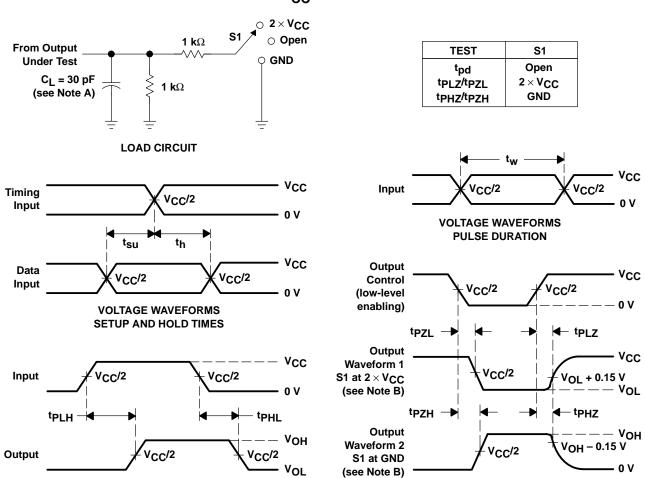
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		UNIT
	(111 01)	(6611-61)	MIN	MAX	
^t pd	CLK	Υ	1.9	4.5	ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETE	P	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAIVIETE	N.	TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation	All outputs enabled	Cı = 0. f = 10 MHz	†	119	132	nE.	
Cpd	capacitance	All outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	22	25	pF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

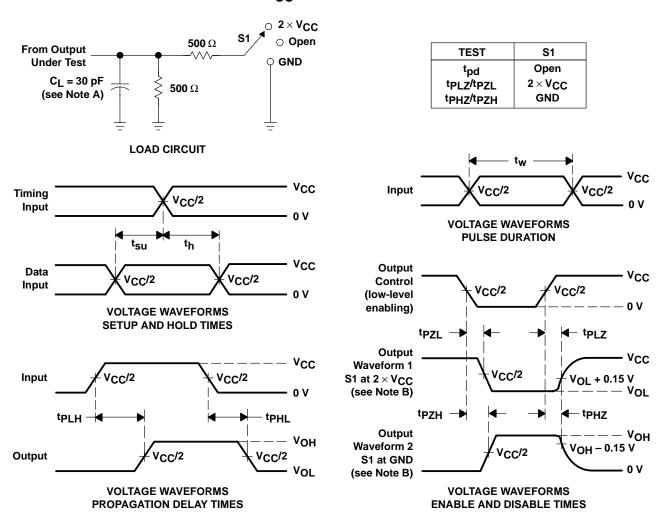
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

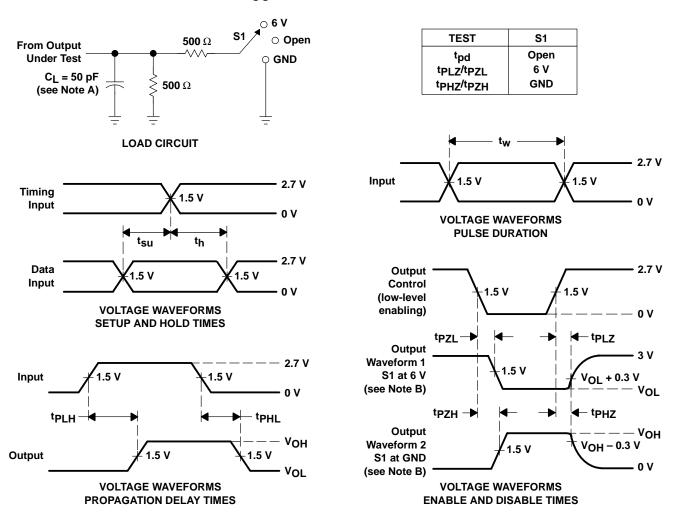


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpz and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALVCH162832 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

DGG PACKAGE

(TOP VIEW)

SCAS588E - MAY 1997 - REVISED FEBRUARY 1999

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Shrink Small-Outline Package

description

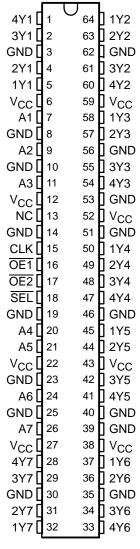
This 1-bit to 4-bit address register/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The SN74ALVCH162832 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When SEL is a logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (OE) inputs. Each OE controls two groups of seven outputs.

When SEL is a logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data at the A inputs is stored in the internal registers. OE controls operate the same as in the buffer mode.

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NC - No internal connection

When \overline{OE} is a logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is a logic high, the outputs are in the high-impedance state.

Neither SEL nor OE affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

te.
tls
de

TEXAS

testing of all parameters.

SCAS588E - MAY 1997 - REVISED FEBRUARY 1999

description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

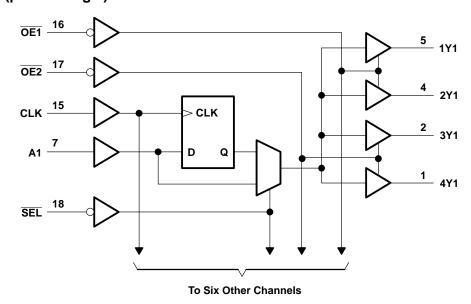
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162832 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP		OUTPUT	
OE	SEL	CLK	Α	Υ
Н	Х	Х	Х	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н

logic diagram (positive logic)





SN74ALVCH162832 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

SCAS588E - MAY 1997 - REVISED FEBRUARY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage	-	0	Vcс	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
1	High lavel autout august	V _{CC} = 2.3 V		-6	mA	
ІОН	High-level output current	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
la.	Low lovel output ourrent	V _{CC} = 2.3 V		6	A	
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate	-		10	ns/V	
TA	Operating free-air temperature		-40	85	°C	
	Operating free-air temperature		-40			

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SCAS588E - MAY 1997 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMET	R TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.	2		
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
Voн	I _{OH} = -6 mA	2.3 V	1.7			V
	10H = -0 IIIA	3 V	2.4			
	$I_{OH} = -8 \text{ mA}$	2.7 V	2			
	I _{OH} = -12 mA	3 V	2			
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	
	I _{OL} = 2 mA	1.65 V			0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
VOL	La. CmA	2.3 V			0.55	V
	IOL = 6 mA	3 V			0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
	I _{OL} = 12 mA	3 V			0.8	
Ц	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V			±500	
loz	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V ₀	CC or GND 3 V to 3.6 V			750	μΑ
Contro	inputs $V_I = V_{CC}$ or GND	3.3 V		4.5		n.E
C _i Data i	onts Al = ACC or GMD	3.3 V		5		pF
C _O Outpu	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	v _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		§		150		150		150	MHz
t _W	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, A data before CLK↑	§		2		2		1.6		ns
th	Hold time, A data after CLK↑	§		0.7		0.5		1.1		ns

[§] This information was not available at the time of publication.



[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162832 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

SCAS588E - MAY 1997 - REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFO1)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1.1	4.7		4.8	1.5	4.3	
t _{pd}	CLK	Y		†	1	5.3		5.3	1.4	4.7	ns
	SEL			†	1.1	6		6.2	1.5	4.8	
^t en	ŌĒ	Y		†	1	5.9		5.9	1.1	5.1	ns
^t dis	ŌĒ	Υ		†	1.4	6.3		5.4	1.6	5.1	ns

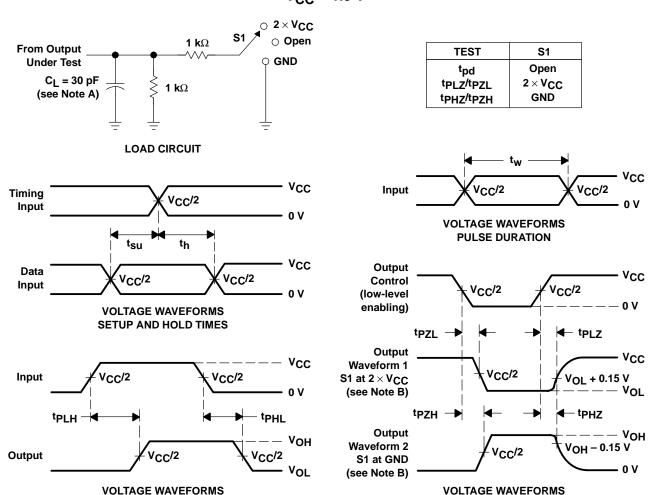
[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAMETER	•	TEST CONDITIONS	TYP	TYP	TYP	UNIT	
<u> </u>	Power dissipation	All outputs enabled	Cı = 0. f = 10 MHz	†	119	132	PF	
Cpd	capacitance	All outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	22	25] PF	

[†] This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

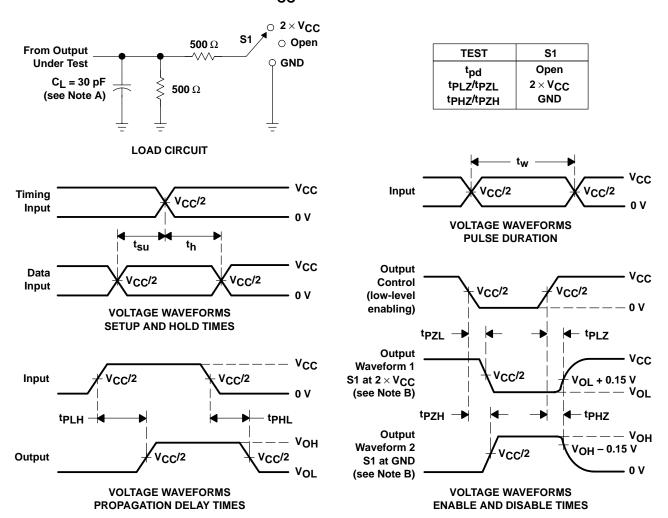
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

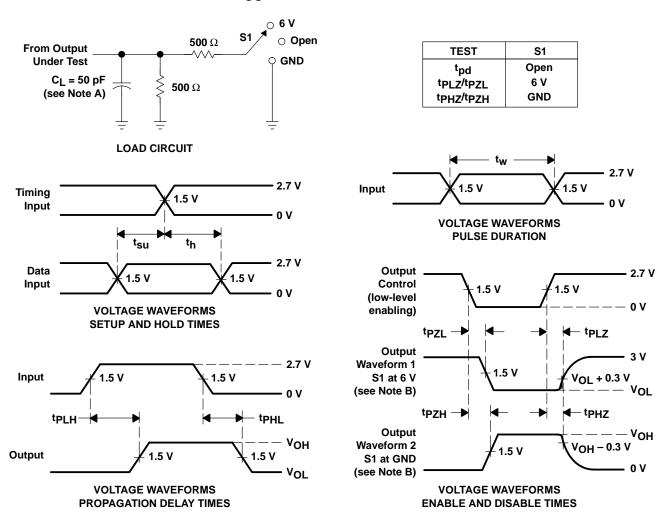


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis-
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

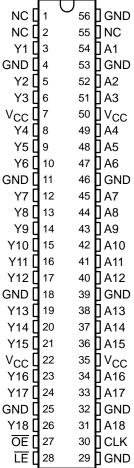
description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

The outputs, which are designed to sink up to 12 mA, include equivalent $26-\Omega$ resistors to reduce overshoot and undershoot.

The SN74ALVC162834 is characterized for operation from -40°C to 85°C.

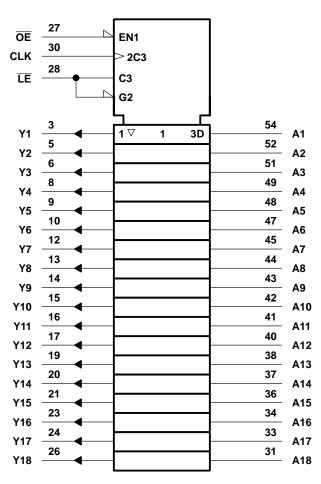
ISTRUMENTS

FUNCTION TABLE

	INP	UTS		OUTPUT
OE	LE	CLK	Α	Υ
Н	Х	Х	Х	Z
L	L	Χ	L	L
L	L	Χ	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	Н	Χ	Y ₀ †
L	Н	L	Χ	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high

logic symbol§

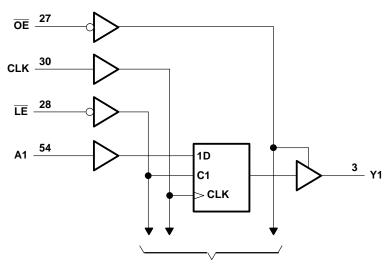


[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)		. -0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
lau	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-6	mA
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low-level output current	V _{CC} = 2.3 V		6	mA
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		8	IIIA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP [†]	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.	2		
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
∨он		Jours 6 mA	2.3 V	1.7			V
		IOH = -6 mA	3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		$I_{OH} = -12 \text{ mA}$	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.4	
VOL		la. 6 mA	2.3 V			0.55	V
		IOL = 6 mA	3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
II		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
Δlcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ
	Control inputs	V. Van or CND	221/		4		~ F
Ci	Data inputs	V _I = V _{CC} or GND	3.3 V	5.5		pF	
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	Pulse duration	LE low		‡		3.3		3.3		3.3		20
t _W	Pulse duration	CLK high or low		‡		3.3		3.3		3.3		ns
		Data before CLK↑		‡		2.1		2.1		1.7		
t _{su}	Setup time	Data hatana LE A	CLK high	‡		2.3		2.3		1.9		ns
		Data before LE ↑	CLK low	‡		1.9		1.9		1.5		
		Data after CLK↑		‡		0.6		0.6		0.7		
t _h	Hold time	Data after <u>LE</u> ↑	CLK high or low	‡		0.8	·	0.8		0.9	·	ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	5.2		5	1	4.2	
t _{pd}	LE	Y		†	1.3	6		6.8	1.3	5.8	ns
·	CLK			†	1.4	6.8		6.1	1.4	5.4	
t _{en}	ŌĒ	Υ		†	1.4	6.3		6.5	1.5	5.9	ns
^t dis	ŌĒ	Y		†	1	4.4		5.2	1.8	5	ns

[†] This information was not available at the time of publication.

switching characteristics from 0° C to 65° C, C_{L} = 50 pF

PARAMETER	FROM	TO	V _{CC} =	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	
	А		1.4	3.9	
t _{pd}	<u>LE</u>	Υ	1.8	5.5	ns
	CLK		1.8	5.2	

operating characteristics, $T_A = 25^{\circ}C$

l	PARAMETER		TEST CO	TEST CONDITIONS V		V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	PARAMETER		TEST CONDITIONS		TYP	TYP	TYP	UNIT	
Ì	C .	Power dissipation	Outputs enabled	C 0	f = 10 MHz	†	38	41	pF
	C _{pd}	capacitance	Outputs disabled	$C_L = 0$,	1 = 10 WIDZ	†	13	15	ρг

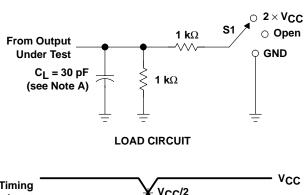
[†] This information was not available at the time of publication.

VCC

0 V

V_{CC}/2

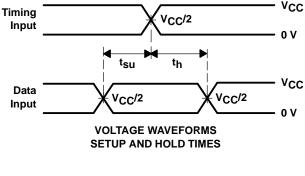
PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V

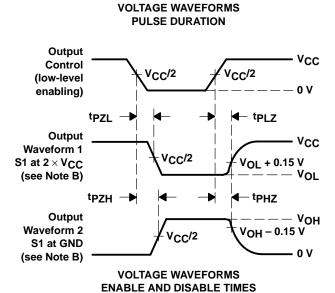


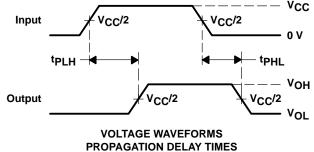
TEST	S 1
t _{pd}	Open
tpLZ/tpZL	2×V _{CC}
tpHZ/tpZH	GND

V_{CC}/2

Input





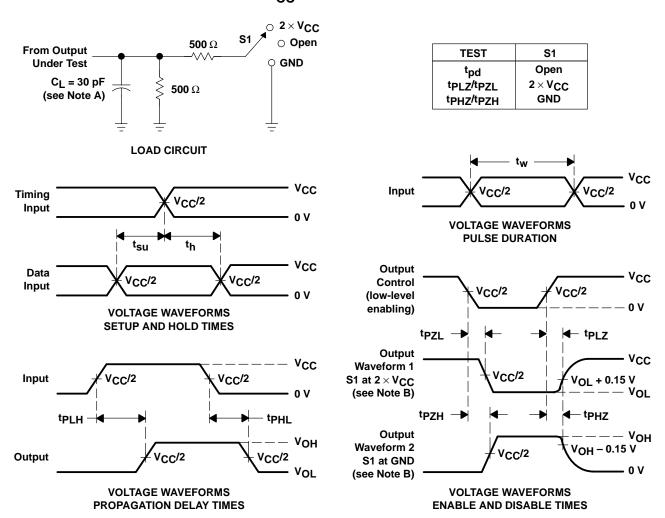


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



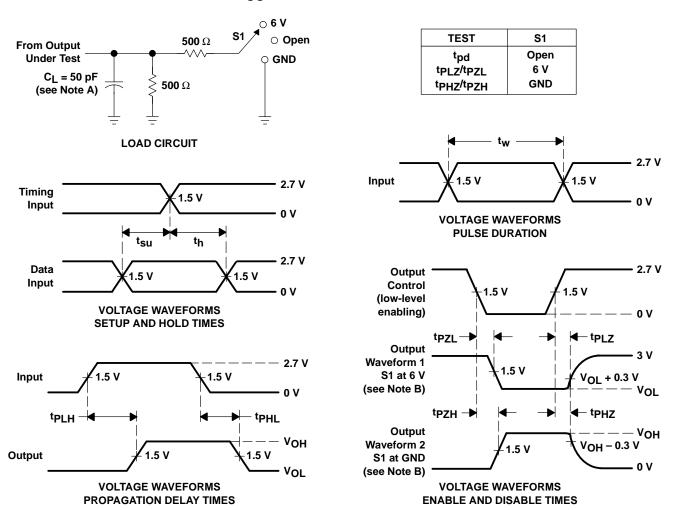
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzI and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Ideal for Use in PC100 Register DIMM Revision 1.1
- Output Port Has Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.



NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The output port includes equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

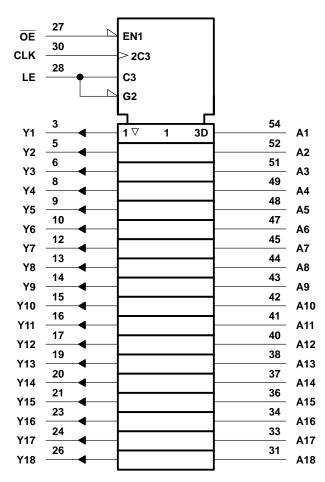
The SN74ALVC162835 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	OUTPUT		
OE	LE	CLK	Α	Y
Н	Х	Х	Χ	Z
L	Н	Χ	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н
L	L	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

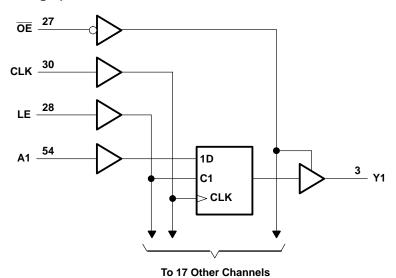
logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
-	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
	Input voltage Output voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
1	High lavel autout august	V _{CC} = 2.3 V		-6	mA
ЮН	nigh-level output current	$V_{CC} = 2.7 \text{ V}$		-8	IIIA
		where I input voltage $ \begin{array}{c} V_{CC} = 1.65 \ V \ to \ 1.95 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.3 \ V \ to \ 1.95 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \ to \ 3.6 \ V \\ V_{CC} = 2.7 \ V \\ V_{CC} = 2.3 \ V \\ V_{CC} = 2.7 \ V \\ V_{CC} = 3 \ V \\ V_{CC} = 2.7 \ V \\ V_{CC} = 3 \ V$	-12		
		V _{CC} = 1.65 V		2	
la.	Low lovel output ourrent	V _{CC} = 2.3 V	6 8		mA
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$			
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2			
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
Voн		lour 6 mA	2.3 V	1.7			V	
		IOH = -6 mA	3 V	2.4				
		$I_{OH} = -8 \text{ mA}$	2.7 V	2				
		$I_{OH} = -12 \text{ mA}$	3 V	2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		$I_{OL} = 2 \text{ mA}$	1.65 V			0.45		
		I _{OL} = 4 mA	2.3 V			0.4	V	
VOL		I _{OL} = 6 mA	2.3 V			0.55		
		IOL = 0 IIIA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6		
		I _{OL} = 12 mA	3 V			0.8		
Ц		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
∆lcc		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	Vi – Voc or CND	221/		3.5		n.E	
Ci	Data inputs	V _I = V _{CC} or GND	3.3 V	5			pF	
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	t _W Pulse duration	LE high		‡		3.3		3.3		3.3		20
ıw.		CLK high or low		CLK high or low ‡	‡		3.3		3.3		3.3	
		Data before CLK↑		‡		2.2		2.1		1.7		
t _{su}	Setup time	Setup time Data before LE↓	CLK high	‡		1.9		1.6		1.5		ns
			CLK low	‡		1.3		1.1		1		
		Data after CLK↑		‡		0.6		0.6		0.7		
t _h	Hold time	Data after LE↓	CLK high or low	‡		1.4		1.7		1.4	·	ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	Α			†	1	5		5	1	4.2	
t _{pd}	LE	Y		†	1.3	5.9		5.8	1.3	5.1	ns
·	CLK			†	1.4	6.3		6.1	1.4	5.4	
t _{en}	ŌĒ	Y		†	1.4	6.3		6.5	1.1	5.5	ns
^t dis	ŌĒ	Y		†	1	4.9		4.9	1.3	4.5	ns

[†] This information was not available at the time of publication.

switching characteristics from 0°C to 85°C, C_L = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(INFOT)	(001F01)	MIN	MAX	
+	А	Υ	0.9	2	ns
t _{pd} +	CLK	Y	1.4	2.9	ns

[‡] Texas Instruments SPICE simulation data

switching characteristics from 0° C to 65° C, $C_L = 50$ pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	
	А	Υ	1	4	ns
^t pd	CLK	Y	1.9	5	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	PARAMETER		1E31 CONDITIONS	TYP	TYP	TYP	ONII
<u> </u>	Power dissipation Outputs enabled		$C_1 = 0$, $f = 10 \text{ MHz}$	†	35.5	40	pF
C _{pd}	capacitance	apacitance Outputs disabled		†	12.5	14	pΓ

[†] This information was not available at the time of publication.



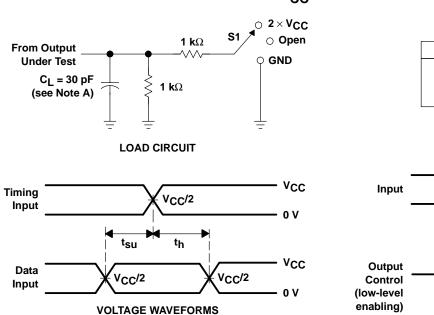
S1

VCC

0 V

V_{CC}/2

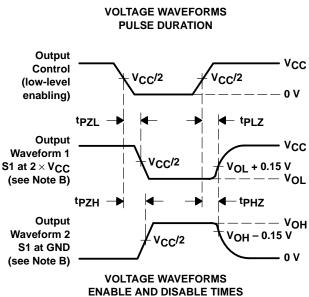
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

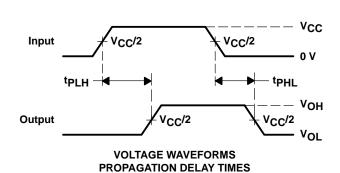




V_{CC}/2

TEST





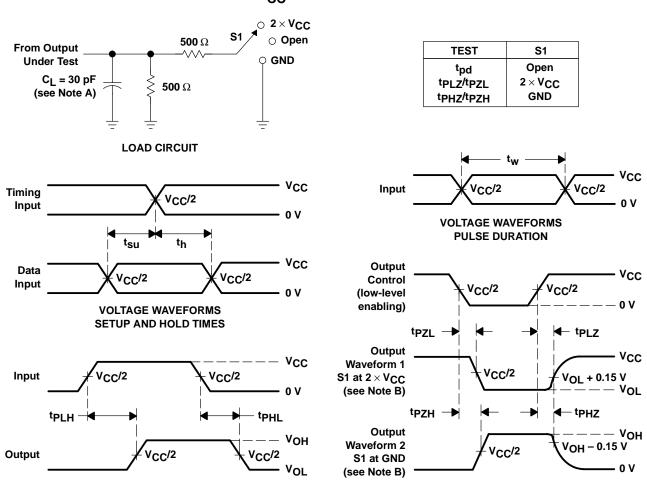
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

VOLTAGE WAVEFORMS

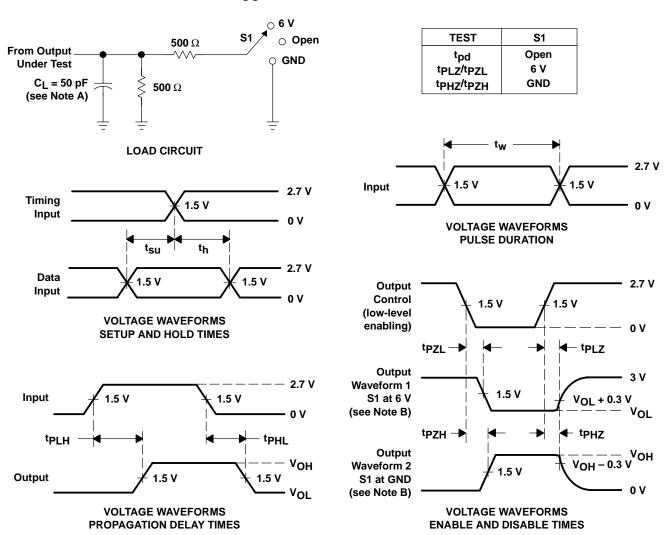
PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpZL and tpZH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

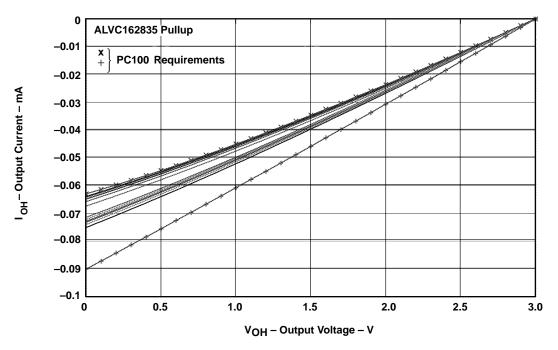


Figure 4. IV Characteristics - Pullup

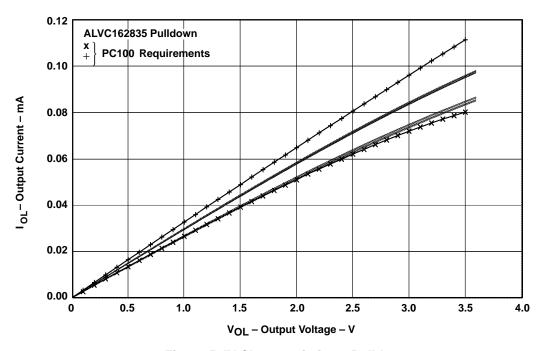


Figure 5. IV Characteristics - Pulldown



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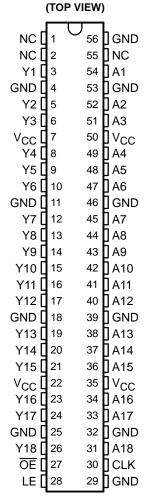
DGG, DGV, OR DL PACKAGE

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Port Has Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.



NC - No internal connection

The output port includes equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162835 is characterized for operation from -40°C to 85°C.

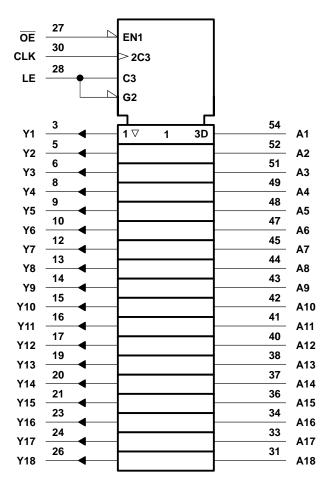


FUNCTION TABLE

	INF	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Χ	Z
L	Н	Χ	L	L
L	Н	X	Н	Н
L	L	\uparrow	L	L
L	L	\uparrow	Н	Н
L	L	L or H	Χ	Y ₀ †

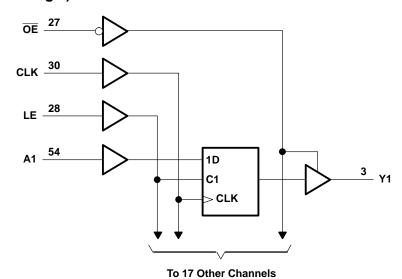
[†] Output level before the indicated steady-state input conditions were established

logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stq}		65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage		0	Vcc	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
1		V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Law level output ourrent	V _{CC} = 2.3 V		6	A	
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP† N	ИАХ	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2		
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
Voн	la 6 mA	2.3 V	1.7			V
	IOH = -6 mA	3 V	2.4			
	$I_{OH} = -8 \text{ mA}$	2.7 V	2			
	$I_{OH} = -12 \text{ mA}$	3 V	2			
	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
	I _{OL} = 2 mA	1.65 V		(0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
VoL	la. 6 mA	2.3 V		(0.55	V
	IOL = 6 mA	3 V		(0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
	I _{OL} = 12 mA	3 V			8.0	
lį	$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ
	V _I = 0.58 V	1.65 V	25			
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
I _I (hold)	V _I = 1.7 V	2.3 V	-45			μΑ
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	- 75			
	$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		<u>+</u>	500	
loz	$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ
ΔlCC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ
Control inputs	VI = Voc or GND	3.3 V		3.5		n.E
C _i Data inputs	$V_I = V_{CC}$ or GND	3.3 v		6		pF
C ₀ Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				VCC =	1.8 V	V _{CC} =		VCC =	$V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$			UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				†		150		150		150	MHz
t Dules duration	t _W Pulse duration	LE high		†		3.3		3.3		3.3		ns
ıw.		CLK high or low		†		3.3		3.3		3.3		115
		Data before CLK↑ Data before LE↓		†		2.2		2.1		1.7		
t _{su}	Setup time		CLK high	†		1.9		1.6		1.5		ns
		Data before LEV	CLK low	†		1.3		1.1		1		
	t _h Hold time	Data after CLK↑		†		0.6		0.6		0.7		
^t h		Data after LE↓	CLK high or low	†		1.4		1.7		1.4		ns

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPOT) (OOTE	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	5		5	1	4.2	
^t pd	LE	Y		†	1.3	5.9		5.8	1.3	5.1	ns
·	CLK			†	1.4	6.3		6.1	1.4	5.4	
t _{en}	ŌĒ	Y		†	1.4	6.3		6.5	1.1	5.5	ns
^t dis	ŌĒ	Y		†	1	4.7		4.9	1.3	4.5	ns

[†] This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	3.3 V 5 V	UNIT
	(1141 01)	(8811 81)	MIN	MAX	
^t pd	CLK	Y	1.9	5	ns

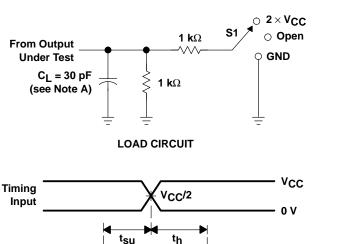
operating characteristics, T_A = 25°C

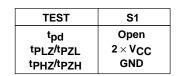
PARAMETER Outputs analysis		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT		
		TEST CONDITIONS	TYP	TYP	TYP	UNIT		
<u> </u>	Power dissipation	Outputs enabled	C ₁ = 0. f = 10 MHz	†	36	41	ρF	
Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	12.5	14	pr	

[†] This information was not available at the time of publication.

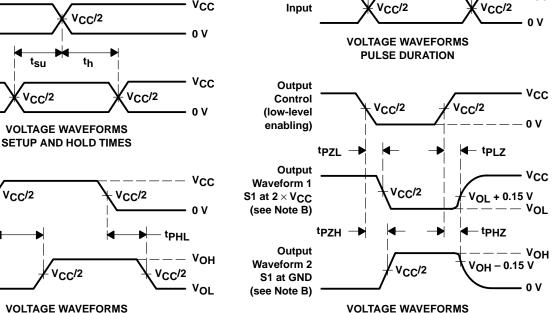
VCC

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





ENABLE AND DISABLE TIMES



NOTES: A. C_L includes probe and jig capacitance.

V_{CC}/2

Data

Input

Input

Output

t_{PLH}

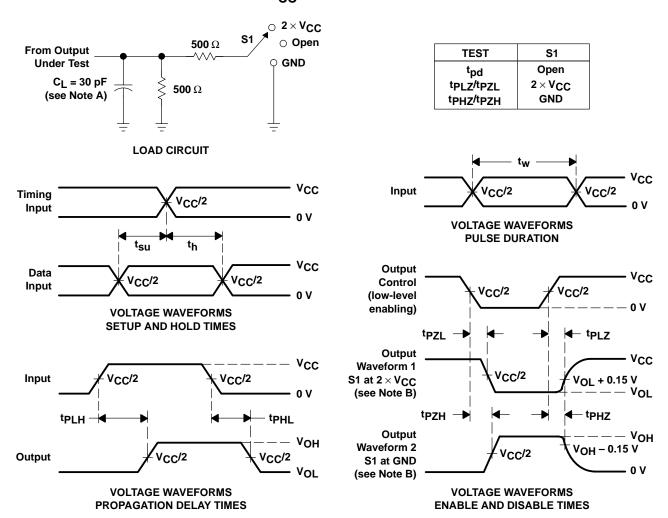
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

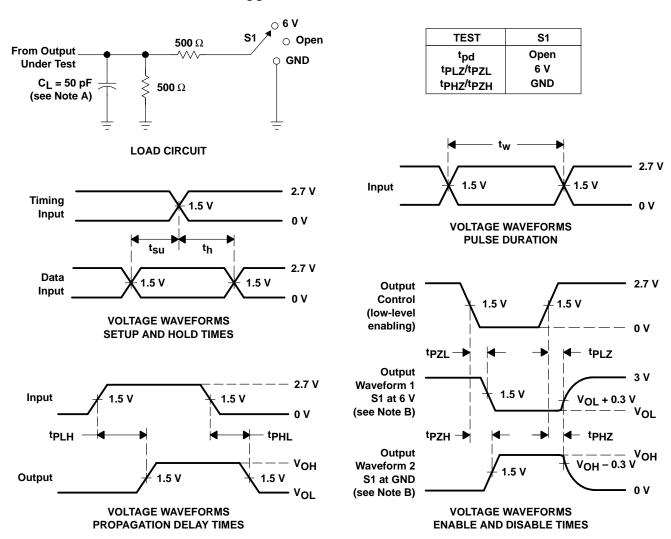


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Port Has Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **Designed to Comply With JEDEC 168-Pin** and 200-Pin SDRAM Buffered DIMM **Specification**
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 20-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

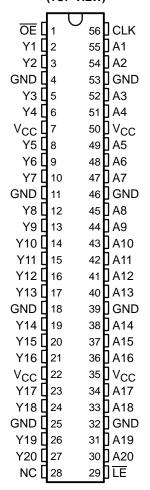
Data flow from A to Y is controlled by the output-enable (OE) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When LE is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

The output port includes equivalent $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC162836 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



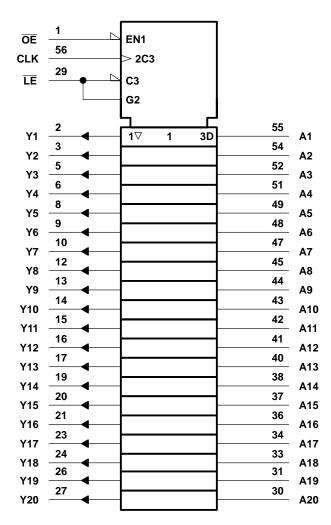
NC - No internal connection

FUNCTION TABLE

	INF	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Χ	Z
L	L	Χ	L	L
L	L	Χ	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

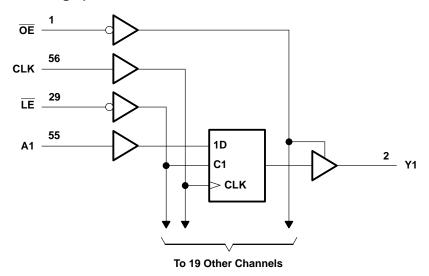
logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		-0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)		$' \text{ to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$		–50 mA
Output clamp current, IOK (VO < 0)		–50 mA
Continuous output current, IO		±50 mA
Continuous current through each V _{CC} or GND .		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	٧	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	Vcc	V	
		V _{CC} = 1.65 V		-2		
1		V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
1	Law lavel output ourrent	V _{CC} = 2.3 V	6 8		mA	
IOL	Low-level output current	V _{CC} = 2.7 V				
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER	TEST CONDITIONS	vcc	MIN	TYP [†]	MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2	2			
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
∨он		lour 6 mA	2.3 V	1.7			V	
		IOH = -6 mA	3 V	2.4				
		$I_{OH} = -8 \text{ mA}$	2.7 V	2				
		$I_{OH} = -12 \text{ mA}$	3 V	2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2		
		$I_{OL} = 2 \text{ mA}$	1.65 V			0.45	V	
		I _{OL} = 4 mA	2.3 V			0.4		
VOL		I _{OL} = 6 mA	2.3 V			0.55		
		IOL = 0 IIIA	3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6		
		I _{OL} = 12 mA	3 V			0.8		
Ц		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
loz		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
Δlcc		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	Vi – Voc or CND	221/		5		n.E	
Ci	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		5.5		pF	
Со	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				V _{CC} =	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				‡		150		150		150	MHz
	Pulse duration	LE low		‡		3.3		3.3		3.3		no
t _W	CLK high or low			‡		3.3		3.3		3.3		ns
		Data before CLK↑		‡		1.4		1.7		1.5		
t _{su}	Setup time	Data haɗana LE ↑	CLK high	‡		1.2		1.6		1.3		ns
		Data before LE ↑	CLK low	‡		1.4		1.5		1.2		
		Data after CLK↑		‡		0.9		0.9		0.9		
th	Hold time	Data after LE ↑	CLK high or low	‡		1.1		1.1		1.1		ns

[‡] This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(IIII O1)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	А			†	1	4.4		4.6	1.2	4	
t _{pd}	LE	Y		†	1.1	5.8		6.1	1.4	5.1	ns
	CLK			†	1	5.2		5.5	1.1	5	
t _{en}	ŌĒ	Y		†	1.1	6.4		6.5	1.2	5.5	ns
^t dis	ŌĒ	Y		†	1	4.7		5.2	1.7	5.1	ns

[†] This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(INFOT)	(001F01)	MIN	MAX	
	A	Y	1	4	ns
^t pd	CLK	Y	1.7	4.5	ns

operating characteristics, $T_A = 25^{\circ}C$

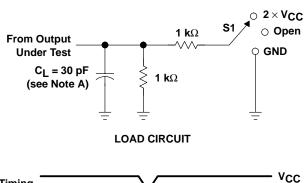
Ī	PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				1E31 CONDITIONS	TYP	TYP	TYP	UNIT
ſ	<u> </u>	C Power dissipation Outp		C ₁ = 0. f = 10 MHz	†	31	36	ρF
	Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	7	11	ρг

[†] This information was not available at the time of publication.

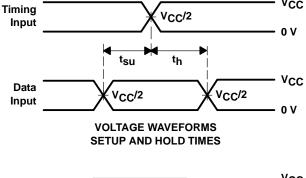
VCC

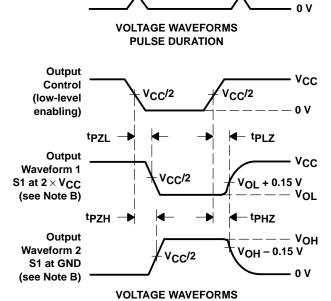
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

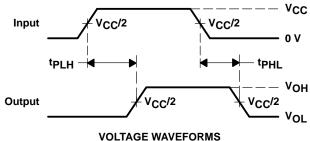




ENABLE AND DISABLE TIMES

V_{CC}/2

Input

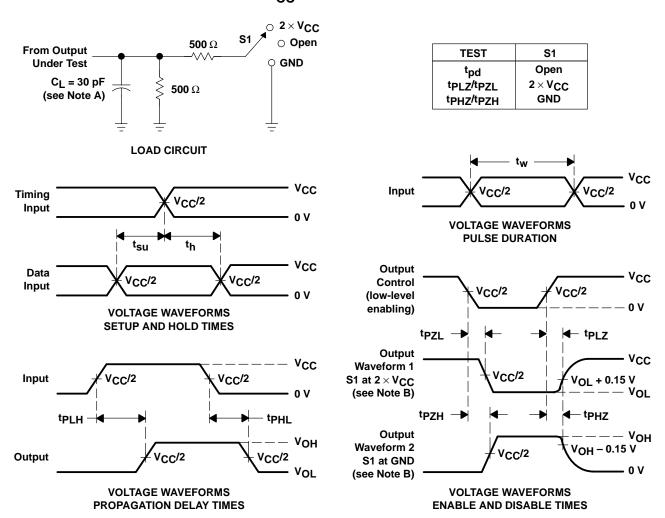


PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

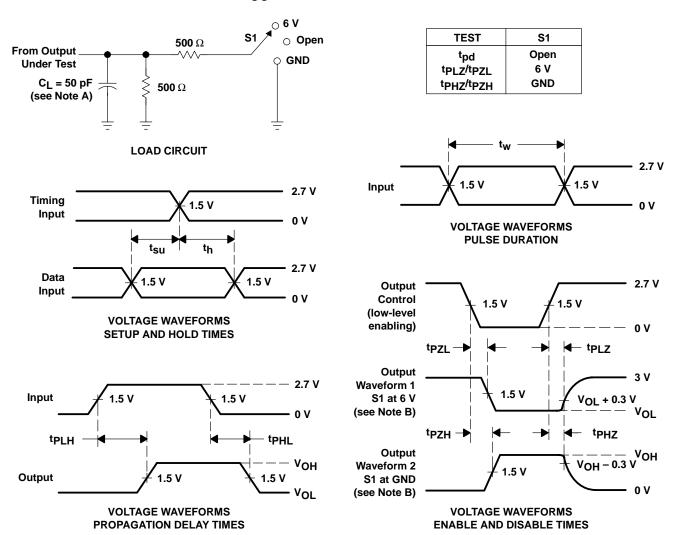


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns, $t_{f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Port Has Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- **Designed to Comply With JEDEC 168-Pin** and 200-Pin SDRAM Buffered DIMM Specification
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown **Resistors**
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

description

This 20-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

The output port includes equivalent 26- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162836 is characterized for operation from -40°C to 85°C.

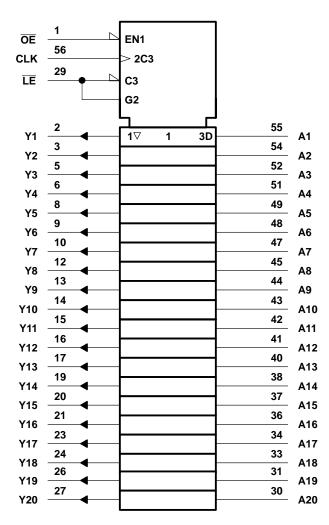
ISTRUMENTS

FUNCTION TABLE

	INP	PUTS		OUTPUT
OE	LE	CLK	Α	Y
Н	Х	Х	Χ	Z
L	L	Χ	L	L
L	L	X	Н	Н
L	Н	\uparrow	L	L
L	Н	\uparrow	Н	Н
L	Н	L or H	Χ	Y ₀ †

[†] Output level before the indicated steady-state input conditions were established

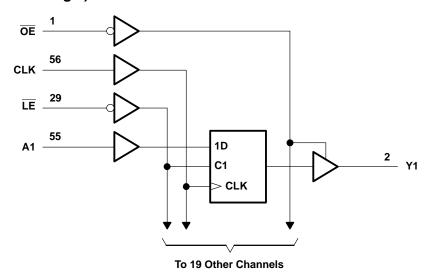
logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	—50 mA
Output clamp current, I _{OK} (V _O < 0)	−50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): Do	GG package 81°C/W
DO	GV package 86°C/W
DI	L package
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
		V _{CC} = 1.65 V		-2	
lou	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-6	mA
IOH	High-level output current	$V_{CC} = 2.7 \text{ V}$		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
la.	Low lovel output ourrent	V _{CC} = 2.3 V		6	mA
lOL	Low-level output current	V _{CC} = 2.7 V		8	IIIA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP [†] MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} -0.2	2	
	$I_{OH} = -2 \text{ mA}$	1.65 V	1.2]
	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9		1
Voн	la C mA	2.3 V	1.7		V
	IOH = -6 mA	3 V	2.4		1
	$I_{OH} = -8 \text{ mA}$	2.7 V	2		
	$I_{OH} = -12 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
	I _{OL} = 2 mA	1.65 V		0.45	
	I _{OL} = 4 mA	2.3 V		0.4	
VoL	la. 6 mA	2.3 V		0.55	V
	IOL = 6 mA	3 V		0.55	
	I _{OL} = 8 mA	2.7 V		0.6	
	I _{OL} = 12 mA	3 V		0.8]
II	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
	V _I = 0.58 V	1.65 V	25		
	V _I = 1.07 V	1.65 V	-25		
	$V_{I} = 0.7 \text{ V}$	2.3 V	45		
II(hold)	V _I = 1.7 V	2.3 V	-45		μΑ
	V _I = 0.8 V	3 V	75		
	V _I = 2 V	3 V	-75		
	$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$	3.6 V		±500	
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ
ΔlCC	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μΑ
Control inputs	V _I = V _{CC} or GND	3.3 V		5.5	pF
Data inputs		3.5 v		6	Pi
C _O Outputs	$V_O = V_{CC}$ or GND	3.3 V		8	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

				$V_{CC} = 1.8 \text{ V}$ $V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency				†		150		150		150	MHz
	Pulse duration	LE low		†		3.3		3.3		3.3		ns
t _W	Puise duration	CLK high or low		†		3.3		3.3		3.3		115
		Data before CLK↑		†		1.4		1.7		1.5		
t _{su}	Setup time	- · · · · · · ·	CLK high	†		1.2		1.6		1.3		ns
		Data before <u>LE</u> ↑	CLK low	†		1.4		1.5		1.2		
	Data after CLK↑			†		0.9		0.9		0.9		
th	Hold time	Data after <u>LE</u> ↑	CLK high or low	†		1.1		1.1		1.1		ns

[†] This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM TO (INPUT) (OUTPUT)		V _{CC} = 1.8 V V _{CC} = ± 0		V _{CC} =	V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141 01)	(0011 01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
	Α			†	1	4.4		4.6	1.2	4	
t _{pd}	LE	Y		†	1.1	5.8		6.1	1.4	5.1	ns
·	CLK			†	1	5.2		5.5	1.1	5	
t _{en}	ŌĒ	Υ		†	1.1	6.4		6.5	1.2	5.5	ns
^t dis	ŌĒ	Υ		†	1	4.7		5.2	1.7	5.1	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
	FARAMETER	1E31 CONDITIONS	TYP	TYP	TYP	ONII	
<u> </u>	Power dissipation	Outputs enabled	$C_1 = 0$, $f = 10 \text{ MHz}$	†	31.5	36	PF
Cpd	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	†	8	10.5	l ht

[†] This information was not available at the time of publication.

S1

Open

2×VCC

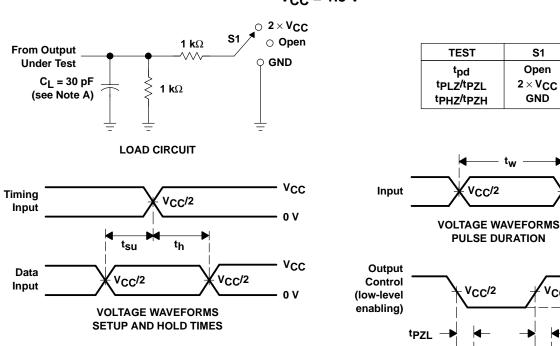
GND

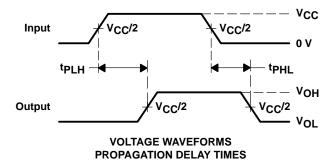
VCC

0 V

V_{CC}/2

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 V$





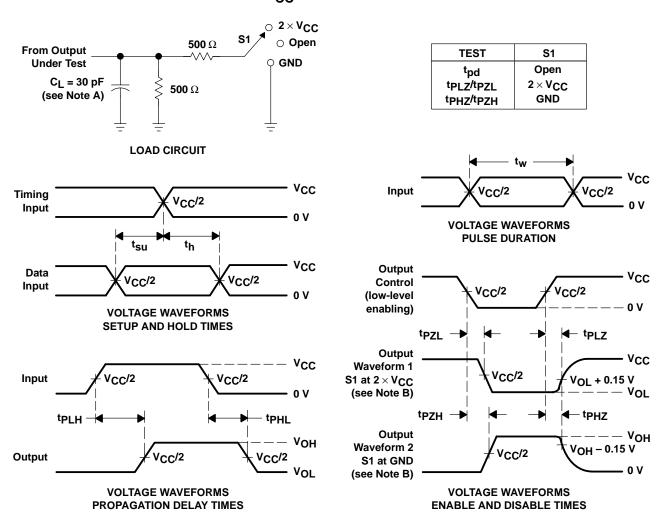
VCC V_{CC}/2 CC/2 0 V - tpLZ Output VCC Waveform 1 V_{CC}/2 S1 at $2 \times V_{CC}$ V_{OL} + 0.15 V - Vol (see Note B) - tPHZ tPZH -Output - Voh Waveform 2 V_{OH} – 0.15 V S1 at GND - 0 V (see Note B) **VOLTAGE WAVEFORMS**

ENABLE AND DISABLE TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

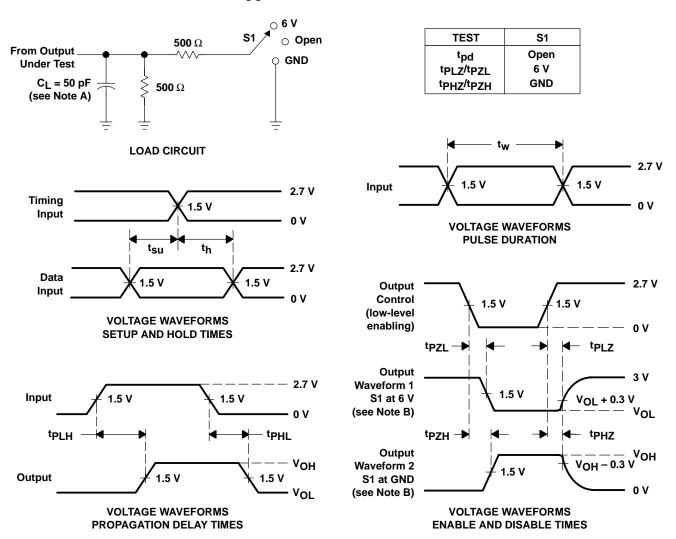


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

SN74ALVCH162841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

SCES088C - OCTOBER 1996 - REVISED FEBRUARY 1999

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH162841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has

noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OE does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

56 1LE 10E 55 1D1 1Q1 42 54 🛭 1D2 1Q2 📙 3 53 GND GND 4 52 1D3 1Q3 🛮 5 51 1D4 1Q4 **[**] 6 50 V_{CC} V_{CC} ∐ 7 1Q5 🛮 8 49 1 1D5 1Q6 **[**] 9 48 🛮 1D6 47 1D7 1Q7 L 10 46 [] GND GND 4 11 45 **1** 1D8 1Q8 **[**] 12 44 🛮 1D9 1Q9 🛮 13 1Q10 🛮 14 43 1D10 2Q1 L 15 42 2D1 2Q2 📙 16 41 2D2 2Q3 17 40 2D3 GND 18 39 GND 38 🛮 2D4 2Q4 📙 19 37 2D5 2Q5 4 20 2Q6 21 36 2D6 V_{CC} 422 35 🛮 V_{CC} 2Q7 23 34 🛮 2D7 208 24 33 L 2D8 32 GND GND L 25 31 2D9 2Q9 🛮 26 2Q10 L 27 30 L 2D10 29 🛮 2LE 2OE 4 28

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description (continued)

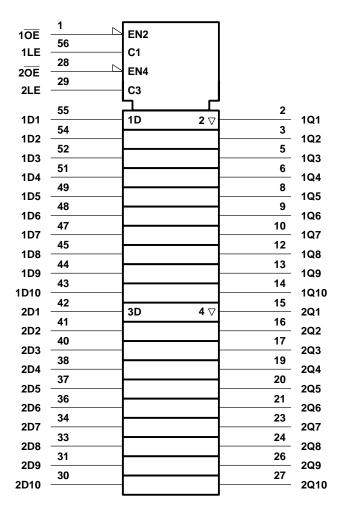
Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH162841 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 10-bit latch)

	INPUTS	ОИТРИТ	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q_0
Н	X	Χ	Z

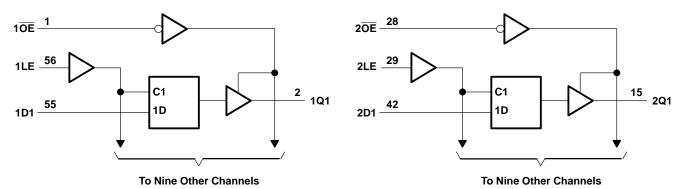
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	0 = 1/4 4 0 1/
Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V_{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{sto}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	٧	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-2		
1	High level output ourrent	V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	V _{CC} = 2.7 V		-8	IIIA	
		V _{CC} = 3 V		-12		
		V _{CC} = 1.65 V		2		
I _{OL} L	Low-level output current	$V_{CC} = 2.3 \text{ V}$		6	mA	
		$V_{CC} = 2.7 \text{ V}$		8		
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			VCC	IVIIIV	TYP [†]	MAX	UNIT		
I _{OH} = -100 μA			1.65 V to 3.6 V	V _{CC} -0.	2				
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2				
		I _{OH} = -4 mA	2.3 V	1.9					
Voн	VOH	la 6 mA		2.3 V	1.7			V	
		I _{OH} = -6 mA		3 V	2.4				
		I _{OH} = -8 mA		2.7 V	2				
		I _{OH} = -12 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 2 mA		1.65 V			0.45		
		I _{OL} = 4 mA		2.3 V			0.4		
VOL		I _{OL} = 6 mA		2.3 V			0.55	V	
				3 V			0.55		
		I _{OL} = 8 mA	2.7 V			0.6			
		I _{OL} = 12 mA	3 V			0.8			
Ιį		V _I = V _{CC} or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		V _I = 0.7 V		2.3 V	45				
^I I(hold)		V _I = 1.7 V		2.3 V	-45			μΑ	
		V _I = 0.8 V		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_{I} = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$		3.6 V			±500		
loz		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Cont	trol inputs			221/		4.5		n.E	
C _i Data	a inputs			3.3 V		6.5		pF	
C _O Outp	outs	$V_O = V_{CC}$ or GND		3.3 V		7		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER		PARAMETER V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↑	§		0.9		0.7		1.1		ns
t _h	Hold time, data after LE↑	§		1.2		1.5		1.1		ns

[§] This information was not available at the time of publication.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} =	2.5 V 2 V	VCC =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(1141 01)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	†	1	5.3		5.2	1.2	4.3	20
^t pd	LE	ζ	†	1	5.9		5.6	1	4.7	ns
t _{en}	ŌĒ	Q	†	1	6.5		6.5	1	5.3	ns
^t dis	ŌĒ	Q	†	1.1	5.6		4.9	1.3	4.4	ns

[†] This information was not available at the time of publication.

operating characteristics, T_A = 25°C

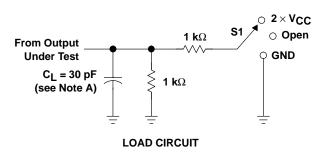
PARAMETER			TEST CONDI	PIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
TAKAMETEK		TEST CONDITIONS		TYP	TYP	TYP	ONIT	
<u> </u>	Power dissipation	Outputs enabled	C: 0		†	24	27	PΓ
Cpd	capacitance	Outputs disabled	$C_L = 0,$ f =	= 10 MHz	†	2	2	þr

[†] This information was not available at the time of publication.

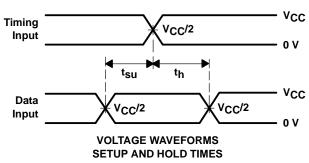
VCC

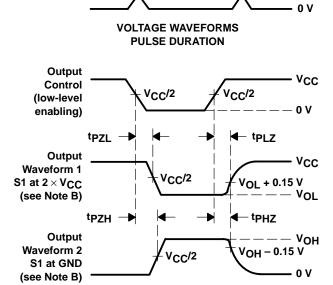
V_{CC}/2

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



TEST	S 1
t _{pd}	Open
tPLZ/tPZL	2×V _{CC}
tPHZ/tPZH	GND



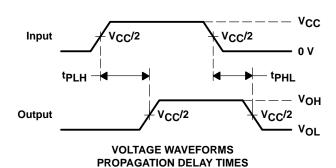


VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

V_{CC}/2

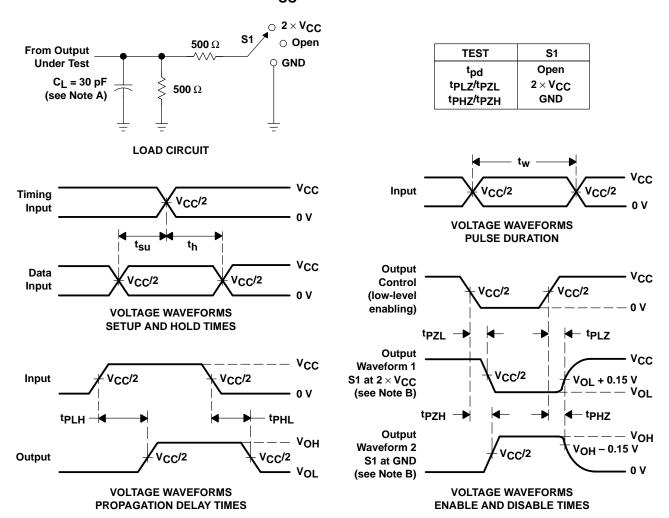
Input



- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

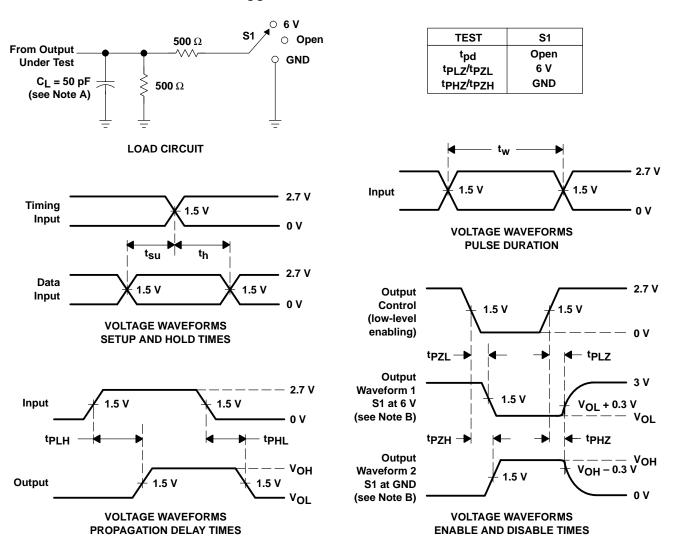


- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

General Information	1
ALVC Gates/Octals	2
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DGG OR DL PACKAGE

(TOP VIEW)

- **Member of the Texas Instruments** Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink **Small-Outline (DGG) Packages**

description

16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} , which is set at 5 V, and A port has V_{CCA}, which is set to operate at 3.3 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses.

To ensure the high-impedance state during power up or power down, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC164245 is characterized for operation from -40°C to 85°C.

48 10E 1DIR L 1B1 🛮 2 47 🛮 1A1 1B2 🛮 3 46 1 1A2 GND 🛮 4 45 GND 1B3 🛮 5 44 🛮 1A3 1B4 🛮 6 43 🛮 1A4 42 V_{CCA} (3.3 V) (5 V) V_{CCB} L 1B5 📙 8 41 1 1A5 1B6 🛮 9 40 1 1A6 39 GND GND 🛚 10 1B7 38 🛮 1A7 11 1B8 [] 37 L 1A8 12 36 2A1 2B1 🛛 13 2B2 [35 2A2 14 GND [15 34 | GND 2B3 🛮 33 D 2A3 16 17 32 2A4 2B4 L (5 V) V_{CCB} L 31 V_{CCA} (3.3 V) 18 2B5 [] 19 30 2A5 29 2A6 2B6 20 GND 21 28 GND 2B7 22 27 2A7 2B8 🛮 23 26 2A8 2DIR 24 25 20E

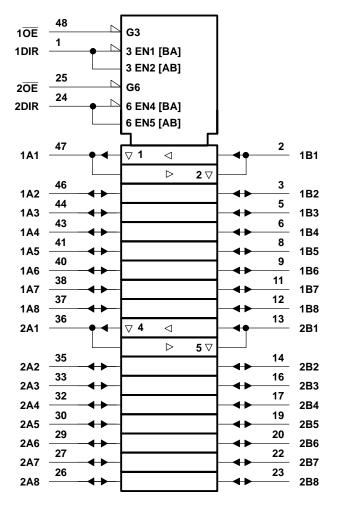
FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION	
OE	DIR	OPERATION	
L	L	B data to A bus	
L	Н	A data to B bus	
Н	X	Isolation	

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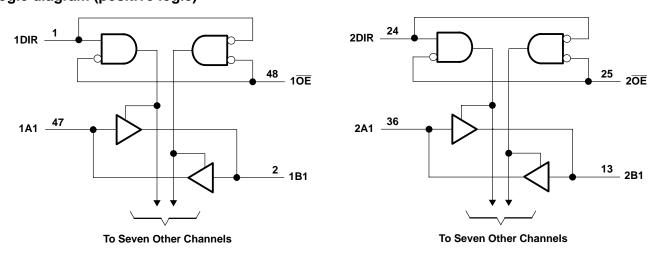
SCAS416F - MARCH 1994 - REVISED FEBRUARY 1999

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)[†]

Supply voltage range: V _{CCA}	–0.5 V to 4.6 V
V _{CCB}	–0.5 V to 6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	–0.5 V to 6 V
I/O port A (see Note 2)	$-0.5 \text{ V to V}_{CCA} + 0.5 \text{ V}$
I/O port B (see Note 1)	$-0.5 \text{ V to V}_{CCB} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{Stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 6 V maximum.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions for V_{CCB} at 5 V (see Note 4)

		MIN	MAX	UNIT
VCCB	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
VIA	Input voltage	0	VCCB	V
V _{OB}	Output voltage	0	V _{CCB}	V
IOH	High-level output current		-24	mA
loL	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate		10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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recommended operating conditions for V_{CCA} at 3.3 V (see Note 4)

		MIN	MAX	UNIT
VCCA	Supply voltage	2.7	3.6	V
VIH	High-level input voltage $V_{CCA} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
V _{IL}	Low-level input voltage $V_{CCA} = 2.7 \text{ V to } 3.6 \text{ V}$		8.0	V
V _{IB}	Input voltage	0	VCCA	V
VOA	Output voltage	0	VCCA	V
lou	High-level output current		-12	mA
IOH	V _{CCA} = 3 V		-24	ША
lou	Low-level output current		12	mA
lOL	V _{CCA} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 5 V (unless otherwise noted) (see Note 5)

PAI	RAMETER	TEST CONDITIONS	VCCB	MIN	TYP [†]	MAX	UNIT
		100 40	4.5 V	4.3			
\/ (A	to D\	$I_{OH} = -100 \mu\text{A}$	5.5 V	5.3			v
V _{OH} (A	. Ю Б)	Jan. 24 mA	4.5 V	3.7			V
		IOH = -24 mA	5.5 V	4.7			
		In. 100 vA	4.5 V			0.2	
\/ /A	to D)	I _{OL} = 100 μA	5.5 V			0.2	V
V _{OL} (A	Ю Б)	Jan. 24 mA	4.5 V			0.55	
		I _{OL} = 24 mA	5.5 V			0.55	
lį	Control inputs	V _I = V _{CCB} or GND	5.5 V			±5	μΑ
loz [‡]	A or B ports	$V_O = V_{CCB}$ or GND	5.5 V			±10	μΑ
Icc		$V_I = V_{CCB}$ or GND, $I_O = 0$	5.5 V			40	μΑ
Δlcc§		One input at 3.4 V, Other inputs at V _{CCB} or GND	4.5 V to 5.5 V			750	μΑ
Ci	Control inputs	V _I = V _{CCB} or GND	5 V		6.5		pF
C _{io}	A or B ports	$V_O = V_{CCB}$ or GND	5 V		6.5		pF

[†] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: V_{CCA} = 2.7 V to 3.6 V



For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated VCC.

SCAS416F - MARCH 1994 - REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 3.3 \text{ V}$ (unless otherwise noted) (see Note 6)

PA	RAMETER	TEST CONDITIONS	VCCA	MIN TYP	MAX	UNIT	
		$I_{OH} = -100 \mu A$	2.7 V to 3.6 V	V _{CC} -0.2			
\/\0/5	2 to 1	Jour 12 mA	2.7 V	2.2		V	
VOH (E	5 (0 A)	IOH = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	2.7 V to 3.6 V		0.2		
V _{OL} (E	3 to A)	I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
IĮ	Control inputs	$V_I = V_{CCA}$ or GND	3.6 V		±5	μΑ	
loz [‡]		$V_O = V_{CCA}$ or GND	3.6 V		±10	μΑ	
Icc		$V_I = V_{CCA}$ or GND, $I_O = 0$	3.6 V		40	μΑ	
Δlcc§		One input at V _{CCA} – 0.6 V, Other inputs at V _{CCA} or GND	3 V to 3.6 V		750	μΑ	
Ci	Control inputs	V _I = V _{CCA} or GND	3.3 V	6.5	;	pF	
C _{io}	A or B ports	V _O = V _{CCA} or GND	3.3 V	8.8	;	pF	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

	V _{CCB} = 5		$V \pm 0.5$	٧		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCA} = 2.7 V	VCCA ± 0.	= 3.3 V 3 V	ns
			MIN MAX¶	PNIM	MAX¶	
+ .	А	В	5.9	1	5.8	nc
^t pd	В	Α	6.7	1.2	5.8	
t _{en}	ŌĒ	В	9.3	1	8.9	ns
^t dis	ŌĒ	В	9.2	2.1	9.5	ns
^t en	ŌĒ	А	10.2	2	9.1	ns
^t dis	ŌĒ	А	9	2.9	8.6	ns

[¶] This limit can vary among suppliers.

operating characteristics, T_A = 25°C

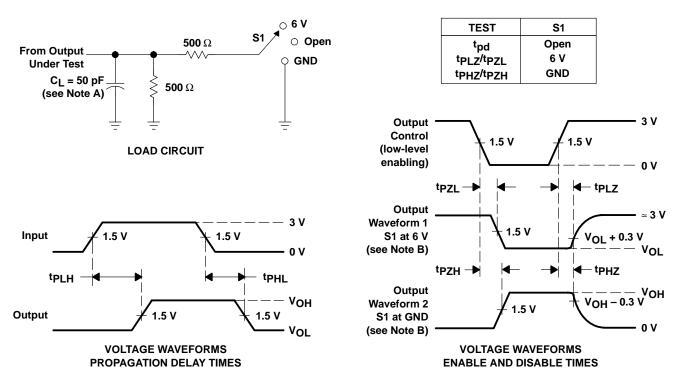
PARAMETER		TEST CONDITIONS	V _{CCA} = 3.3 V V _{CCB} = 5 V	UNIT	
<u> </u>	Power dissipation capacitance	Outputs enabled (A or B)	Cı = 50 pF. f = 10 MH;	56	pF
Cpd	rowei dissipation capacitance	Outputs disabled (A or B)	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	6	PF

[†] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. ‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated VCC. NOTE 6: $V_{CCB} = 5 V \pm 0.5 V$

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PARAMETER MEASUREMENT INFORMATION V_{CCA} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

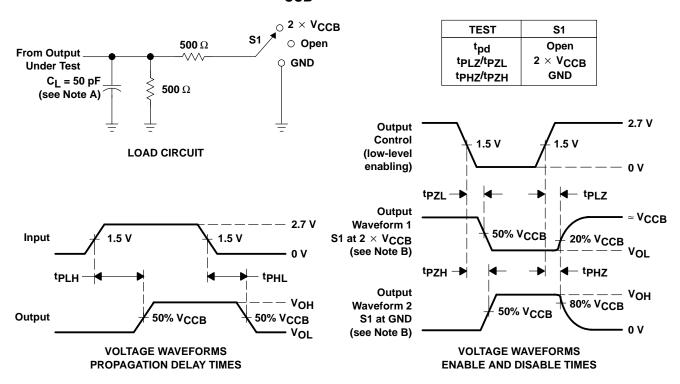
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCAS416F - MARCH 1994 - REVISED FEBRUARY 1999

PARAMETER MEASUREMENT INFORMATION $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$



- OTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

General Information	1
ALVC Gates/Octals	2
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SN74SSTL16837A 20-BIT SSTL_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCBS675G - SEPTEMBER 1996 - REVISED SEPTEMBER 1998

- **Member of the Texas Instruments** Widebus™ Family
- Supports SSTL_3 Signal Inputs and **Outputs**
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL 3 Class I and Class II **Specifications**
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

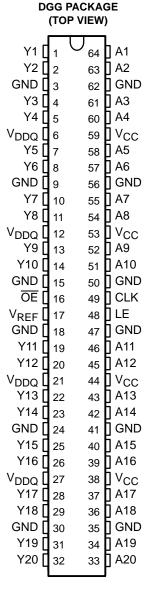
description

This 20-bit universal bus driver is designed for 3-V to 3.6-V V_{CC} operation and SSTL_3 or LVTTL I/O levels.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when latch enable (LE) is high. The A data is latched if LE is low and clock (CLK) is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When OE is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16837A is characterized for operation from 0°C to 70°C.



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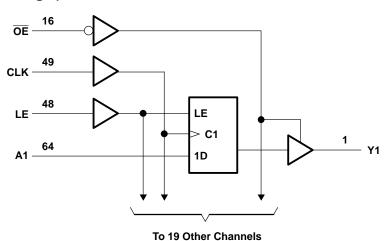
SCBS675G - SEPTEMBER 1996 - REVISED SEPTEMBER 1998

FUNCTION TABLE

	INP	OUTPUT		
OE	LE	CLK	Α	Υ
L	Н	Х	Н	Н
L	Н	Χ	L	L
L	L	\uparrow	Н	Н
L	L	\uparrow	L	L
L	L	Н	Χ	Y ₀ †
L	L	L	Χ	Y ₀ † Y ₀ ‡ Z
Н	Χ	X	Χ	Z

[†] Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC} or V _{DDQ}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	\dots -0.5 V to V _{DDQ} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	73°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{DDQ}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



[‡] Output level before the indicated steady-state input conditions were established

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recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		V _{DDQ}		3.6	V
V _{DDQ}	Output supply voltage		3		3.6	V
VREF	Reference voltage ($V_{REF} = 0.45 \times V_{DDQ}$)		1.3	1.5	1.7	V
VTT	Termination voltage ($V_{REF} = V_{TT} = 0.45 \times V_{I}$	ODQ)	V _{REF} -50mV	V _{REF}	V _{REF} +50mV	V
VI	Input voltage		0		VCC	V
VIH	AC high-level input voltage	All inputs	V _{REF} +400mV			V
VIL	AC low-level input voltage	All inputs			V _{REF} -400mV	V
VIH	DC high-level input voltage	All inputs	V _{REF} +200mV			V
VIL	DC low-level input voltage	All inputs			V _{REF} -200mV	V
ІОН	High-level output current				-20	mΛ
loL	Low-level output current				20	mA
TA	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST C	ONDITIONS	v _{cc}	MIN	TYP [†]	MAX	UNIT	
VIK		I _I = -18 mA		3 V			-1.2	V	
		I _{OH} = -100 μA		3 V to 3.6 V	V _{CC} -0.	2			
۷он		$I_{OH} = -16 \text{ mA}$		3 V	2.2			V	
		I _{OH} = -20 mA] 3 v	2.1				
		I _{OL} = 100 μA		3 V to 3.6 V			0.2		
VOL		I _{OL} = 16 mA		3 V			0.5	V	
		I _{OL} = 20 mA] 3 v			0.55		
	LE	V _I = 2.1 V or 0.9 V	V _{REF} = 1.3 V or 1.7 V	3.6 V			±40	μΑ	
		$V_{I} = 3.6 \text{ V or } 0$	VREF = 1.5 V 01 1.7 V	3.6 V			±1.2	mA	
	Data inputs, OE	V _I = 2.1 V or 0.9 V	V _{REF} = 1.3 V or 1.7 V	3.6 V			±5		
lį		V _I = 3.6 V or 0					±5	μΑ	
	CLK	V _I = 2.1 V or 0.9 V	V _{REF} = 1.3 V or 1.7 V	3.6 V			±150		
	CLK	V _I = 3.6 V or 0	VREF = 1.3 V 01 1.7 V				±4	mA	
	VREF	V _{REF} = 1.3 V or 1.7 V		3.6 V			±150	μΑ	
loz		V _O = 0.9 V or 2.1 V		3.6 V			±10	μΑ	
loz		$V_0 = 0 \text{ or } 3.6 \text{ V}$		3.0 V			±10	μΑ	
Icc		$V_I = 2.1 \text{ V or } 0.9 \text{ V}$	I _O = 0	3.6 V			90	mA	
icc		V _I = 3.6 V or 0	10 = 0	3.0 V			90] ""^	
Ci	Control inputs	V ₁ = 2.1 V or 0.9 V		3.3 V		2.5		pF	
9	A port	V = 2.1 V OI 0.9 V	V _I = 2.1 V or 0.9 V			2		ÞΓ	
Со	Y port	V _O = 2.1 V or 0.9 V		3.3 V		3	·	pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

SN74SSTL16837A 20-BIT SSTL_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCBS675G - SEPTEMBER 1996 - REVISED SEPTEMBER 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

					V _{CC} = 3.3 V ± 0.3 V	
				MIN	MAX	
f _{clock} Clock frequency					200	MHz
	t _w Pulse duration	LE high		2.5		20
t _W	ruise duration	CLK high or low		2.5		ns
		A before CLK↑	LE low	1.5		
t _{su}	Setup time	A before LE↓	CLK high	1.5		ns
		A pelote LE	CLK low	2		
+.	Hold time	A after CLK↑ LE low		1		no
^t h	noia titie	A after LE↓		1		ns

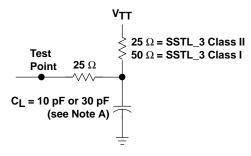
switching characteristics over recommended operating free-air temperature range, Class I, $V_{REF} = V_{TT} = V_{DDQ} \times 0.45$ and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	
f _{max}			200		MHz
	А		1.1	4	
^t pd	LE	Υ	1.5	4.1	ns
· ·	CLK		1	3	
t _{en}	ŌĒ	Y	1.8	5.5	ns
^t dis	ŌĒ	Y	1.8	6	ns

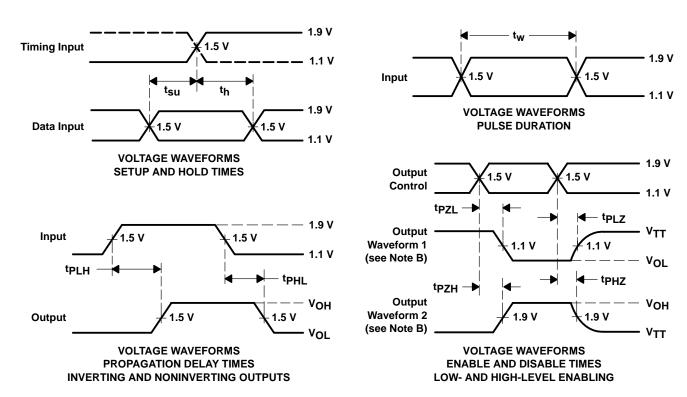
switching characteristics over recommended operating free-air temperature range, Class II, $V_{REF} = V_{TT} = V_{DDQ} X$ 0.45 and $C_L = 30 \ pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	UNIT	
	(INPOT)	(001701)	MIN	MAX	
f _{max}			200		MHz
	А		1.1	4.2	
t _{pd}	LE	Υ	1.5	4.3	ns
·	CLK		1	3.2	
^t en	ŌĒ	Y	1.8	5.5	ns
^t dis	ŌĒ	Y	1.8	6	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 1 ns, $t_f \leq$ 1 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. $V_{TT} = V_{REF} = V_{CC} \times 0.45$
 - F. tpLz and tpHz are the same as tdis.
 - G. tpzL and tpzH are the same as ten.
 - H. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCBS709A - OCTOBER 1997 - REVISED MAY 1998

- Member of the Texas Instruments Widebus™ Family
- Supports SSTL_3 Signal Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL_3 Class I and Class II Specifications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Thin Shrink Small-Outline Package

description

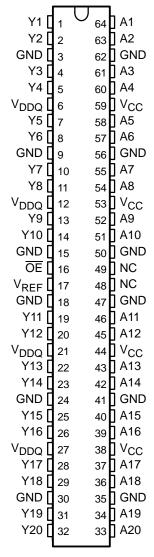
This 20-bit buffer is designed for 3-V to 3.6-V V_{CC} operation and SSTL_3 input levels.

Data flow from A to Y is controlled by the output-enable (\overline{OE}). When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16847 is characterized for operation from 0°C to 70°C.

DGG PACKAGE (TOP VIEW)

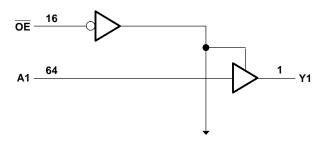


NC - No internal connection

FUNCTION TABLE

INP	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

logic diagram (positive logic)



To 19 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} or V _{DDQ}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{DDQ} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O (V _O = 0 to V _{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
Storage temperature range, T _{stg}	

functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

				MIN	NOM	MAX	UNIT
Vcc	Supply voltage		V _{DDQ}		3.6	V	
V _{DDQ}	Output supply voltage			3		3.6	V
VREF	Reference voltage ($V_{REF} = 0.45 \times V_{DI}$	DQ)		1.3	1.5	1.7	V
VTT	Termination voltage			V _{REF} -50mV	V _{REF}	V _{REF} +50mV	V
VI	Input voltage			0		VCC	V
VIH	AC high-level input voltage	All inputs	٧	/REF+400mV			V
VIL	AC low-level input voltage	All inputs				V _{REF} -400mV	V
VIH	DC high-level input voltage	All inputs	V	REF+200mV			V
V _{IL}	DC low-level input voltage	All inputs				V _{REF} -200mV	V
ЮН	High-level output current					-20	mΛ
loL	Low-level output current		20	mA			
TA	Operating free-air temperature			0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	PARAMETER	TEST CON	IDITIONS	v _{cc}	MIN	TYP†	MAX	UNIT
VIK		I _I = -18 mA		3 V			-1.2	V
		I _{OH} = -100 μA		3 V to 3.6 V	V _{CC} -0.	2		
Vон		$I_{OH} = -16 \text{ mA}$		3 V	2.2			V
		$I_{OH} = -20 \text{ mA}$		3 V	2.1			
		I _{OL} = 100 μA		3 V to 3.6 V			0.2	
VOL		I _{OL} = 16 mA I _{OL} = 20 mA		3 V			0.5	V
				3 V			0.55	
l .	Data inputs, OE	$V_I = 2.1 \text{ V or } 0.9 \text{ V},$	V _{REF} = 1.3 V or 1.7 V	3.6 V			±5	μΑ
l _l	VREF	V _{REF} = 1.3 V or 1.7 V		3.6 V			±150	μΑ
loz		$V_0 = 0.9 \text{ V or } 2.1 \text{ V}$		3.6 V			±10	μΑ
ICC		$V_{I} = 2.1 \text{ V or } 0.9 \text{ V},$	I _O = 0	3.6 V			90	mA
Ci	Control inputs	\(\(\frac{1}{2}\) \(\frac{1}{2}\) \(\frac{1}{2	I = 2.1 V or 0.9 V			2		pF
	A port	V = 2.1 V OI 0.9 V				2.5		ρī
Co	Y port	$V_0 = 2.1 \text{ V or } 0.9 \text{ V}$		3.3 V		3.5		pF

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN74SSTL16847 20-BIT SSTL_3 INTERFACE BUFFER WITH 3-STATE OUTPUTS

SCBS709A - OCTOBER 1997 - REVISED MAY 1998

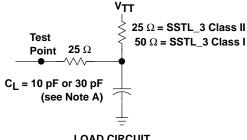
switching characteristics over recommended operating free-air temperature range, Class I, $V_{REF} = V_{TT} = V_{DDQ} \times 0.45$ and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
^t pd	A	Υ	1.5	3	ns
t _{en}	ŌĒ	Υ	1.5	4	ns
^t dis	ŌĒ	Y	1.6	4.9	ns

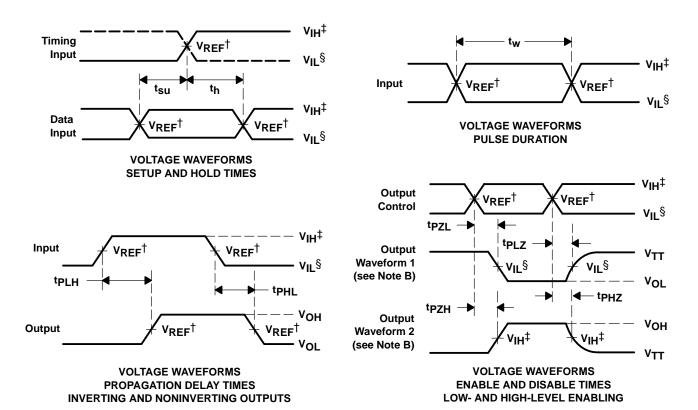
switching characteristics over recommended operating free-air temperature range, Class II, $V_{REF} = V_{TT} = V_{DDQ} X$ 0.45 and $C_L = 30 \ pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd}	А	Υ	1.5	3	ns
t _{en}	ŌĒ	Υ	1.5	4.1	ns
^t dis	ŌĒ	Υ	1.5	4.8	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



 $^{^{\}dagger}$ V_{REF} = 0.45 V_{DDQ}

NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 1.25 ns/V, $t_f \le 1.25 \text{ ns/V}.$
- The outputs are measured one at a time with one transition per measurement.
- E. VTT = VREF = VDDQ X 0.45
- F. tpLZ and tpHZ are the same as tdis.
- G. tpzL and tpzH are the same as ten.
- H. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



[‡]V_{IH} = V_{REF}+400mV (AC voltage levels)

[§] V_{IL} = V_{REF}-400mV (AC voltage levels)

- **Member of the Texas Instruments** Widebus™ Family
- Supports SSTL_2 Signal Data Inputs and **Outputs**
- Supports LVTTL Switching Levels on the **RESET Pin**
- **Differential CLK Signal**
- Flow-Through Architecture Optimizes PCB
- Meets SSTL 2 Class I and Class II **Specifications**
- Packaged in Plastic Thin Shrink **Small-Outline Package**

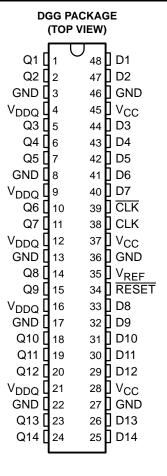
description

This 14-bit registered buffer is designed for 2.3-V to 3.6-V V_{CC} operation and SSTL_2 input and output levels.

Data flow from D to Q is controlled by differential clock pins (CLK, CLK) and the RESET. Data are triggered on the positive edge of the positive clock (CLK). The negative clock (CLK) must be used to maintain noise margins. When RESET is low, all registers are reset, and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

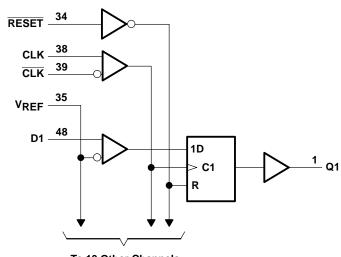
The SN74SSTL16857 is characterized for operation from 0°C to 70°C.



FUNCTION TABLE (each flip-flop)

	OUTPUT			
RESET	CLK	CLK	D	Q
L	Х	Х	Х	L
Н	\downarrow	\uparrow	Н	Н
Н	\downarrow	\uparrow	L	L
Н	L or H	L or H	Х	Q_0

logic diagram (positive logic)



To 13 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} or V _{DDQ}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{DDQ} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{DDQ} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0)$	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O (V _O = 0 to V _{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	106°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		V_{DDQ}		3.6	V
V _{DDQ}	Output supply voltage		2.3		2.7	V
VREF	Reference voltage (V _{REF} = V _{DDQ} /2)		1.15	1.25	1.35	V
VTT	Termination voltage		V _{REF} -40mV	V _{REF}	V _{REF} +40mV	V
٧ _I	Input voltage		0		VCC	V
VIH	AC high-level input voltage	Data inputs	V _{REF} +350mV			V
V _{IL}	AC low-level input voltage	Data inputs			V _{REF} –350mV	V
VIH	DC high-level input voltage	Data inputs	V _{REF} +180mV			V
V _{IL}	DC low-level input voltage	Data inputs			V _{REF} -180mV	V
V _{IH}	High-level input voltage	Control inputs	2			V
V _{IL}	Low-level input voltage	Control inputs			0.8	V
VICR	Common-mode input voltage range	CLK, CLK	0.97		1.53	V
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	360			mV
ІОН	High-level output current				-20	mA
l _{OL}	Low-level output current				20	IIIA
T _A	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SCAS625 - FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT		
VIK		$I_{I} = -18 \text{ mA}$		2.3 V			-1.2	V
		I _{OH} = -100 μA		2.3 V to 2.7 V	V _{CC} -0.2			
Vон		I _{OH} = -8 mA		2.3 V	1.95			V
		I _{OH} = -16 mA		2.3 V	1.95			
		I _{OL} = 100 μA		2.3 V to 2.7 V			0.2	
V_{OL}		$I_{OL} = 8 \text{ mA}$		2.3 V			0.35	V
	-	I _{OL} = 16 mA		2.5 V			0.35	
		V _I = 1.7 V or 0.8V		2.7 V			±5	
	Data inputs	V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V	2.7 V			±5	Δ
	Data inputs	V _I = 1.7 V or 0.8V	VREF = 1.13 V 01 1.33 V	3.6 V			±5	μΑ
		V _I = 2.7 V or 0					±5	
	CLK, CLK	V _I = 1.7 V or 0.8V	V _{REF} = 1.15 V or 1.35 V	2.7 V			±5	μΑ
l _l		V _I = 2.7 V or 0		2.7 V			±5	mA
"	CLK, CLK	V _I = 1.7 V or 0.8V		3.6 V			±5	μΑ
		V _I = 2.7 V or 0		0.0 V			±5	mA
	RESET	$V_I = V_{CC}$ or GND		2.7 V			±5	μΑ
	RESET	AL = ACC OLOUP		3.6 V			±5	μΑ
	V _{REF}	V _{REF} = 1.15 V or 1.35 V		2.7 V			±5	μΑ
	VREF	VREF = 1.13 V 01 1.33 V		3.6 V			±5	μΑ
		V _I = 1.7 V or 0.8 V		2.7 V			90	
Icc		$V_{ } = 2.7 \text{ V or } 0$	I _O = 0	Z.1 V			90	mA
100		V _I = 1.7 V or 0.8 V]10-0	3.6 V			90	ША
		V _I = 2.7 V or 0		3.0 V			90	
	Control inputs			2.5 V [†]				
C _i	Data inputs	V _I = 1.7 V or 0.8 V		2.5 V I				pF
	Control inputs	V = 1.7 V OI 0.0 V	V = 1.7 V OΓ U.8 V					ρı
Data inputs				3.3 V [‡]				

[†] All typical values are at V_{CC} = 2.5 V, T_{A} = 25°C. ‡ All typical values are at V_{CC} = 3.3 V, T_{A} = 25°C.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} =		V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	
fclock	f _{clock} Clock frequency						MHz
t _W	Pulse duration, CLK, CLK high or low						ns
	Catua tima	Data before CLK↑, CLK↓					
t _{su}	Setup time	RESET high before CLK↑, CLK↓					ns
th	Hold time, data after CLK↑, CLK↓						ns

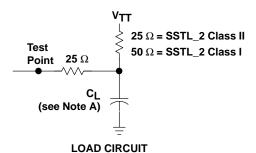
switching characteristics over recommended operating free-air temperature range, Class I, $V_{TT} = V_{REF} = V_{DDQ}/2$, and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)

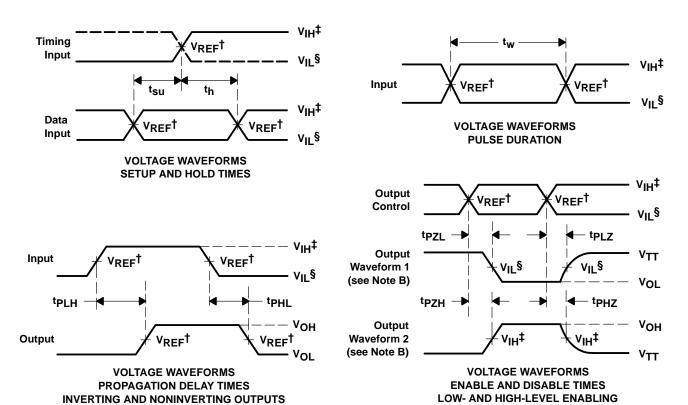
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V	٧	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(6617-61)	MIN MA	λX	MIN	MAX	
f _{max}							MHz
^t pd	CLK and CLK	Q					ns
t _{PHL}	RESET	Q					ns

switching characteristics over recommended operating free-air temperature range, Class II, $V_{TT} = V_{REF} = V_{DDQ}/2$, and $C_L = 30~pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM TO (OUTPUT)		V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			MIN MAX	MIN MAX	
f _{max}					MHz
t _{pd}	CLK and CLK	Q			ns
t _{PHL}	RESET	Q			ns

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V AND V_{CC} = 3.3 V \pm 0.3 V





 $^{^{\}dagger}$ V_{REF} = V_{DDQ}/2

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 1.25 ns/V, $t_f \le 1.25 \text{ ns/V}.$
- D. The outputs are measured one at a time with one transition per measurement.
- E. VTT = VREF = VDDQ/2
- tpLZ and tpHZ are the same as tdis.
- G. tpzL and tpzH are the same as ten.
- H. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



[‡] V_{IH} = V_{REF} + 350 mV (AC voltage levels) § V_{IL} = V_{REF} - 350 mV (AC voltage levels)

SN74SSTL32867 26-BIT REGISTERED BUFFER WITH SSTL 2 INPUTS AND LVCMOS OUTPUTS

SCES240A - APRIL 1999 - REVISED MAY 1999

- Member of the Texas Instruments
 Widebus™ Family
- Supports SSTL_2 Signal Data Inputs
- Supports LVTTL Switching Levels on the RESET Pin
- Flow-Through Architecture Optimizes PCB Layout
- Differential CLK Signal
- Advanced ULTTL Output Circuitry Eliminates Switching Noise in Unterminated Line
- Packaged in Plastic Fine-Pitch Ball-Grid-Array Package

description

This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation and SSTL_2 input and unterminated LVCMOS-output applications.

Data flow from A to Y is controlled by differential clock (CLK, $\overline{\text{CLK}}$) inputs and the LVTTL reset ($\overline{\text{RESET}}$) input. Data are triggered on the positive edge of the positive clock (CLK). The negative clock ($\overline{\text{CLK}}$) is used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The SN74SSTL32867 is characterized for operation from 0°C to 70°C.

GKE PACKAGE (TOP VIEW)

3 4 5 6 00000 Α В 00000 00000 С 00000 D 00000 Ε 00000 F 00000 G 00000н 00000 J 00000 Κ L 00000 00000 М 00000 Ν 00000 Ρ 00000 R Т 00000

terminal assignments

	1	2	3	4	5	6
Α	A1	Vcc	GND	V_{DDQ}	Y1	Y2
В	А3	A2	V _{REF}	GND	Y3	Y4
С	A5	A4	NC	GND	Y5	Y6
D	A7	A6	GND	V_{DDQ}	Y7	Y8
Е	A9	A8	Vcc	GND	Y9	V_{DDQ}
F	A11	A10	GND	V_{DDQ}	Y10	GND
G	A13	A12	Vcc	V_{DDQ}	Y12	Y11
Н	A15	A14	GND	GND	GND	Y13
J	CLK	NC	GND	GND	GND	Y14
K	CLK	RESET	Vcc	V_{DDQ}	Y15	Y16
L	A16	A17	GND	V_{DDQ}	Y17	GND
M	A18	A19	VCC	GND	Y18	V_{DDQ}
N	A20	A21	GND	V_{DDQ}	Y20	Y19
Р	A22	A23	NC	GND	Y22	Y21
R	A24	A25	NC	GND	Y24	Y23
T	A26	Vcc	GND	V_{DDQ}	Y26	Y25

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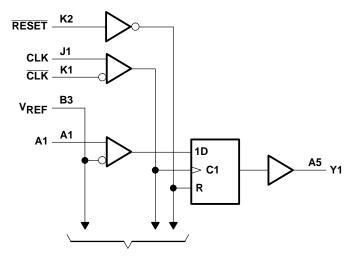


FUNCTION TABLE

	INPUTS					
RESET	CLK	CLK	Α	Υ		
Н	↑	\downarrow	Н	Н		
Н	\uparrow	\downarrow	L	L		
Н	L or H	L or H	Х	Υ ₀		
L .	X	X	Х	L		

logic diagram (positive logic)

SCES240A - APRIL 1999 - REVISED MAY 1999



To 25 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} or V _{DDQ}	
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{DDQ} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	40°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. Current flows only when the output is in the high state and $V_O > V_{DDO}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



SCES240A - APRIL 1999 - REVISED MAY 1999

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		V _{DDQ}		2.7	V	
V _{DDQ}	Output supply voltage		2.3		2.7	V	
VREF	Reference voltage (V _{REF} = V _{DDQ} /2)		1.15	1.25	1.35	V	
VTT	Termination voltage		V _{REF} -40mV	V_{REF}	V _{REF} +40mV	V	
VI	Input voltage	0		VCC	V		
VIH	AC high-level input voltage	Data input	V _{REF} +350mV				
V _{IL}	AC low-level input voltage	Data input			V _{REF} -350mV		
VIH	DC high-level input voltage	Data input	V _{REF} +180mV			V	
V _{IL}	DC low-level input voltage	Data input			V _{REF} -180mV	V	
V _{IH}	High-level input voltage	RESET	1.7			V	
V _{IL}	Low-level input voltage	RESET			0.7	V	
VICR	Common-mode input voltage range	CLK, CLK	0.97		1.53	V	
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	360			mV	
ЮН	High-level output current				-8	A	
loL	Low-level output current				8	mA	
TA	Operating free-air temperature		0		70	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST COND	ITIONS	VCC	MIN	TYP [†]	MAX	UNIT
VIK		I _I = -18 mA	$I_{\parallel} = -18 \text{ mA}$				-1.2	V
		I _{OH} = -100 μA		2.3 V to 2.7 V	V _{CC} -0.	2		
Vон		I _{OH} = -4 mA		2.3 V	2			V
		I _{OH} = -8 mA		2.5 V	1.7			
		I _{OL} = 100 μA		2.3 V to 2.7 V			0.2	
VOL		I _{OL} = 4 mA		2.3 V			0.3	V
	_	$I_{OL} = 8 \text{ mA}$		2.5 V			0.6	
	Data inputs	$V_{ } = 1.7 \text{ V or } 0.8 \text{V}$	V _{REF} = 1.15 V or 1.35 V	2.7 V			±5	
	RESET input	$V_1 = 2.7 \text{ V or } 0$		2.1 V			±5	
l _l	CLK, CLK	V _I = 1.7 V or 0.8V	V _{REF} = 1.15 V or 1.35 V	2.7 V			±5	μΑ
	CLK, CLK	$V_1 = 2.7 \text{ V or } 0$		Z.1 V			±5	
	V _{REF}	V _{REF} = 1.15 V or 1.35 V		2.7 V			±5	
la a		V _I = 1.7 V or 0.8 V	10.0	2.7 V				mA
Icc		V _I = 2.7 V or 0	IO = 0	2.7 V				IIIA
Ci	RESET input	V _I = 1.7 V or 0.8 V	/. 47V or 0.9V					pF
9	Data inputs	v = 1.7 v 01 0.0 v		2.5 V [†]				ρι
Co	Outputs	V _O = 1.7 V or 0.8 V		2.5 V [†]				pF

[†] All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 2.5 V \pm 0.2 V			UNIT
			MIN	TYP	MAX	UNII
fclock	Clock frequency		200			MHz
t _W	Pulse duration, CLK, CLK high or low		1.6	0.8		ns
	Catua tima	Data before CLK↑, CLK↓	1.1	0.5		
tsu	Setup time	RESET high before CLK↑, CLK↓	1.1	0.5		ns
th	Hold time, data after CLK↑, CLK↓		0.5	0		ns

switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)

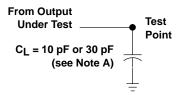
PARAMETER	FROM	то	V_{CC} = 2.5 V \pm 0.2 V			UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	ONIT
f _{max}					200	MHz
t _{pd}	CLK and CLK	Υ		1.9	2.8	ns
^t PHL	RESET	Υ		2.2	3.2	ns

switching characteristics over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and $C_L = 30$ pF (unless otherwise noted) (see Figure 1)

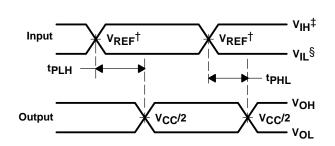
PARAMETER	FROM	то		2.5 V \pm	0.2 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	UNIT
f _{max}					200	MHz
t _{pd}	CLK and CLK	Υ		2.6	3.8	ns
^t PHL	RESET	Y		2.9	4.4	ns

SCES240A - APRIL 1999 - REVISED MAY 1999

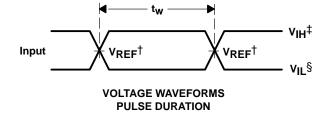
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

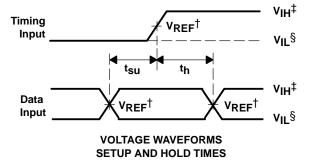


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS





 † V_{REF} = V_{DDQ}/2

NOTES: A. C_I includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 1.25 ns/V, t_f \leq 1.25 ns/V.
- C. The outputs are measured one at a time with one transition per measurement.
- D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

 $^{^{\}ddagger}$ VIH = VREF+350mV (ac voltage levels) for SSTL inputs. VIH = VCC for LVTTL inputs.

[§] V_{IL} = V_{REF}-350mV (ac voltage levels) for SSTL inputs. V_{IL} = GND for LVTTL inputs.

SN74SSTL32877 **26-BIT REGISTERED BUFFER** WITH SSTL 2 INPUTS AND OUTPUTS

SCES241A - APRIL 1999 - REVISED MAY 1999

- **Member of the Texas Instruments** Widebus™ Family
- Supports SSTL_2 Signal Data Inputs and **Outputs**
- Supports LVTTL Switching Levels on the **RESET Pin**
- Flow-Through Architecture Optimizes PCB
- **Differential CLK Signal**
- Meets SSTL_2 Class I and Class II **Specifications**
- Packaged in Plastic Fine-Pitch **Ball-Grid-Array Package**

description

This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation and SSTL_2 input and output levels.

Data flow from A to Y is controlled by differential clock (CLK, $\overline{\text{CLK}}$) inputs, the SSTL_2 output-enable ($\overline{\text{OE}}$) input, and the LVTTL reset (RESET) input. Data are triggered on the positive edge of the positive clock (CLK). The negative clock (CLK) must be used to maintain noise margins. When RESET is low, all registers are reset, and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The SN74SSTL32877 is characterized for operation from 0°C to 70°C.

GKE PACKAGE (TOP VIEW)

2 3 4 5 6

00000 Α 00000 В 00000 С 00000 D 00000 Ε 00000 F 00000 G 00000н 00000 J 00000 Κ L 00000 00000 М 00000 Ν 00000 Ρ 00000 R Т 00000

terminal assignments

	1	2	3	4	5	6
Α	A1	Vcc	GND	V_{DDQ}	Y1	Y2
В	А3	A2	V _{REF}	GND	Y3	Y4
С	A5	A4	NC	GND	Y5	Y6
D	A7	A6	GND	V_{DDQ}	Y7	Y8
Е	A9	A8	VCC	GND	Y9	V_{DDQ}
F	A11	A10	GND	V_{DDQ}	Y10	GND
G	A13	A12	VCC	V_{DDQ}	Y12	Y11
Н	A15	A14	GND	GND	GND	Y13
J	CLK	NC	GND	GND	GND	Y14
K	CLK	RESET	Vcc	V_{DDQ}	Y15	Y16
L	A16	A17	GND	V_{DDQ}	Y17	GND
M	A18	A19	Vcc	GND	Y18	V_{DDQ}
N	A20	A21	GND	V_{DDQ}	Y20	Y19
Р	A22	A23	NC	GND	Y22	Y21
R	A24	A25	ŌĒ	GND	Y24	Y23
Т	A26	Vcc	GND	V_{DDQ}	Y26	Y25

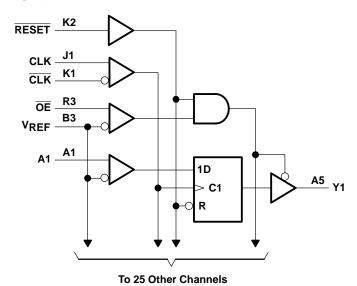
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	FUNCTION TABLE								
	INPUTS								
OE	RESET	CLK	CLK	Α	Y				
L	Н	1	\downarrow	Н	Н				
L	Н	\uparrow	\downarrow	L	L				
L	Н	L or H	L or H	Χ	Yo				
Н	Н	Χ	Χ	X	Z				
Х	L	X	X	Х	L				

logic diagram (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} or V _{DDQ}	0.5 V to 3.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to $V_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{DDQ} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. Current flows only when the output is in the high state and $V_O > V_{DDQ}$.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		V_{DDQ}		2.7	V
V _{DDQ}	Output supply voltage		2.3		2.7	V
VREF	Reference voltage (V _{REF} = V _{DDQ} /2)	Reference voltage (V _{REF} = V _{DDQ} /2)		1.25	1.35	V
VTT	Termination voltage		V _{REF} -40mV	V _{REF}	V _{REF} +40mV	V
VI	Input voltage	Input voltage			VCC	V
VIH	AC high-level input voltage	OE, data inputs	V _{REF} +350mV			V
VIL	AC low-level input voltage	OE, data inputs			V _{REF} -350mV	V
VIH	DC high-level input voltage	OE, data inputs	V _{REF} +180mV			V
VIL	DC low-level input voltage	OE, data inputs			V _{REF} -180mV	V
VIH	High-level input voltage	RESET	1.7			V
V _{IL}	Low-level input voltage	RESET			0.7	V
VICR	Common-mode input voltage range	CLK, CLK	0.97		1.53	V
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	360			mV
ЮН	High-level output current				-20	A
loL	Low-level output current				20	mA
TA	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST COND	ITIONS	VCC	MIN	TYP [†]	MAX	UNIT	
٧ıĸ		I _I = -18 mA		2.3 V			-1.2	V	
		OH = -100 μA		2.3 V to 2.7 V	V _{CC} -0.2	2			
Vон		$I_{OH} = -8 \text{ mA}$		2.3 V	1.95			V	
		I _{OH} = -16 mA		2.3 V	1.95				
		I _{OL} = 100 μA		2.3 V to 2.7 V			0.2		
VOL		I _{OL} = 8 mA		2.3 V			0.35	V	
		I _{OL} = 16 mA		2.3 V			0.35		
	Data inputs	V _I = 1.7 V or 0.8V	V _{REF} = 1.15 V or 1.35 V				±5		
	OE input	V _I = 2.7 V or 0	VREF = 1.15 V 01 1.35 V				±5		
١.	RESET input	V _I = 2.7 V or 0]	±5				
lj	011/ 011/	V _I = 1.7 V or 0.8V	V 4 45 V 27 4 25 V	2.7 V			±5	μΑ	
	CLK, CLK	V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V				±5		
	V _{REF}	V _{REF} = 1.15 V or 1.35 V			±5				
1		V _I = 1.7 V or 0.8 V	1- 0	0.71/				A	
ICC		V _I = 2.7 V or 0	IO = 0	2.7 V				mA	
C.	RESET input	V: - 1.7 V or 0.9 V	4. 4.7.77 - 2.0.77					n.E	
C _i	Data inputs	V _I = 1.7 V or 0.8 V		2.5 V [†]				pF	
Co	Outputs	V _O = 1.7 V or 0.8 V		2.5 V [†]				pF	

 $[\]dagger$ All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 2.5 V \pm 0.2 V			UNIT
			MIN	TYP	MAX	UNIT
f _{clock}	Clock frequency		200			MHz
t _W	Pulse duration, CLK, CLK high or low		1.6	0.8		ns
t _{Su} Setup time	Catua tima	Data before CLK↑, CLK↓	1.1	0.5		20
	Setup time	RESET high before CLK↑, CLK↓	1.1	0.5		ns
t _h	Hold time, data after CLK↑, CLK↓		0.5	0		ns

switching characteristics over recommended operating free-air temperature range, Class I, $V_{TT} = V_{REF} = V_{DDQ}/2$, and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	UNIT
f _{max}					200	MHz
^t pd	CLK and CLK	Υ		1.7	2.5	ns
tPHL	RESET	Υ		2.4	3.5	ns
^t en	ŌĒ	Y		2.6	3.8	ns
^t dis	ŌĒ	Y		2.6	3.8	ns

switching characteristics over recommended operating free-air temperature range, Class II, $V_{TT} = V_{REF} = V_{DDQ}/2$ and $C_L = 30$ pF (unless otherwise noted) (see Figure 1)

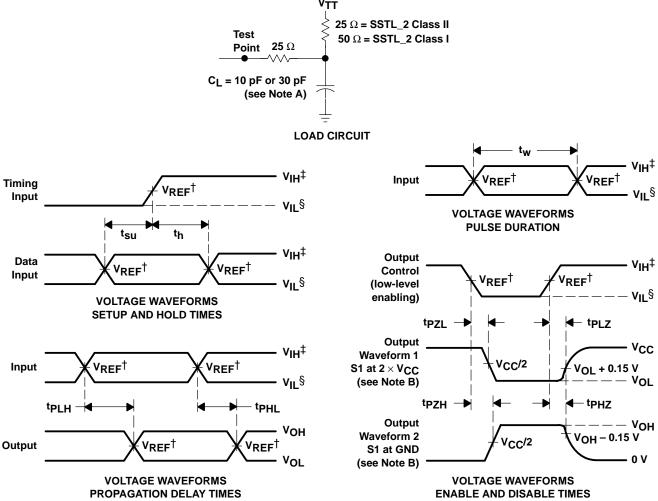
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V \pm 0.2 V			UNIT
			MIN	TYP	MAX	UNIT
f _{max}					200	MHz
^t pd	CLK and CLK	Υ		1.7	2.5	ns
^t PHL	RESET	Y		2.4	3.5	ns
t _{en}	ŌĒ	Y		2.6	3.8	ns
^t dis	ŌĒ	Y		2.6	3.8	ns

SN74SSTL32877

26-BIT REGISTERED BUFFER

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PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



 $[\]dagger V_{RFF} = V_{DDO}/2$

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. $V_{TT} = V_{REF} = V_{DDQ}/2$
- F. tpLz and tpHz are the same as tdis.
- G. tpzL and tpzH are the same as ten.
- H. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



 $[\]pm$ V_{IH} = V_{REF} + 350 mV (ac voltage levels) for SSTL inputs. V_{IH} = V_{CC} for LVTTL inputs.

 $V_{IL} = V_{REF} - 350 \text{ mV}$ (ac voltage levels) for SSTL inputs. $V_{IL} = V_{REF} - 350 \text{ mV}$ (ac voltage levels) for SSTL inputs.

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SN74HSTL16918 9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

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- **Member of the Texas Instruments** Widebus™ Family
- Inputs Meet JEDEC HSTL Std JESD 8-6 and **Outputs Meet Level III Specifications**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

description

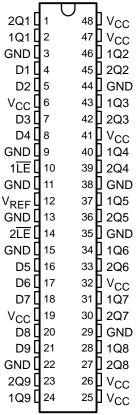
This 9-bit to 18-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The SN74HSTL16918 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable (LE) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While \overline{LE} is low, the Q outputs of the corresponding nine latches follow the D inputs. When LE is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL16918 is characterized for operation from 0°C to 70°C.

DGG PACKAGE (TOP VIEW)



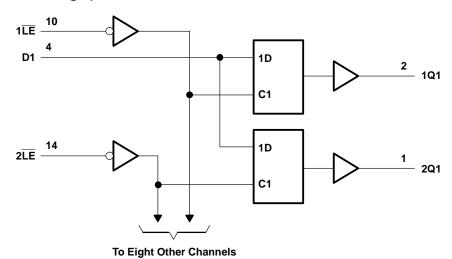
FUNCTION TABLE

INP	UTS	OUTPUT
LE	D	Q
L	Н	Н
L	L	L
Н	Χ	Q ₀ †

†Output level before indicated steady-state input conditions were established

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	89°C/W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 - This current flows only when the output is in the high state and V_O > V_{CC}.
 The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3.15		3.45	V
V _{REF}	Reference voltage		0.68	0.75	0.9	V
٧ _I	Input voltage		0		1.5	V
\vee_{IH}	AC high-level input voltage	All inputs	V _{REF} +200 mV			٧
V_{IL}	AC low-level input voltage	All inputs			V _{REF} -200 mV	V
V_{IH}	DC high-level input voltage	All inputs	V _{REF} +100 mV			V
V _{IL}	DC low-level input voltage	All inputs			V _{REF} -100 mV	V
ІОН	High-level output current				-24	mA
loL	Low-level output current	- -			24	mA
T _A	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TI	TEST CONDITIONS		TYP	MAX	UNIT
٧ıĸ		$V_{CC} = 3.15 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2	V
Vон		$V_{CC} = 3.15 \text{ V},$	$I_{OH} = -24 \text{ mA}$	2.4			V
VOL	_	$V_{CC} = 3.15 \text{ V},$	I _{OL} = 24 mA			0.5	V
	Control inputs		$V_{ } = 0 \text{ or } 1.5 \text{ V}$			±5	
Ιį	Data inputs	V _{CC} = 3.45 V	$V_{I} = 0 \text{ or } 1.5 \text{ V}$			±5	μΑ
	VREF		$V_{REF} = 0.68 \text{ V or } 0.9 \text{ V}$			90	
Icc		$V_{CC} = 3.45 \text{ V},$	V _I = 0 or 1.5 V		50	100	mA
C.	Control inputs	$V_{CC} = 0 \text{ or } 3.3 \text{ V},$	$V_{I} = 0 \text{ or } 3.3 \text{ V}$		2		pF
Ci	Data inputs	$V_{CC} = 0 \text{ or } 3.3 \text{ V},$	V _I = 0 or 3.3 V		2.5		þΓ
Co	Outputs	$V_{CC} = 0$,	VO = 0		4	·	pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} =	3.3 V 5 V	UNIT
			MIN	MAX	
t _W	Pulse duration, LE low		3		ns
t _{su}	Setup time, D before $\overline{\text{LE}} \uparrow$		2		ns
t _h	Hold time	D after LE ↑	1		ns
t _{ldr} ‡	Data race condition time	D after LE ↓		0	ns

[‡] This is the maximum time after LE switches low that the data input can return to the latched state from the opposite state without producing a glitch on the output.

switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
	(INFOT)	(0011 01)	MIN	MAX	
. .	D	0	1.9	3.4	20
^t pd	LE	g	1.9	4.2	ns

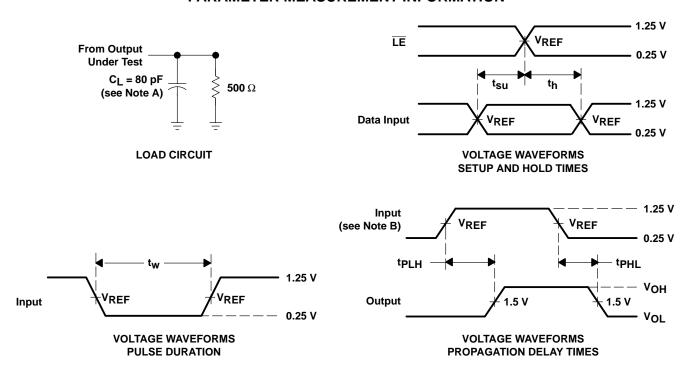
simultaneous switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V_{S}^{\S}

PARAMETER	FROM TO (INPUT) (OUTPUT)		V _{CC} = ± 0.1	UNIT	
	(1141 01)	(6611 61)	MIN	MAX	
	D	0	1.9	4.4	20
^t pd	ĪĒ	g	1.9	5.2	ns

[§] All outputs switching



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 1$ ns.
- C. The outputs are measured one at a time with one transition per measurement.
- D. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74HSTL162822 14-BIT TO 28-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

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- **Member of the Texas Instruments** Widebus™ Family
- Inputs Meet JEDEC HSTL Standard JESD8-6
- All Outputs Have Equivalent 25- Ω Series Resistors
- **Packaged in Plastic Thin Shrink** Small-Outline Package

description

This 14-bit to 28-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. HSTL levels are expected on the inputs. LVTTL levels are driven on the Q outputs.

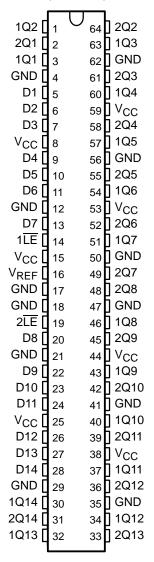
All outputs are designed to sink up to 12 mA and include 25- Ω series resistors to reduce overshoot and undershoot.

The SN74HSTL162822 is particularly suitable for driving an address bus to two banks of memory. Each bank of 14 outputs is controlled with its own latch-enable (\overline{LE}) input.

Each of the 14 data (D) inputs is tied to the inputs of two D-type latches, which provide true data at the outputs. While \overline{LE} is low, the outputs (Q) of the corresponding 14 latches follow the D inputs. When \overline{LE} is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL162822 is characterized for operation from -40°C to 90°C.

DGG PACKAGE (TOP VIEW)



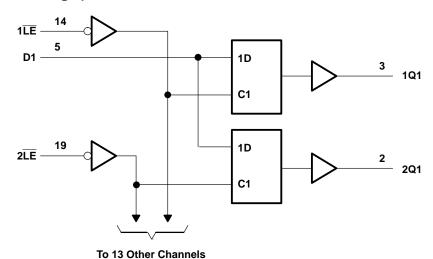
FUNCTION TABLE

INP	JTS	OUTPUT			
LE	D	Q			
L	Н	Н			
L	L	L			
Н	Χ	Q ₀ †			

†Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{K}(V_{I} < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

 - This current flows only when the output is in the high state and V_O > V_{CC}.
 The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vсс	Supply voltage		3.15		3.45	V
V _{REF}	Reference voltage		0.68	0.75	0.9	V
٧ _I	Input voltage		0		1.5	V
VIH	High-level input voltage	All pins	V _{REF} +100 mV			V
V _{IL}	Low-level input voltage	All pins	V _{REF} -100 mV		V	
ЮН	High-level output current		-12		A	
loL	Low-level output current				12	mA
TA	Operating free-air temperature		-40		90	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74HSTL162822 14-BIT TO 28-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	1	TEST CONDITIONS		TYP [†]	MAX	UNIT
٧ _{IK}		$V_{CC} = 3.15 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2	V
Vон		$V_{CC} = 3.15 \text{ V},$	I _{OH} = -12 mA	2.2			V
VOL		$V_{CC} = 3.15 \text{ V},$	I _{OL} = 12 mA			8.0	V
	Control inputs		V _I = 0 or 1.5 V			5	
lj	Data inputs	V _{CC} = 3.45 V	V _I = 0 or 1.5 V			5	μΑ
	VREF		V _{REF} = 0.68 V or 0.9 V			90	
Icc		$V_{CC} = 3.45 \text{ V},$	V _I = 0 or 1.5 V		50	100	mA
C.	Control inputs	$V_{CC} = 0 \text{ or } 3.3 \text{ V},$	V _I = 0 or 3.3 V		2		, r
Ci	Data inputs	$V_{CC} = 0 \text{ or } 3.3 \text{ V},$	V _I = 0 or 3.3 V		2		pF
Co	Outputs	$V_{CC} = 0$,	VO = 0		4		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

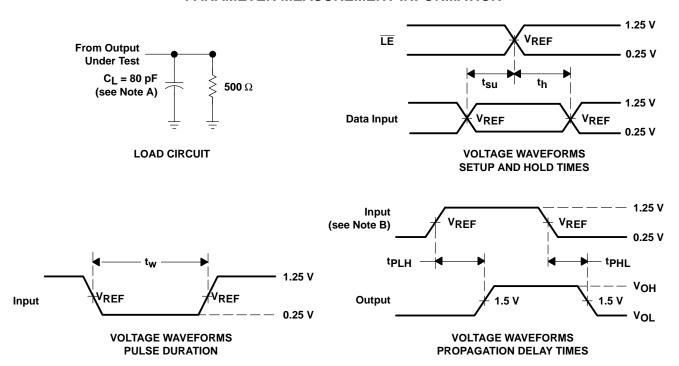
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = ± 0.1	3.3 V 5 V	UNIT
		MIN	MAX	
t _W	Pulse duration, LE low	3		ns
t _{su}	Setup time, D before LE↑	2		ns
th	Hold time, D after LE↑	1		ns

switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
	(1141 01)	(0011 01)	MIN	MAX	
	D	0	1.6	5	20
^t pd	<u>LE</u>	g	1.7	5.7	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 1$ ns.
- C. The outputs are measured one at a time with one transition per measurement.
- D. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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ALVC Gates/Octals	2
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SN74ALB16245	3.3-V ALB 16-Bit Transceiver With 3-State Outputs	8–9

- **Member of the Texas Instruments** Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate **Overshoot and Undershoot**
- **Industry Standard '16244 Pinout**
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (OE) inputs.

SN74ALB16244 is characterized operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

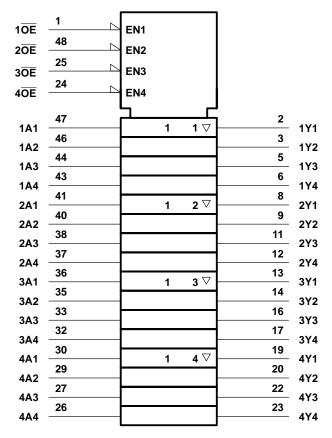
INP	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	X	Z

DGG OR DL PACKAGE (TOP VIEW)

1 OE	1	O	48	2 <u>OE</u>
1Y1	2		47] 1A1
1Y2	3		46] 1A2
GND	4		45	GND
1Y3	5		44	1A3
	6] 1A4
00.	7		42	v_{cc}
	8			2A1
	9		40	2A2
	10		39	GND
	11		38	2A3
	12			2A4
	13			3A1
	14			3A2
	15		34	GND
	16			3A3
	17			3A4
	18			□ v _{cc}
	19		30	4A1
	20		29	4A2
	21		28	GND
-	22		27	4A3
	23		26	4 <u>A4</u>
4 OE	24		25	3 <u>OE</u>

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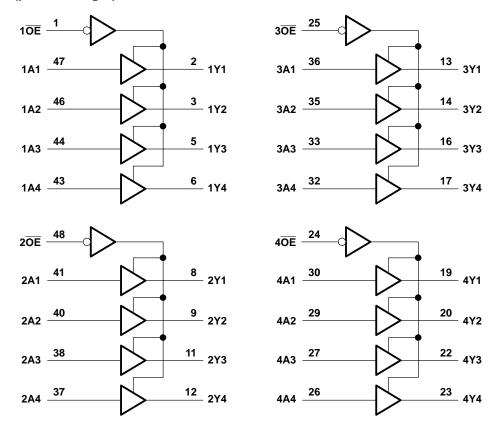
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{IK}(V_I < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	
	94°C/W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		3	3.6	V
I _{OH} †	High-level output current			-25	mA
I _{OL} †	OL [†] Low-level output current			25	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

[†] Refer to Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT		
Viii	Doto inputo	Vaa – 2 V	I _I = 18 mA			3.6	V _{CC} -1.2	V		
VIK	Data inputs	ACC = 3 A	$I_{I} = -18 \text{ mA}$			-0.9	-1.2	V		
	Control inputs	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GN	D			±10	μΑ		
			VI = VCC	OE low		0.4	0.6	mA		
Ц	Data innuta	Va = 2.6.V		OE high			25	μΑ		
	Data inputs	VCC = 3.6 V		OE low		-0.8	-1	mA		
			V _I = 0	OE high			-60	μΑ		
lozh		$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			0.6	20	μΑ		
lozL		$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$			-0.1	- 50	μΑ		
ICC/bu	ffer	V _{CC} = 3.6 V,	$I_{O} = 0$,	$V_I = V_{CC}$ or GND		3.7	5.6	mA		
ICCZ		V _{CC} = 3.6 V,	Control inputs =	V _{CC} or GND			0.8	mA		
ΔlCC§	ΔI_{CC} $V_{CC} = 3 \text{ V to } 3.6 \text{ V, One input at } V_{CC} - 0.6 \text{ V,}$ Other inputs at V_{CC} or GND				600	μА				
Ci		V _I = 3 V or 0						4.5		pF
Co		V _O = 3 V or 0			5.5		pF			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	то	V _{CC} =	= 3.3 V ±	0.3 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP‡	MAX	UNIT
^t pd	А	Y	0.6	1.3	2	ns
t _{en}	ŌĒ	Υ	1.3	2.5	4.7	ns
^t dis	ŌĒ	Υ	1.8	2.8	4.2	ns

[‡] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

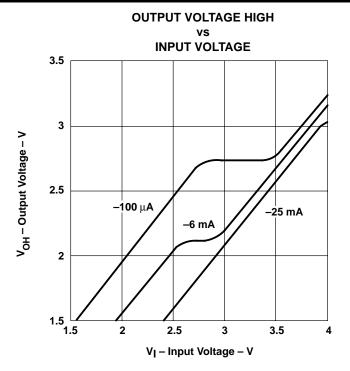


Figure 1. $V_{\mbox{OH}}$ Over Recommended Free-Air Temperature Range

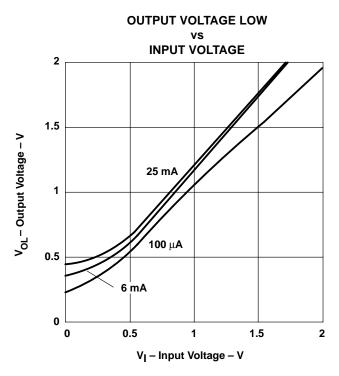
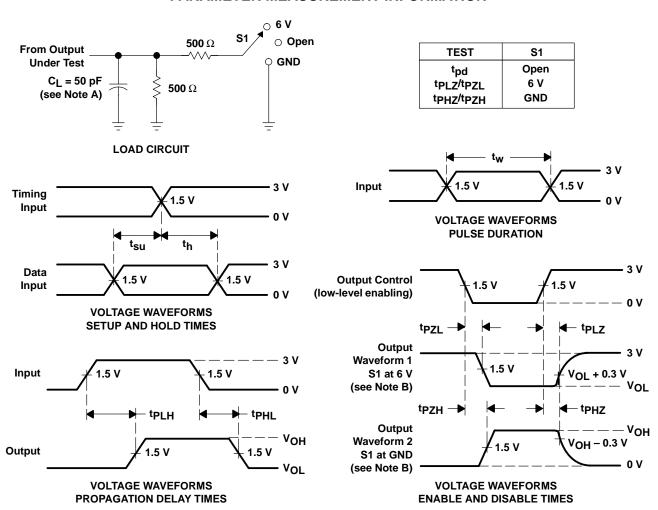


Figure 2. $V_{\mbox{\scriptsize OL}}$ Over Recommended Free-Air Temperature Range



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



SN74ALB16245 3.3-V ALB 16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS678B - SEPTEMBER 1996 - REVISED JULY 1997

•	Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)
•	State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation	1DIR
•	Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot	GND
•	Industry Standard '16245 Pinout	1B4 0 6 43 1A4
•	Distributed V _{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise	$V_{CC} \begin{bmatrix} 1 & 42 \\ 185 \end{bmatrix} V_{CC}$
•	Flow-Through Architecture Optimizes PCB Layout	1B6 09 40 1A6 GND 10 39 GND
•	Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1B7 🖟 11 38 🖟 1A7 1B8 🖟 12 37 🖟 1A8 2B1 🖟 13 36 🖟 2A1
	Small-Outline (DGG) Packages	2B2 14 35 2A2
desc	ription	GND 0 15 34 GND
ucse	in puon	2B3 🛮 16 33 🗓 2A3
	The SN74ALB16245 is a 16-bit transceiver	2B4 🛮 17 32 🗓 2A4
	designed for high-speed, low-voltage (3.3-V) V _{CC}	V _{CC}
	operation. This device is intended to replace the	2B5 19 30 2A5
	conventional transceiver in any speed-critical path. The small propagation delay is achieved	2B6 20 29 2A6
	using a unity gain amplifier on the input and	GND
	feedback resistors from input to output, which	2B7 U 22 27 U 2A7 2B8 [] 23 26 [] 2A8
	allows the output to track the input with a small	2DIR 24 25 2OE

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

The SN74ALB16245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

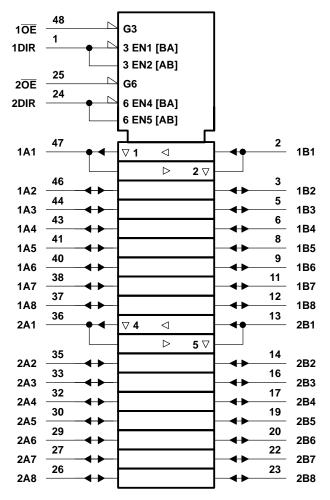
INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

Widebus is a trademark of Texas Instruments Incorporated



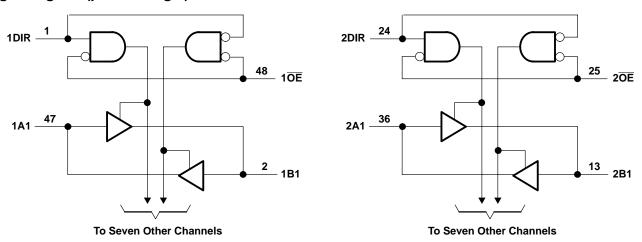
offset voltage.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCBS678B - SEPTEMBER 1996 - REVISED JULY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	V to V_{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)0.5 \	√ to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		3	3.6	V
lOH‡	High-level output current			-25	mA
l _{OL} ‡	Low-level output current			25	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

[‡] Refer to Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITION	ONS	MIN	TYP§	MAX	UNIT
Vinc	A or P porto	V _{CC} = 3 V	I _I = 18 mA			3.7	V _{CC} +1.2	V
VIK	A or B ports	ACC = 2 A	$I_{I} = -18 \text{ mA}$			-0.9	-1.2	V
	Control inputs	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GN	D			±10	μΑ
			\/ ₁ \/ ₂ = 2	OE low		0.4	0.6	mA
I _I	A or P porto	Va = 2 6 V	$\Lambda^{I} = \Lambda^{CC}$	OE high			25	μΑ
	A or B ports	V _{CC} = 3.6 V	V 0	OE low		-0.7	-1	mA
			V _I = 0	OE high			-60	μΑ
lozh		V _{CC} = 3.6 V,	V _O = 3 V			0.7	20	μΑ
lozL		$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V			-0.2	- 50	μΑ
ICC/br	uffer	V _{CC} = 3.6 V,	$I_{O} = 0$,	$V_I = V_{CC}$ or GND		3.7	5.6	mA
ICCZ		V _C C = 3.6 V,	Control inputs =	V _{CC} or GND			0.8	mA
ΔICC¶		V _{CC} = 3 V to 3.6 V Other inputs at V _C		e input at V _{CC} -0.6 V, GND			600	μΑ
C _i		V _I = 3 V or 0				3.5		pF
C _{io}		V _O = 3 V or 0				7.5		pF

[§] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

^{3.} The package thermal impedance is calculated in accordance with JESD 51.

SCBS678B - SEPTEMBER 1996 - REVISED JULY 1997

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	то	V_{CC} = 3.3 V \pm 0.3 V			UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP [†]	MAX	UNIT
^t pd	A or B	B or A	0.6	1.3	2	ns
t _{en}	ŌĒ	A or B	1.5	3.2	6	ns
^t dis	ŌĒ	A or B	1.8	2.8	4.2	ns

 $[\]uparrow$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

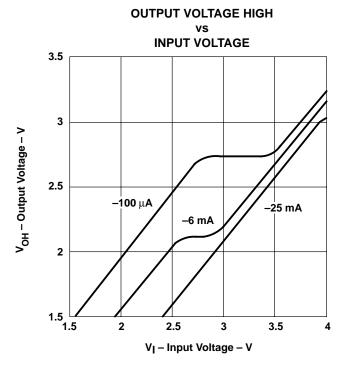


Figure 1. V_{OH} Over Recommended Free-Air Temperature Range

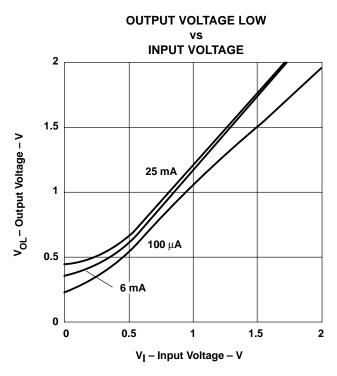
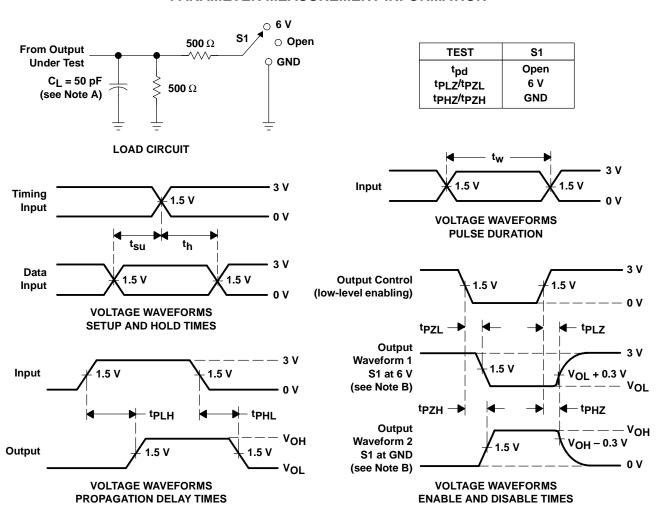


Figure 2. $V_{\mbox{\scriptsize OL}}$ Over Recommended Free-Air Temperature Range



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



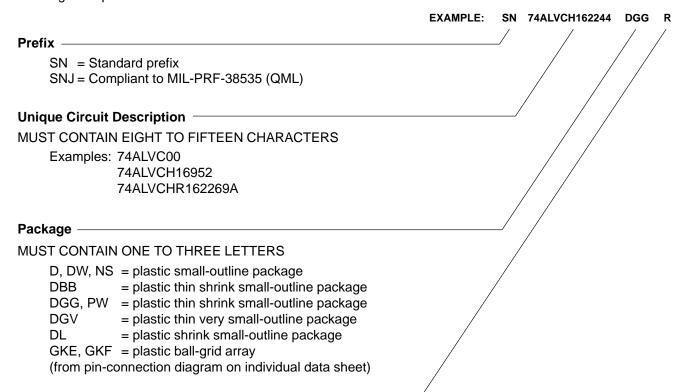
General Information	1
ALVC Gates/Octals	2
ALVC Widebus™/Widebus+™	3
ALVC Widebus™ With Series Damping Resistors	4
ALVC Dual-Supply-Voltage Translators	5
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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.



Tape and Reel Packaging ———

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)

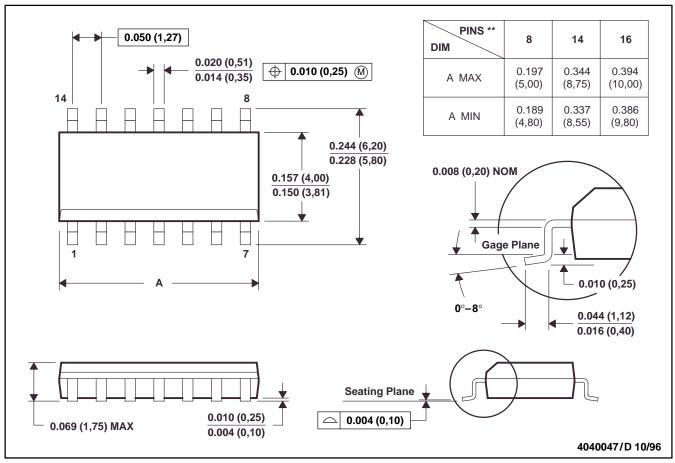
R = Standard tape and reel (required for DBB, DGG, and DGV; optional for D, DL, and DW packages)



D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



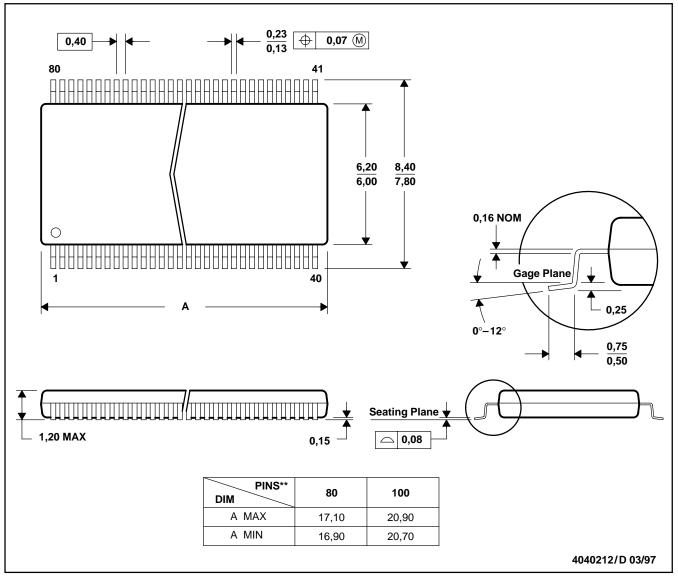
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

DBB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

80 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

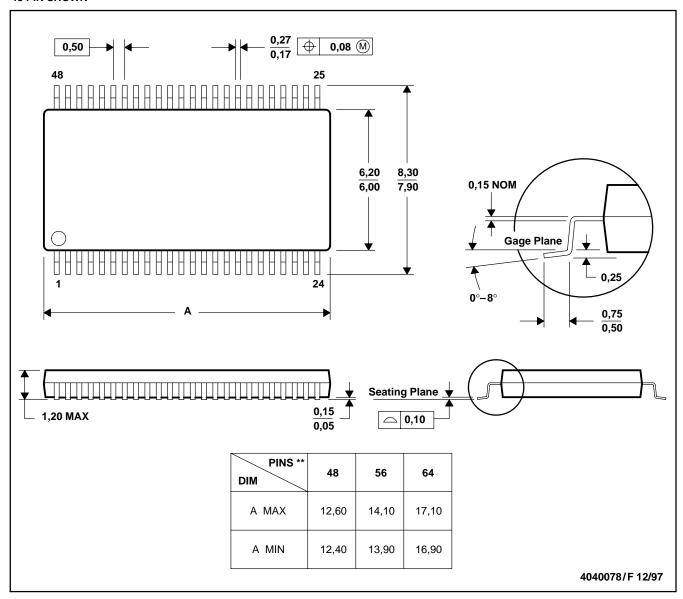
B. This drawing is subject to change without notice.

C. The 80-pin falls within JEDEC MO-153 and the 100-pin falls within JEDEC MO-194.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

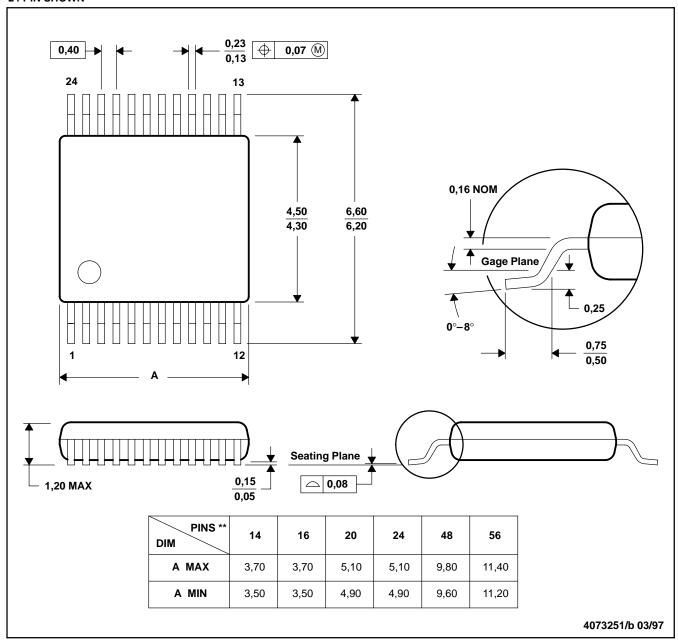
C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24 PIN SHOWN



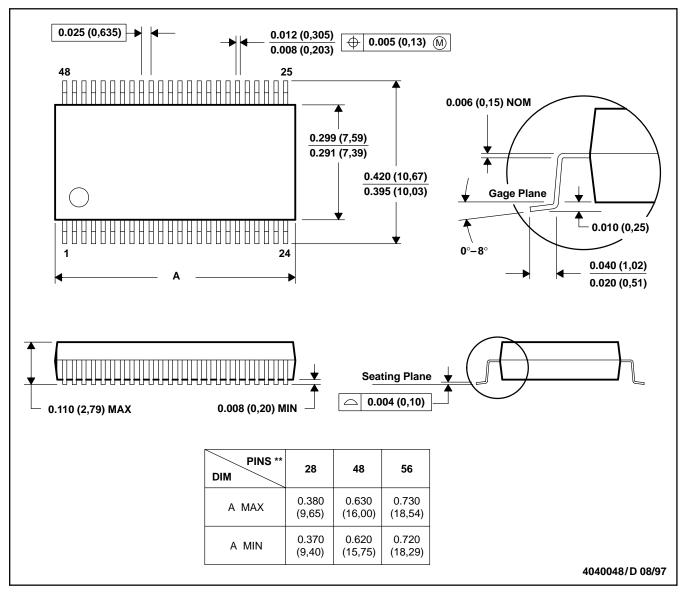
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

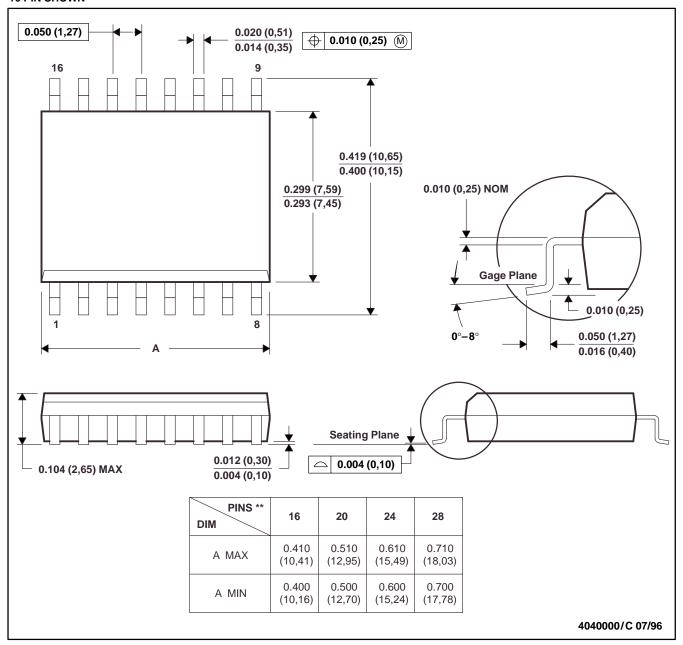
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

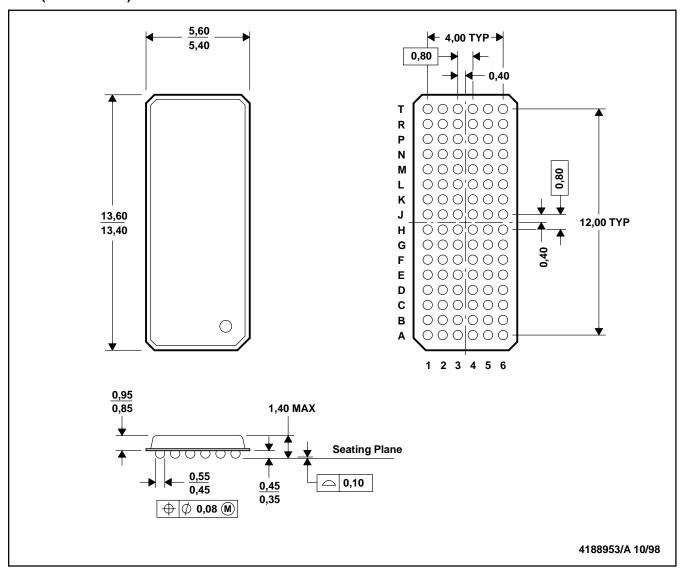
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

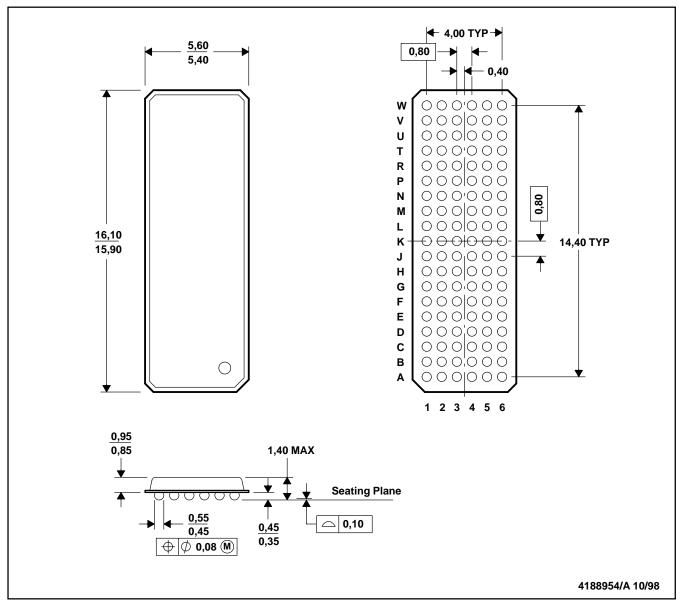
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments Incorporated.



GKF (R-PBGA-N114)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. MicroStar BGA™ configuration

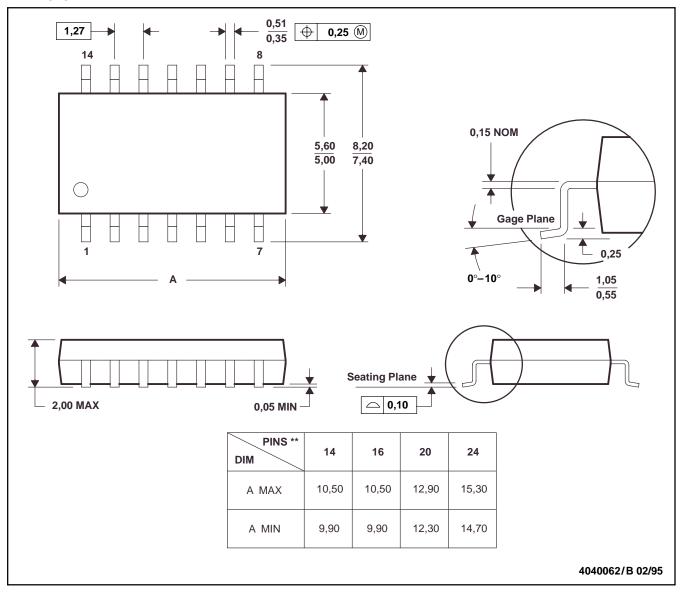
MicroStar BGA is a trademark of Texas Instruments Incorporated.



NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

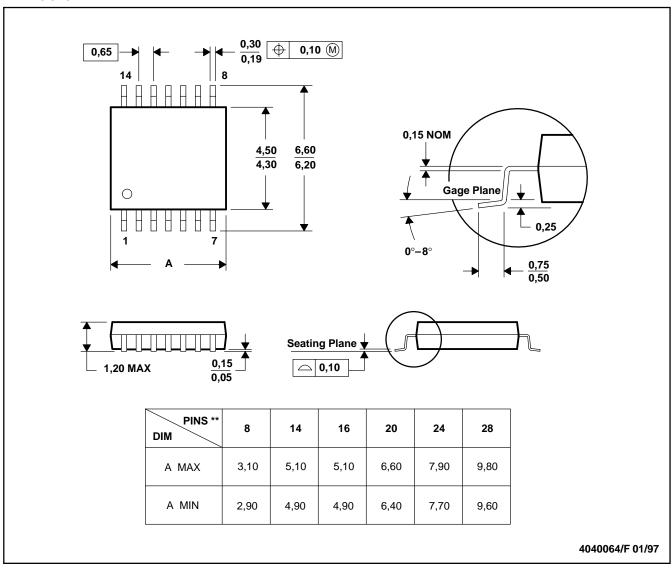
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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Output Derating Curves

Propagation-delay, enable-time, and disable-time parameter values in the ALVC data sheets are provided with V_{CC} ranging from 3 V to 3.6 V and with a load capacitance of 50 pF. As the load capacitance varies, values for these parameters change. Data for Figures 1 through 3 were taken under worst-case scenarios, i.e., with V_{CC} at 3 V and $T_A = 85^{\circ}C$. The data are for capacitive loads from 10 pF to 50 pF, in 10-pF increments. Although the data were taken on the ALVCH16245, the results can be considered representative of all ALVC devices.

Figure A–1 illustrates the effect on propagation delay for high-to-low and low-to-high transitions for the A-to-B direction; B-to-A results were slightly faster than the A-to-B results, but for clarity are not illustrated. For propagation delay, a 10-pF decrease in load capacitance produces approximately a 12.5% decrease in propagation delay.

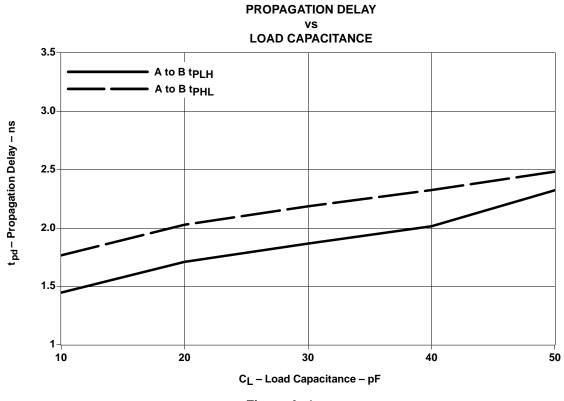


Figure A-1

Figure A–2 illustrates the effect of load capacitance on disable time for high-to-3-state and low-to-3-state transitions for \overline{OE} to A and \overline{OE} to B, respectively. High-to-3-state and low-to-3-state for \overline{OE} to B and \overline{OE} to A results, respectively, were slightly faster, but for clarity are not illustrated. For disable time, a 10-pF decrease in load capacitance produces approximately a 14% decrease in disable time.

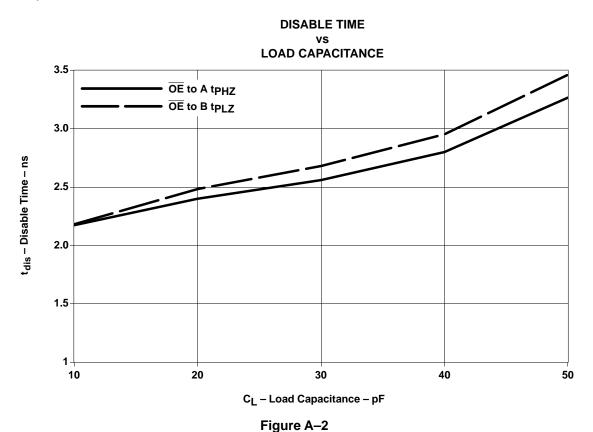


Figure A=3 illustrates the effect of load capacitance on enable time for 3-state-to-high and 3-state-to-low transitions for \overline{OE} to A and \overline{OE} to B, respectively. 3-state-to-high and 3-state-to-low for \overline{OE} to B and \overline{OE} to A results, respectively, were slightly faster, but for clarity are not illustrated. For enable time, a 10-pF decrease in load capacitance produces approximately a 10% decrease in enable time.

