Application Note

Overcoming Design Challenges - Implementing High Performance Interfaces

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ABSTRACT

Today's complex systems have devices operating at multiple voltage nodes that require high-bandwidth, fast-transitions with low-delay. Texas Instruments' TXV family offers options from both the fixed-directional and the general-purpose direction-controlled translation portfolios with the flexibility for high-bandwidth, while avoiding unexpected high and low logic performance issues for applications that can have timing-margin sensitive interfaces. This application note focuses on demonstrating key timing benefits of the TXV family for strict timing applications, using TXV-EVMs.

The application note further describes using the *TXV Voltage Translators and Level Shifters* versus competitor, for systems with strict timing requirements; such as Reduced Gigabit Media Independent (RGMII) applications.

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Trademarks

1 Introduction

RGMII as an example of a high-bandwidth data bus protocol typically communicates with very stringent timing considerations, interfaced between Ethernet Modules such as Media Access Control devices (MAC) / Microcontroller unit (MCU) and Ethernet Physical Layers (PHYs) as shown in Figure 1-2, with aggregate bandwidth as high as 1000Mbps.

RGMII as a communication protocol can be found in many applications that sends data over Ethernet, widely used in industrial, telecommunication and automotive sectors. Figure 1-1 illustrates typical example for transferring data over Ethernet using RGMII. Once all video and audio data are processed, the video and audio data are sent from the MAC or MCU to the PHY where they are serialized and sent over Ethernet.

TXV level shifters are used to bridge voltage mismatch, enabling communication, and further supporting the required timing considerations in RGMII applications.

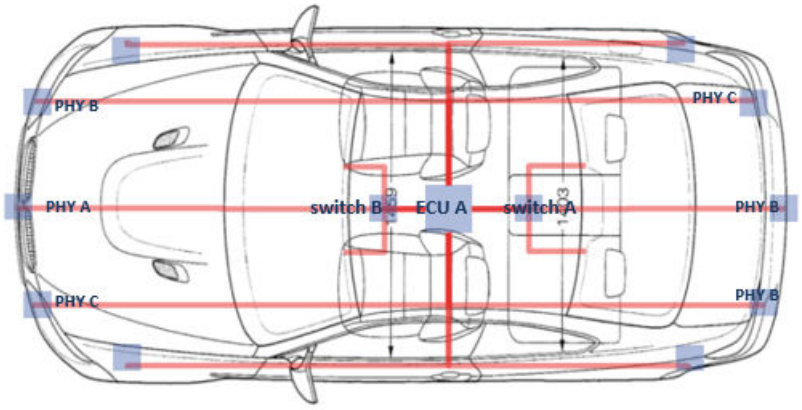

Figure 1-1. Automotive Example for Data Over Ethernet Using RGMII

Table 1-1 highlights RGMII timing considerations. For more information, see *Supporting Time and Skew Sensitive Interfaces with TI's TXV Level-Shifter Portfolio*, application brief.

Table 1-1. RGMII 2.0 Timing Budget

Parameter	Min	Typical	Max	Units
Output Skew	-500	0	500	ps
Duty Cycle	45	50	55	%
Data Rate (Gigabit operation)		125		MHz
Rise / Fall time (20-80%)			750	ps

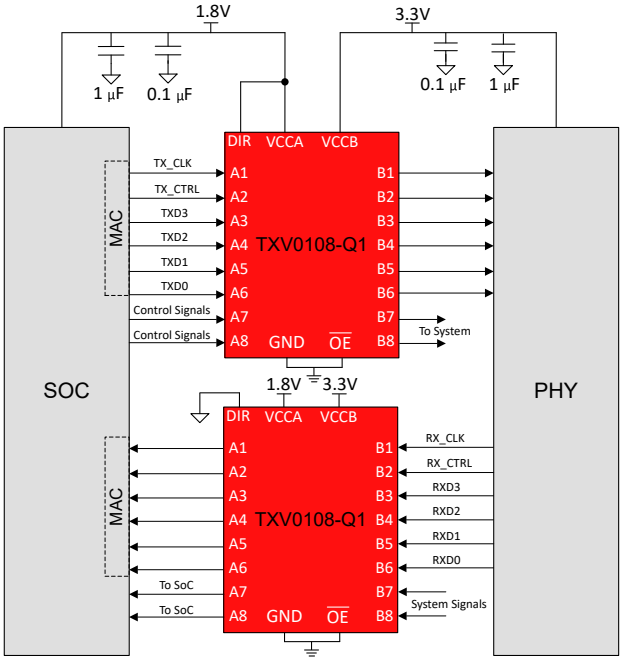

Figure 1-2. TXV0108 Typical Application

1.1 TXV as an Upgradeable Pin-to-Pin Design

In the past, existing level-shifter designs in the market were designed for general level-shifting applications. This posed difficulties for designers confirming if existing designs will work for high performance timing-sensitive interfaces with more complex requirements, such as RGMII. Examples of existing designs from TI includes the AXC (*SN74AXC8T245*) and the AVC families (*SN74AVC8T245*). However, the data sheets do not define the timing budget across process variations, voltages and temperature corners.

TI has developed a new TXV level shifter family, well tested and defined for strict timing budget interfaces across process variations, voltages and temperature corners to support such high performance requirements.

Within the TXV family, *TXV0108 / TXV0108-Q1* (direction-controlled) have been intentionally made pin-to-pin compatible with the existing AXC and AVC families for systems using AXC / AVC for uni-directional applications.

The *TXV0106 / TXV0106-Q1* (fixed-direction) shown in Figure 1-3 is an alternative, offering lower pin count which enables board space and cost savings.

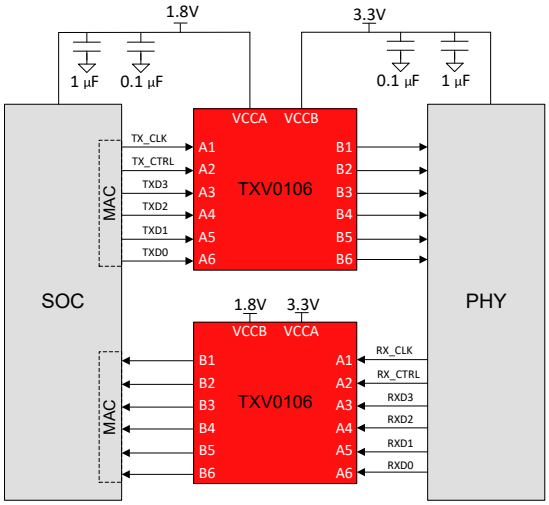

Figure 1-3. Typical TXV0106 Application

As shown, TXV010x can be used to level-shift RGMII signals from MAC to PHY or PHY to MAC. It is recommended that the transmitter clock and data signals are on the same device, as well as the receiver clock and data signals. This is due to a small difference as low as 500 ps in skew (propagation delay between the output channels) may violate the requirement, with the possibility of data errors within the RGMII interfaces.

2 Leveraging TXV for Power Isolation

Electrical noise and interference can negatively affect communication between MAC and PHY when either the MAC or the PHY are powered down, or when both the MAC and PHY do not ramp up simultaneously. TXV can be implemented as a form of isolation to combat signal distortions between hosts / peripherals.

The TXV device is fully specified for partial power-down applications using I_{OFF} and power supply isolation sensitive applications. TXV's V_{CC} isolation feature activates when either V_{CC} supply is < 100 mV or at GND, placing all I/Os in high-impedance. Thereby, protecting the connected downstream devices from miscommunication or damages that might have occurred due to power sequencing limitations between the hosts or peripherals.

The I_{OFF} circuitry disables the output, minimizes noise interference and any damaging back-flow current to downstream devices through TXV when either the host or the peripheral are powered down. Competitor typically specifies higher I_{OFF} leakage current up to 30 µA while TXV is specified for approximately 8x lesser back-flow leakage current of 3.6 µA (max).

For more information, see *Solving Power Sequencing Challenges for Ethernet RGMII Communications*, application brief.

3 Bench Performance

3.1 Leveraging TXV for Low Propagation Delay (T_{PD}) Applications

Low propagation delay is an important factor in high-speed circuit design on newer processors that level shift at low inputs or outputs. Inconsistent or higher propagation delay in an IC can cause data errors at a system level.

Table 3-1 compares TXV and competitor, with TXV measuring overall lower or faster propagation delay than competitor (15 pF / 125 MHz / 25°C, typical bench data).

Table 3-1. Bench - Propagation Delay (T_{pd})

VCCA / VCCB Translation at 250Mbps	*TXV0108* (ns)	Competitor (ns)
1.65 V to 1.65 V	2.35	3.03
1.65 V to 1.8 V	2.26	2.84
1.65 V to 3.6 V	2.05	2.28
1.8 V to 1.8 V	2.1	2.8
1.8 V to 3.6 V	1.96	2.24
AVERAGE	2.14	2.64

3.2 Leveraging TXV for Timing Performance

Table 3-2. Bench - Timing Performance

Parameter - 5 pF	*TXV0108* (ns)	Competitor (ps)	TXV RGMII Margin	Comp RGMII Margin
25°C Skew	21	118	96 % better than spec	76 % better than spec
125°C Skew	43	156	91 % better than spec	69 % better than spec
25°C Rise or Fall Time	484 / 417	782 / 775	36 % better than spec	4 % **worst** than spec
125°C Rise or Fall Time	555 / 507	885 / 890	26 % better than spec	19 % **worst** than spec

The output skew is defined as the time difference between the delay on output channels while driving equal loads. It is important in the RGMII interface for the high-speed clock to synchronize the data on RX and TX lines with maximum allowed skew of 500 ps and maximum rise and fall transition times of 750 ps. Table 3-2 shows how TXV passes and how competitor can fail, for the lower skew and faster transition requirement.

- Figure 3-1 measures the rise-to-rise output channel-to-channel skew for A-to-B direction rising-edge input under standard RGMII loading condition of 5 pF for TXV (measuring 21 ps, tighter skew) vs competitor (measuring approximately 6x looser skew).
- Figure 3-2 measures fall or rise times for TXV (measuring 484 / 417 ps) vs competitor (measuring approximately 2x slower rise or fall times >750 ps), violating RGMII requirement.

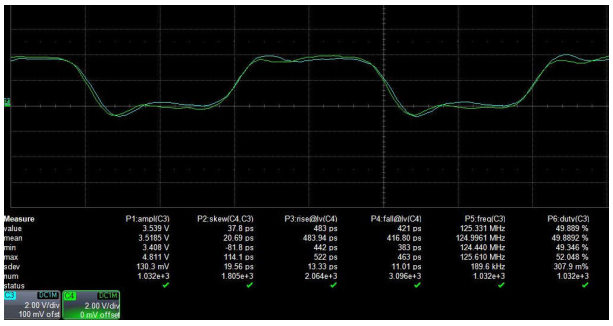

Figure 3-1. TXV Outputs (5 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

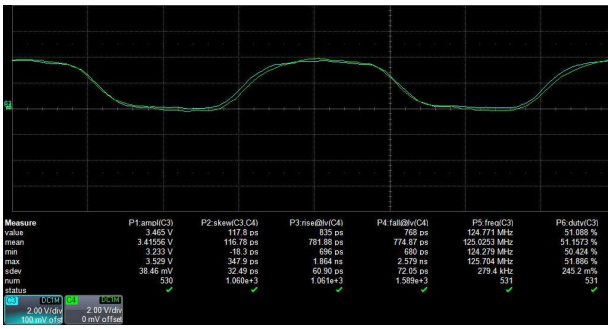

Figure 3-2. Competitor Outputs (5 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

- As temperature increases to 125°C, Figure 3-3 compares *TXV0108* (measuring 555 / 507 ps rise or fall times, 43 ps tighter rise-to-rise skew) with competitor (measuring approximately 4x looser skew and approximately 2x slower rise or fall times >750 ps), violating RGMII's timing budget shown in Figure 3-4.

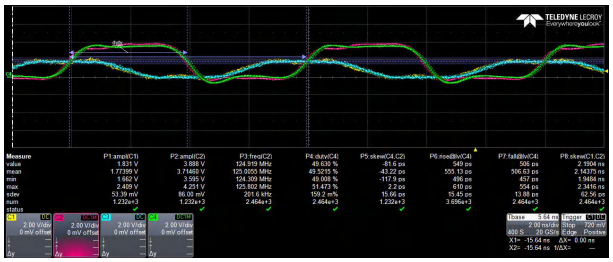

Figure 3-3. TXV Waveform (5 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 125°C)

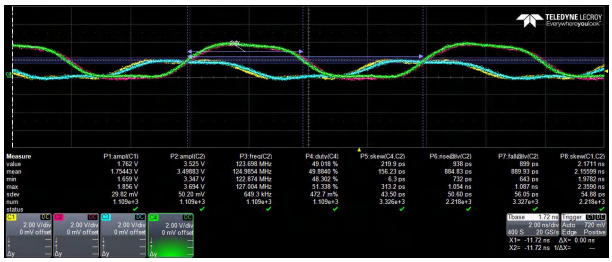

Figure 3-4. Competitor Waveform (5 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 125°C)

3.3 Leveraging TXV for Buffering

Table 3-3. Bench - Buffering Performance

Parameter	*TXV0108* (ns)	Competitor (ps)	TXV RGMII Margin	Comp RGMII Margin
10 pF $Skew_{rf}$ / $Skew_{fr}$	164 / 61	39 / 257	67 % better than spec	49 % better than spec
10 pF Rise/Fall Time	698/ 534	900 / 833	10 % better than spec	20 % **worst** than spec
15 pF $Skew_{rf}$ / $Skew_{fr}$	53 / 181	195 / 93	64 % better than spec	61 % better than spec
15 pF Rise/Fall Time	752 / 652	1200 / 1300	0.3 % worst than spec	73 % **worst** than spec

- Table 3-3 shows rise-to-fall and fall-to-rise skew data collected using a pseudo-random binary sequence (PRBS) signal generator due to the difficulty / randomness to predict, further highlighting worst timing margins observed on bench, for high performance interfaces during random conditions with increased load.

As mentioned, skew between MAC and PHY can lead to data errors and performance issues. Today, complex systems tend to use connectors or longer traces in designing printed circuit boards (PCB), incorporating additional parasitic capacitance. Choosing the correct level-shifter for buffering, can increase the chances of overcoming such design challenges between the hosts or peripherals.

RGMII standard assumes 5 pF loading conditions for the interface's I/O, and can increase as design complexities increases with additional parasitic capacitance. Designers can use TXV for buffering more than the assumed standard load condition to support RGMII's timing conditions for data and clock signals.

- For 10 pF, Figure 3-5 shows TXV outputs (measuring PRBS rise-to-fall skew of 164 ps and fall-to-rise skew of 61 ps) vs competitor (measuring 39 ps and 257 ps respectively). For fall or rise times, TXV (measured 698 or 534 ps) vs competitor (measuring approximately 2x slower rise or fall times >750 ps), violating RGMII requirement as shown in Figure 3-6.

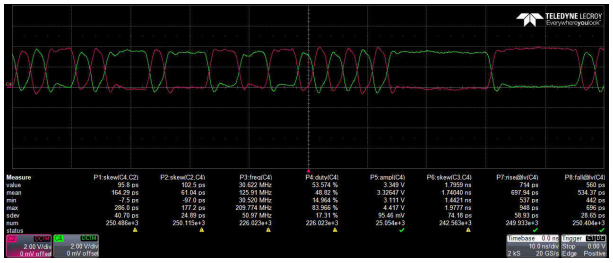

Figure 3-5. TXV Outputs (10 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

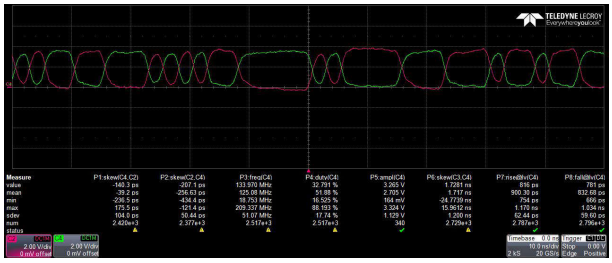

Figure 3-6. Competitor Outputs (10 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

- For 15 pF, Figure 3-7 shows TXV outputs (measuring PRBS rise-to-fall skew of 53 ps and fall-to-rise skew of 181 ps) vs competitor (measuring 195 ps and 93 ps respectively). For fall or rise times, TXV (measured 752 / 652 ps) vs competitor (measuring approximately 2x slower rise or fall times >750 ps), violating RGMII requirement as shown in Figure 3-8.

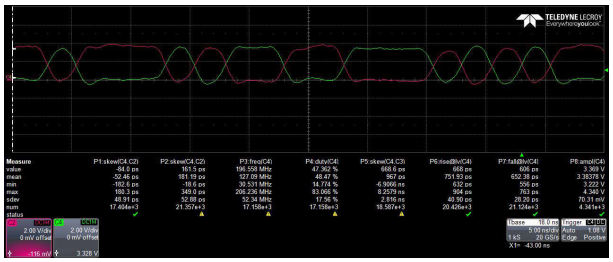

Figure 3-7. TXV Outputs (15 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

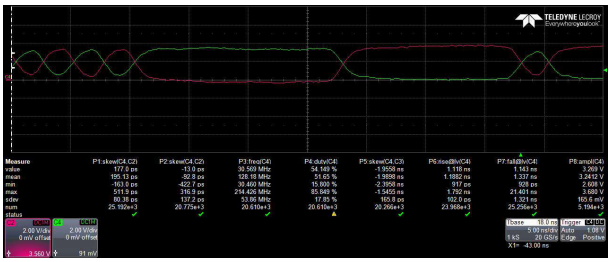

Figure 3-8. Competitor Outputs (15 pF 1.8 V to 3.3 V Up Translation at 125 MHz, 25°C)

3.4 Leveraging TXV for High-Bandwidth Applications

Table 3-4. Bench - 3.3 V V_{CCO} Bandwidth Performance

Parameter - 560Mbps	TXV (V)	Competitor (V)	Valid Levels (V) {0.7*V_{CCO} and 0.3*V_{CCO}}
VOH	2.6	1.8	> 2.31
VOL	0.032	1.3	< 0.99

- Figure 3-9 shows typical bench data for TXV (1.8 V red inputs, 3.3 V green outputs) running at 560Mbps (280 MHz) with stable VOH (as high as 2.6 V) and stable VOL (as low as 32 mV).
- Figure 3-10 shows how competitor can fail (1.8 V blue inputs, 3.3 V green outputs) with unstable VOH (as low as 1.9 V) and unstable VOL (as high as 1.3 V) for invalid logic switching levels.

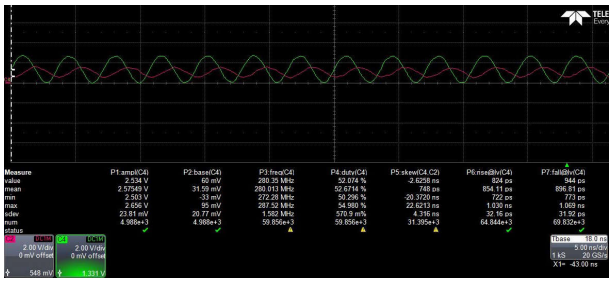

Figure 3-9. TXV Waveform (15 pF 1.8 V to 3.3 V Up Translation at 280 MHz, 25°C)

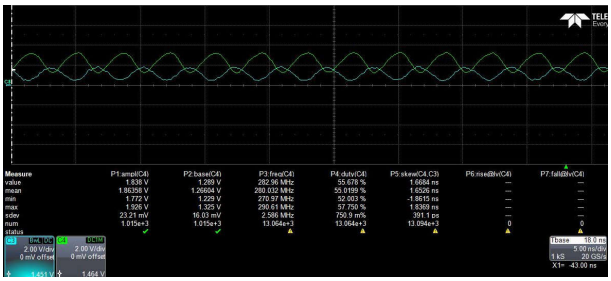

Figure 3-10. Competitor Waveform (15 pF 1.8 V to 3.3 V Up Translation at 280 MHz, 25°C)

For interfaces higher than 560Mbps (280 MHz), Figure 3-11 shows typical bench data with TXV (1.8 V red inputs, 3.6 V green outputs) running at 600Mbps (300 MHz) with VOH / VOL levels at 2.2 V and 0.3 V respectively, measuring low propagation delay (as fast as 1 ns), with 15 pF load.

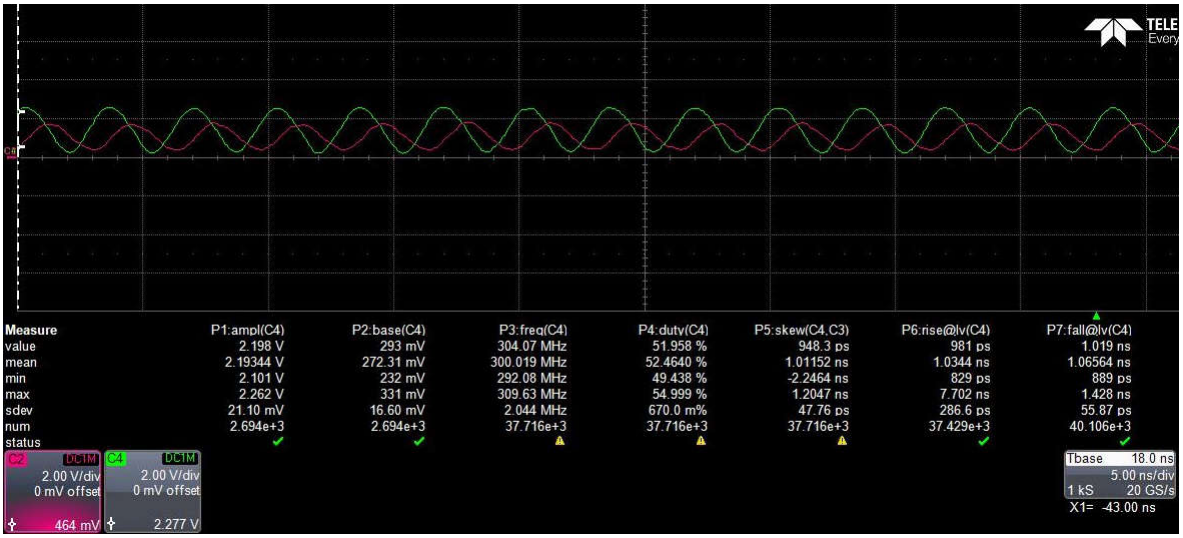

Figure 3-11. TXV Outputs (15 pF 1.8 V to 3.6 V Up Translation at 300 MHz, 25°C)

For typical applications such as 3.3 V, TI's *TXV0108* measured faster data throughput with stable outputs while competitor can fail with unstable outputs as shown in Table 3-4, with damages prevalent. Switching around 1/2 of the output's V_{cc} can lead to increased current draw with the likelihood of damaging the device if above the absolute maximum ratings. Refer to *Implications of Slow or Floating CMOS Inputs,* for additional information.

4 Summary

To support communication for high bandwidth applications with strict timing budgets, the TXV high-speed voltage translator with tighter output channel-to-channel skew and very fast transition rate (as compared to competitor), is recommended.

To conclude, use the *TXV0106 / TXV0106-Q1* or *TXV0108 / TXV0108-Q1* devices for tighter skew, faster rise or fall time, robust buffering, robust back-flow current protection, high data rate capabilities, and minimal propagation delay interfaces.

5 References

1. Texas Instruments, *Implications of Slow or Floating CMOS Inputs*, application note.
2. Texas Instruments, *Supporting Time and Skew Sensitive Interfaces with TI's TXV Level-Shifter Portfolio*, application brief.
3. Texas Instruments, *Solving Power Sequencing Challenges for Ethernet RGMII Communications*, application brief.

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