Application Brief

Optimizing Mechanically Scanning LIDAR With Logic and Translation

Albert Xu *Interface Logic*

Functional Block Diagram

For the purpose of this application brief, Figure 1 shows logic and translation use cases. Each red block is associated to a use-case document. Table 1 and Table 2 list documentation links. For a complete block diagram, see the Mechanically Scanning LIDAR product page.

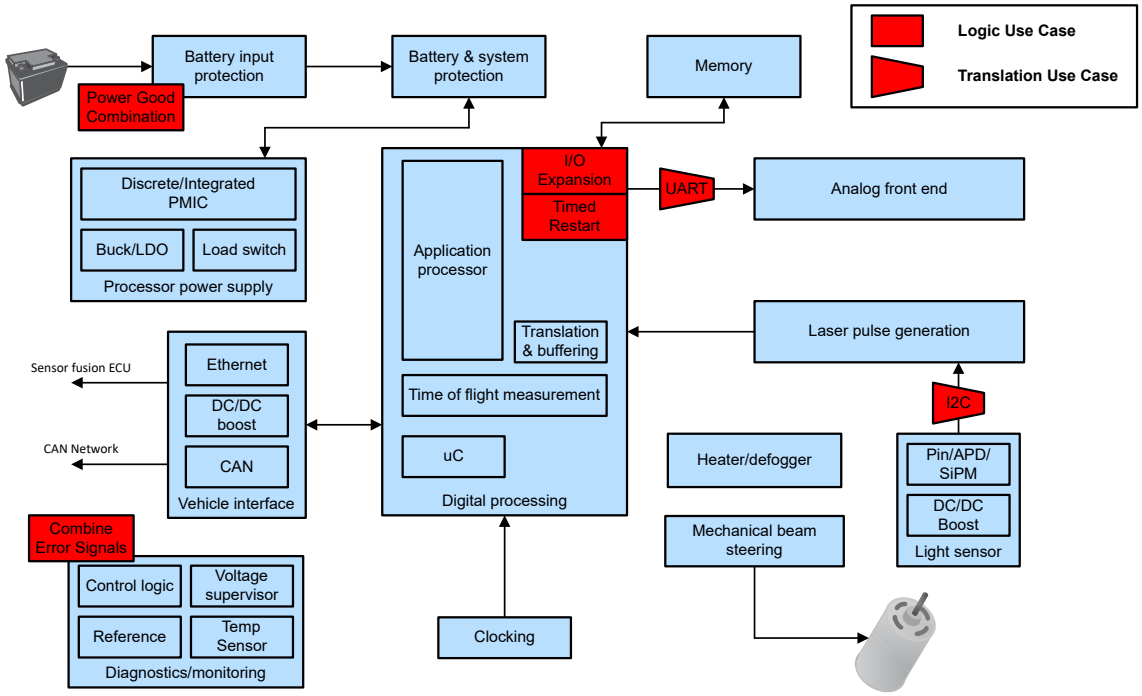


Figure 1. Simplified Block Diagram for Mechanically Scanning LIDAR

Logic and Translation Use Cases

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in Figure 1 .

Table 1. Logic Use Cases

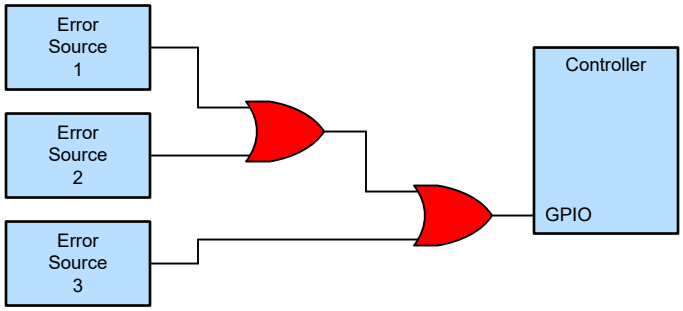
Nearest Block	Use-Case Identifier	Use Case
Battery input protection	Power good combination	*Combine Power Good Signals*
Digital processing	I/O expansion	*Increase Inputs on a uC*
	Timed restart	*Reset a System for a Short Time*
Diagnostics and monitoring	Combine error signals	*Use Fewer Inputs to Monitor Error Signals*

Table 2. Translation Use Cases

Nearest Block	Use-Case Identifier	Use Case
Digital processing	UART translation	*Translate Voltages for UART*
Light sensor	I2C translation	*Translate Voltages for I2C*

Combining Error Signals

Error source signals can be combined to reduce the number of required inputs to a system controller when it is more important to know *that* an error has occurred than it is to know which device triggered the error. For example, if an overheating condition is detected, it is likely that the system can increase fan speed or shut down operations to respond to the issue regardless of which device signaled the error.



Example Block Diagram for Combining Three Error Sources Into One Error Signal Using OR Gates

See the *Use Fewer Inputs to Monitor Error Signals* video to learn more about this use case.

Table 3. Recommended Parts

Part Number	Automotive Qualified	V_{CC} Range	Type	Features
SN74HCS21-Q1	✓	2 V – 6 V	Dual 4-input AND gate	Schmitt trigger inputs Positive and negative clamp diodes on all inputs and outputs
SN74LVC1G125-Q1	✓	1.65 V – 5.5 V	Single buffer with 3-state outputs	Standard CMOS inputs Inverting OE signal; see '1G126 for non-inverting OE signal
SN74LVC1G11-Q1	✓	1.65 V – 5.5 V	Single 3-input AND gate	Standard CMOS inputs Supports partial-power-down with I_{off} circuitry, disabling outputs.
SN74LVC1G96-Q1	✓	1.65 V – 5.5 V	Configurable multi-function gate	Schmitt trigger inputs Between the '1G57 and '1G58, all 2-input logic gate functions can be produced. See data sheets for details.

For more devices with Schmitt trigger input architecture, see the online parametric tool which can be sorted by the desired voltage, output current, and other features.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265