Application Brief

Enabling Power-Efficient FPGA Designs With Level Translation

Atul Patel *Translation Interface*

The use of FPGAs (Field Programmable Gate Arrays) in electronic systems and products is popular as FPGAs have grown and as the variety of offerings have increased. The popularity of FPGAs has increased given the flexibility that FPGAs afford users in terms of allowing them to reprogram processors rather than waiting for a new silicon spin. In addition, FPGAs reduce design cycle times by enabling system designers to quickly prototype new functionality by implementing firmware updates rather than going through time consuming hardware changes. FPGAs are available in a wide spectrum of capabilities with many of the newest FPGAs rivaling some of the most complex custom ASICs (Application Specific Integrated Circuits) that are being developed.

The increases in FPGA processing power, I/Os (Input/Output), and memory provide designers with many options for implementing specific designs. However, using these FPGA resources often comes at the cost of higher power dissipation when using many of the resources that are available on modern FPGAs. FPGA vendors often provide recommendations for provisioning the vendors FPGAs for achieving a lower overall power envelope for a given FPGA design.

Often, FPGA provisioning recommendations require FPGA core voltages to be lowered to below common voltage rails such as 1.8V or 3.3V. For example, complex FPGAs with large Look Up Table (LUT) counts, FPGA vendors can recommend operating the FPGA at a core voltage such as 1.2V or even lower to achieve designed for power consumption. The lower core voltage translates into lower I/O voltages that the FPGA can support. One of the design challenges that system designers face when working with an FPGA operating at a core voltage of 1.2V or lower is that the peripheral devices the FGPA connects with often operates at I/O voltages much higher than the FPGA I/O can support, which results in an I/O voltage level mismatch (See Figure 1).

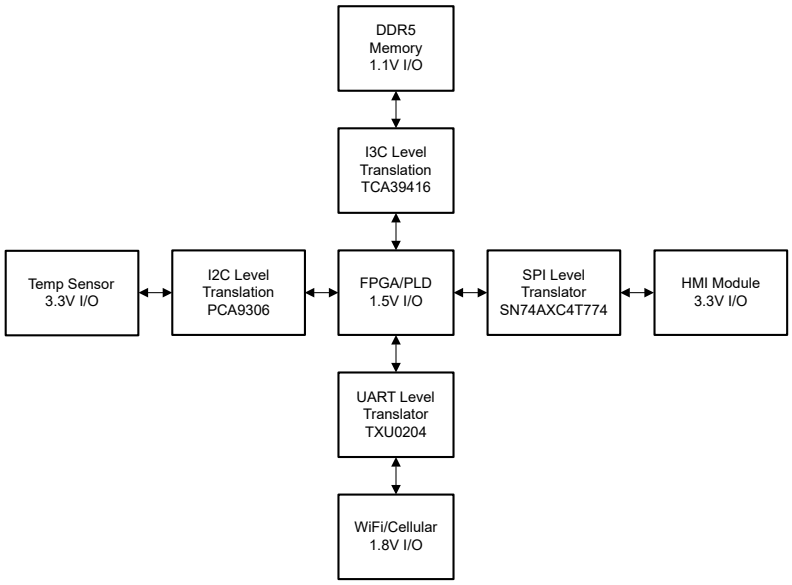

Figure 1. Potential FPGA to Peripheral I/Os Requiring Level Translation

For systems designers, increasing the FPGAs, I/O voltage require increasing the core voltage of the entire FPGA or a significant portion to a higher level resulting in higher overall power dissipation. If only a few of the FPGAs I/Os have I/O level mismatches, this increases the overall power envelope of the entire FPGA. One design that enables system designers to maintain the FPGAs lower core voltage and resolve I/O level mismatches is to use simple voltage level translator devices.

Level translation devices provide system designers a simple and cost-effective design for resolving the systems I/O level mismatch challenges without having to compromise on performance, power, or size. Integrated level shifting designs are available in a wide assortment of I/O types, bit widths, data rate ranges, current drive capabilities, and package options. Texas Instruments' portfolio of level shifter devices contains many different types of level translation functions that collectively can address almost any application requirement. TI's level translation portfolio includes auto directional, direction controlled, and fixed direction level translators in industrial, automotive, and enhanced ratings.

For a list of recommended level translation devices for common interface types, see Table 1. Table 2 lists common FPGA families and target I/O levels that are often recommended for designed for power dissipation and the different interfaces supported by each family of devices that must be level shifted. For more information on all of TI's level translation designs, see *Voltage Translators & Level Shifters*.

Table 1. Recommended Translator by Interface

Translation Level		
Interface	**Up to 3.6V**	**Up to 5.5V**
FET Replacement	2N7001T	SN74LXC1T45 / TXU0101
1 Bit GPIO/Clock Signal	SN74AXC1T45	SN74LXC1T45 / TXU0101
2 Bit GPIO	SN74AXC2T245	SN74LXC2T45 / TXU0102
2-Pin JTAG/UART	SN74AXC2T45	SN74LXC2T45 / TXU0202
I2C/MDIO/SMBus	TXS0102 / LSF0102 / PCA9306	TXS0102 / LSF0102 / PCA9306
I3C	TCA39416	TCA39416
4-Bit GPIO	SN74AXC4T245	TXB0104 / TXU0104
UART	SN74AXC4T245	TXB0104 / TXU0204
SPI	SN74AXC4T774 / TXB0104	TXB0104 / TXU0304
JTAG	SN74AXC4T774 / TXB0104	TXB0104 / TXU0304
I2S/PCM	SN74AXC4T774 / TXB0104	TXB0104 / TXU0204
Quad-SPI	TXB0106	TXB0106
SDIO/SD/MMC	TXS0206 / TWL1200	N/A
8-Bit GPIO/RGMII	TXV0108/ TXV0106	SN74LXC8T245

Table 2. Common FPGA Families and Typical Vcc I/O

Vendor	Family	Typical Vcc I/O	Common Interfaces
Intel® Altera®	Arria-10-GT®	1.2V	SPI, QSPI, I2C, RGMII, UART, GPIO, LVDS
Intel® Altera®	Arria-10-GX®	1.2V	SPI, QSPI, I2C, RGMII, UART, GPIO, LVDS
Intel® Altera®	Arria-II®	1.2V / 1.8V	SPI, I2C, JTAG, LVDS, PECL, GPIO
Intel® Altera®	Arria-V-GT®	1.2V	SPI, QSPI, I2C, UART, GPIO, JTAG, LVDS, BLVDS, LVPECL
Intel® Altera®	Arria-V-GX®	1.2V	SPI, QSPI, I2C, UART, GPIO, JTAG, LVDS, BLVDS, LVPECL
Intel® Altera®	Cyclone II®	1.5V	SPI, I2C, UART, GPIO, JTAG, LVDS, RGMII, LVDS, LVPECL
Intel® Altera®	Stratix-10-GX®	1.8V	SPI, I2C, RGMII, JTAG, LVDS, LVPECL, GPIO
Intel® Altera®	Stratix®	1.5V	SPI, I2C, RGMII, RMII, GPIO, JTAG
Lattice®	ECP2®	1.2V	SPI, JTAG, LVDS, I2C
Lattice®	LFXP2®	1.2V	SPI, JTAG, LVDS, I2C
Microsemi®	ProASIC3®	1.5V	SPI, I2C, JTAG, LVDS, MLVDS, BLVDS
AMD® Xilinx®	Artix-7®	1.8V	SPI, BLVDS, LVDS, I2C, JTAG, RGMII, UART, GPIO
AMD® Xilinx®	Kintex-7®	1.2V/1.35V/1.5V	SPI, BLVDS, LVDS, I2C, JTAG, GPIO
AMD® Xilinx®	Kintex Ultra®	1V/1.2V/1.35V/1.5V/1.8V	SPI, BLVDS, LVDS, I2C, JTAG, UART, GPIO
AMD® Xilinx®	Spartan-3A®	1.2V	SPI, LVDS, I2C, JTAG, UART, GPIO
AMD® Xilinx®	Virtex-5®	1.2V	SPI, BLVDS, LVDS, I2C, JTAG, UART, GPIO
AMD® Xilinx®	Virtex-6®	1.2V/1.8V	SPI, BLVDS, LVDS, I2C, JTAG, UART, GPIO
AMD® Xilinx®	Virtex-Ultra®	1V/1.2V	SPI, BLVDS, LVDS, I2C, JTAG, RGMII, UART, GPIO
AMD® Xilinx®	Zynq-7000®	1.2V	SPI, I2C, UART, SDIO, RGMII, JTAG, GPIO
AMD® Xilinx®	Zynq-Ultra®	1.5V	SPI, QSPI, I2C, UART, SDIO, RGMII, JTAG, GPIO

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