*Product Overview*

# *Enabling System on Module and Industrial PC Connectivity With Level Translation*

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The ability to apply machine learning and artificial intelligence algorithms at the edge of computing and electronic system environments is more important today than ever before. Processing videos, images, audio, and other sensor data and then acting on that data at the edge enables higher performance more resilient systems. Bringing processing to the edge is enabling applications to take advantage of technologies such as real-time machine vision, audio transcription, video analytics and many others. One key enabling technology for bringing processing to the edge are System on Modules (SoMs) or Computer of Module (CoMs) Industrial Personal Computers (IPC). SoMs and CoMs are part of a broader category of computing platforms known as single board computers. Systems designers can leverage SoM and CoM modules to implement high performance embedded computing solutions. SoMs are essentially entire computer systems that are built in credit card sized or smaller form factor modules. The small size and low power dissipation of SoMs enables systems designers to bring processing power closer to the edge without having to sacrifice system form factors, processing density, or power budgets. SoMs are extremely popular within industrial applications spaces given the wide selection of SoM and CoM module offerings the market provides. What makes SoMs and CoMs especially versatile is the wide array of system interfaces that are supported by them. The large assortment of I/O (Input/Output) interface types enables SoMs to communicate with many different types of external peripheral devices that are likely to be used in an end application (see Figure 1).

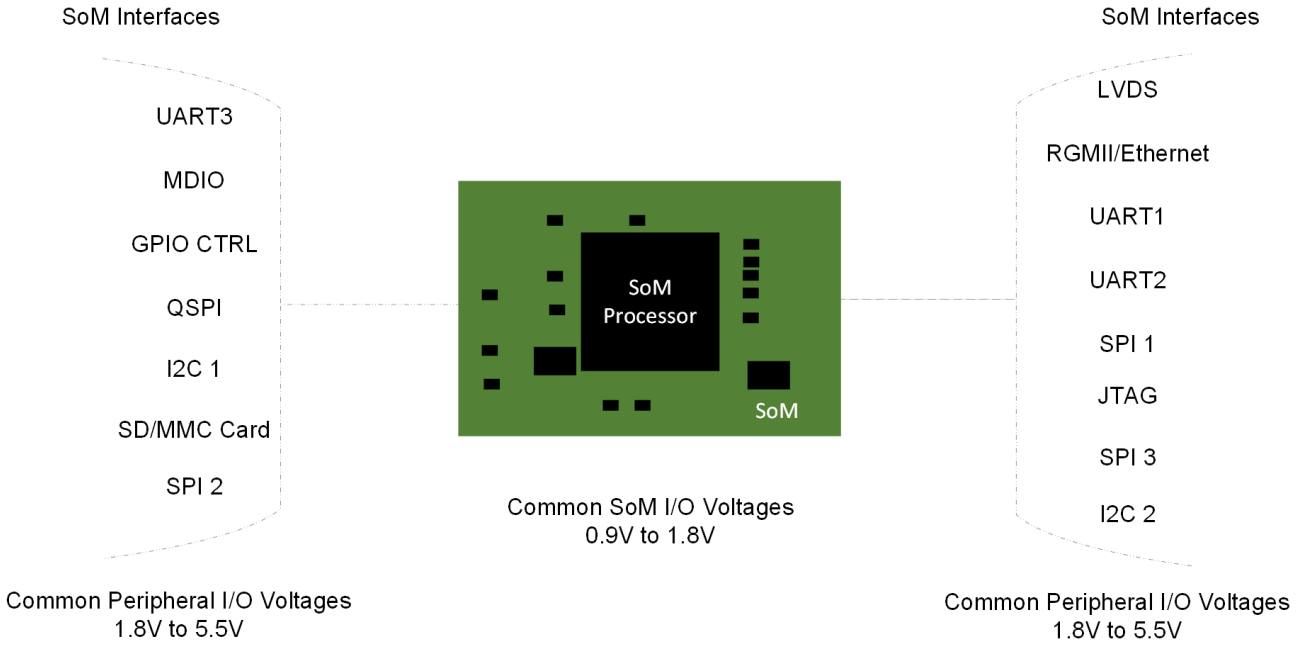


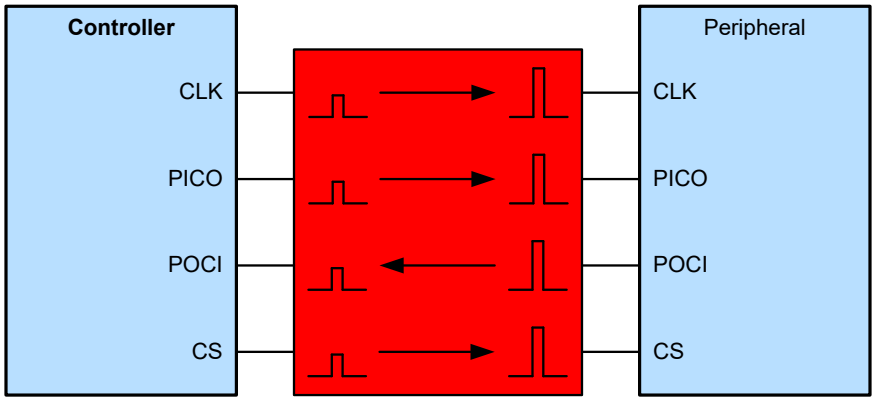

**Figure 1. Common SoM and Industrial PC I/O Interfaces**

As the core processor devices that make up the SoM move down the silicon process curve, their core voltages also scale downward in order keep power dissipation reasonable while keeping heat dissipation manageable. The lower core voltages of SoM components also limits the I/O voltage that the SoM interfaces can operate at. The lower I/O voltages of new SoMs and CoMs presents a design challenge to design engineers who often need to interface these modules with peripheral devices operating at higher I/O voltages. One solution that system designers can use to resolve I/O level mismatches between SoM and peripheral device I/Os is to use I/O level shifter devices. Integrated I/O level translation solutions are available in a wide assortment of I/O types, bit widths, data rate ranges, current drive capabilities, and package options. Figure 1 shows common interfaces that are supported by mainstream SoMs while Table 1 shows recommended level translation solutions for level shifting between the different SoM and peripheral device I/O types. Texas Instruments' portfolio of level shifter devices contains many different types of level translation functions that collectively is able to address almost any application requirement. TI's level translation portfolio includes Auto Directional, Direction Controlled, and Fixed Direction level translators in Industrial, Automotive and Enhanced ratings. The sections below provide level translation recommendations for the most common interface types such as SPI, I2C, and UART. For more information on TI's level translation devices, see the level translation landing page on ti.com.

**Table 1. Recommended Translator by Interface**

| Interface | Translation Level | | Small Package Option |
|---|---|---|---|
| | Up to 3.6 V | Up to 5.5 V | |
| FET Replacement | 2N7001T | SN74LXC1T45 / TXU0101 | DPW, DTQ |
| 1 Bit GPIO/Clock Signal | SN74AXC1T45 | SN74LXC1T45 / TXU0101 | DTQ |
| 2 Bit GPIO | SN74AXC2T245 | SN74LXC2T45 / TXU0102 | DTM |
| 2-Pin JTAG/UART | SN74AXC2T45 | SN74LXC2T45 / TXU0202 | DTM |
| I2C/MDIO/SMBus | TXS0102 / LSF0102 | TXS0102 / LSF0102 | DQE, DQM |
| IC-USB | SN74AVC2T872 / TXS0202 | NA | YZP |
| 4 Bit GPIO | SN74AXC4T245 | TXB0104 / TXU0104 | BQB, DTR |
| UART | SN74AXC4T245 | TXB0104 / TXU0204 | BQB, DTR |
| SPI | SN74AXC4T774 / TXB0104 | TXB0104 / TXU0304 | BQB, RUT |
| JTAG | SN74AXC4T774 / TXB0104 | TXB0104 / TXU0304 | BQB, RUT |
| I2S/PCM | SN74AXC4T774 / TXB0104 | TXB0104 / TXU0204 | BQB, RUT |
| Quad-SPI | TXB0106 | TXB0106 | RGY |
| SDIO/SD/MMC | TXS0206 / TWL1200 | NA | YFP |
| 8 Bit GPIO/RGMII | SN74AXC8T245 | SN74LXC8T245 | RJW, RHL |

## Translate Voltages for SPI




**Example SPI Voltage Translation Block Diagram**

See more about this use case in the *Logic Minute* video *Voltage Translation for SPI*.

## Design Considerations

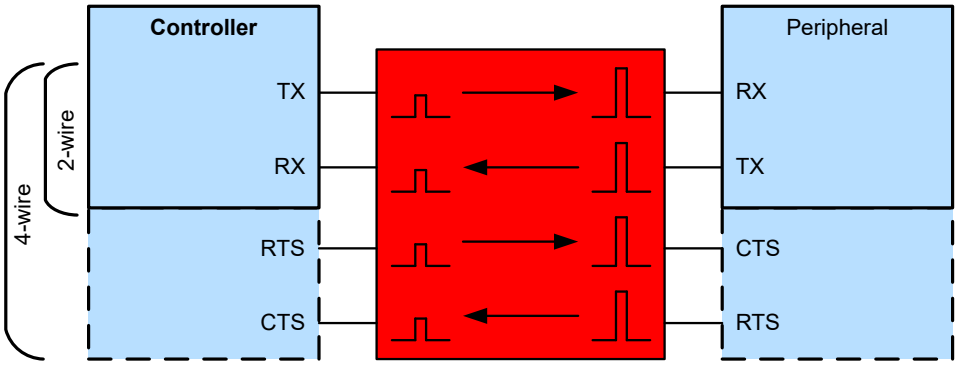
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

## Recommended Parts

| Part Number | AEC-Q100 | Voltage Translation Range | Features |
|---|---|---|---|
| TXU0304 | | 1.1 V–5.5 V | Schmitt-trigger inputs<br>Integrated pulldown resistors<br>$V_{CC}$ Isolation and $V_{CC}$ Disconnect |
| TXU0304-Q1 | ✓ | | |
| SN74AXC4T774 | | 0.65 V–3.6 V | Direction controlled<br>Glitch-free power supply sequencing<br>$V_{CC}$ Isolation |
| SN74AXC4T774-Q1 | ✓ | | |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for UART




**Example UART Voltage Translation Block Diagram**

See more about this use case in the *Logic Minute* video *Voltage Translation for UART*.

## Design Considerations

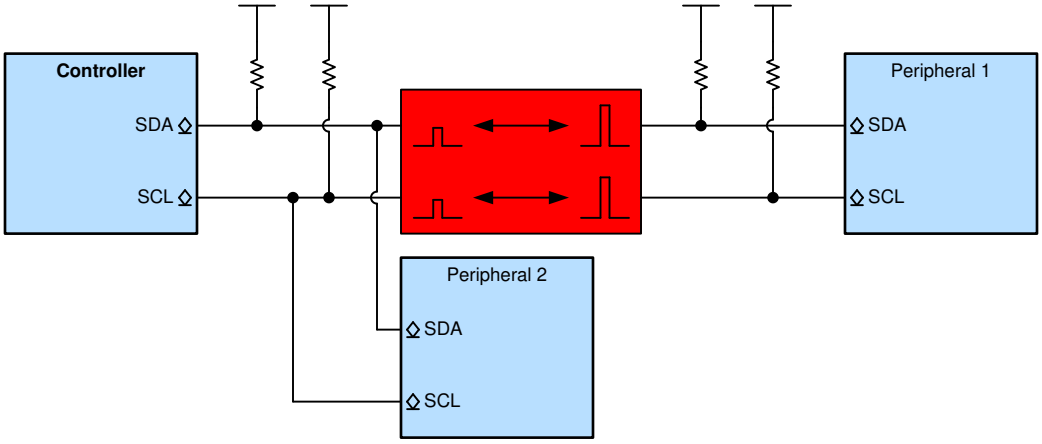
- Some devices support up to 5 Mbps UART communication; most are limited to 115 kbps or less
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

## Recommended Parts

| Part Number | AEC-Q100 | Supported UART Topology | Voltage Translation Range | Features |
|---|---|---|---|---|
| TXU0204 | | 2-wire and 4-wire | 1.1 V–5.5 V | Schmitt-trigger inputs<br>Integrated pulldown resistors<br>$V_{CC}$ Isolation and $V_{CC}$ Disconnect |
| TXU0204-Q1 | ✓ | | | |
| SN74AXC2T245 | | 2-wire | 0.65 V–3.6 V | Direction controlled<br>Glitch-free power supply sequencing<br>$V_{CC}$ Isolation |
| SN74AXC2T245-Q1 | ✓ | | | |
| SN74AXC4T245 | | 2-wire and 4-wire | | |
| SN74AXC4T245-Q1 | ✓ | | | |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for I²C




**Example of Using Voltage Translation With an I²C Communication Bus**

## Design Considerations

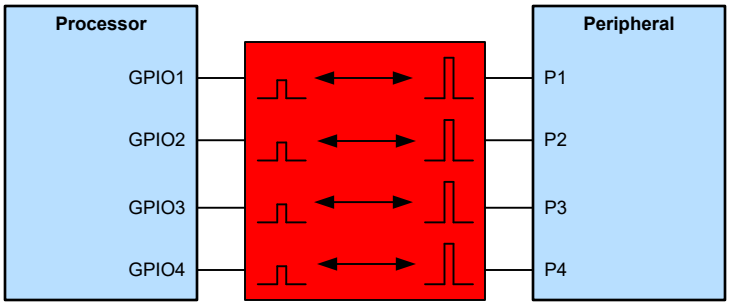
- Typical data rates can range from 100 kpbs – 3.4 Mbps
- Certain I²C modes have minimum rise time requirements that may be violated due to the edge-rate acceleration feature in the TXS family
- Enable communication when devices have mismatched logic voltage levels.
- Prevent damage to devices that cannot support higher voltage inputs.
- Improve data rates over discrete translation solutions.
- [FAQ] Why are the TXS01xx VIH/VIL specifications so stringent?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*.

## Recommended Parts

| Part Number | AEC-Q100 Qualified | Voltage Translation Range | Features |
|---|---|---|---|
| LSF0102 | | 0.95 V – 5 V | Over-voltage tolerant I/O<br>Low $R_{ON}$ for less signal distortion |
| LSF0102-Q1 | ✓ | | |
| TXS0102 | | 1.65 V – 5.5 V | Edge-rate acceleration<br>Supports Partial-Power-Down applications<br>Integrated pull-up resistors |
| TXS0102-Q1 | ✓ | | |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for GPIO




**Example GPIO Voltage Translation Block Diagram**

## Design Considerations

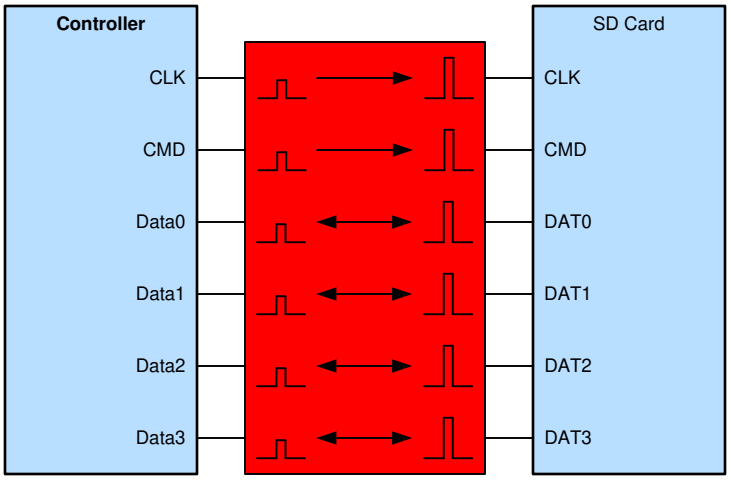
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] What are the power sequencing requirements for the translation device?
- [FAQ] What should be done with unused I/O pins of the level translator devices?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

## Recommended Parts

| Part Number | AEC-Q100 | Bits | Voltage Translation Range | Features |
|---|---|---|---|---|
| SN74LXC8T245 | | 8 | 1.1 V–5.5 V | Schmitt-trigger inputs<br>Dynamic pulldowns on I/O<br>$V_{CC}$ Isolation and $V_{CC}$ Disconnect |
| SN74LXC8T245-Q1 | ✓ | | | |
| TXU0104 | | 4 | 1.1 V–5.5 V | Schmitt-trigger inputs<br>Integrated pulldown resistors<br>$V_{CC}$ Isolation and $V_{CC}$ Disconnect |
| TXU0104-Q1 | ✓ | | | |
| SN74AXC2T45 | | 2 | 0.65 V–3.6 V | Direction controlled<br>Glitch-free power supply sequencing<br>$V_{CC}$ Isolation |
| SN74AXC2T45-Q1 | ✓ | | | |
| SN74AXC1T45 | | 1 | | |
| SN74AXC1T45-Q1 | ✓ | | | |

For more devices, browse through the *online parametric tool* where you can choose between the three types of translators.

## Translate Voltages for SDIO




**Example of Using Voltage Translation With an SD Card Communication Bus**

## Design Considerations

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while SD Card is not connected
- [FAQ] Are there voltage level translation / level shifter device recommendations for the industry standard interfaces like GPIO, SPI, UART, I2C, MDIO, RGMII, I2S?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

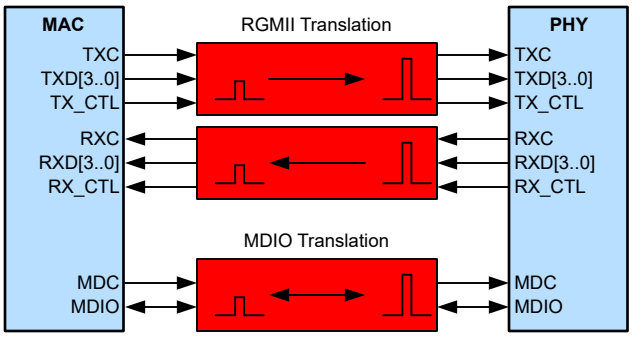
## Recommended Parts

| Part Number | Voltage Translation Range | Maximum Data Rate (Mbps) | Features |
|---|---|---|---|
| TXS02612 | 1.1 V–3.6 V | 120 | Enables a single SDIO port to be interfaced with two SDIO peripherals<br>8-kV System-level (IEC 61000-4-2) ESD protection |
| TXS0206 | 1.1 V–3.6 V | 60 | Auto-bidirectional<br>Integrated EMI Filtering<br>8-kV System-level (IEC 61000-4-2) ESD protection |
| TXS0206-29 | 1.1 V–3.6 V | 60 | Auto-bidirectional<br>Integrated 2.9 V LDO regulator<br>8-kV System-level (IEC 61000-4-2) ESD protection |
| SN74AVCA406 | 1.2 V–3.6 V | 52 | MMC, SD, Memory Stick, Smart Media, and XD-Picture Card Voltage Translation Transceiver<br>15-kV System-level (IEC 61000-4-2) ESD protection |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for RGMII

RGMII is a high-bandwidth data bus protocol with very strict timing considerations. The following device recommendations are provided as a suggested solution as they can support the data rates required for RGMII interfaces; however, because the RGMII specification is defined without consideration for voltage level translation, board-level assessment of key timing parameters and assessment of performance within the system is encouraged.




**Example of Using Voltage Translation With RGMII**

## Design Considerations

- Board layout is critical to the success of RGMII translation; we recommend using signal integrity simulations and prototyping for any design
- Use active translators for maximum data rate
- Use one device for all TX signals and one for all RX signals to minimize channel-to-channel skew
- See *Low Voltage Translation For SPI, UART, RGMII, JTAG Interfaces* for details regarding the performance of SN74AXC8T245 in RGMII applications
- Place translators closest to the low-voltage device, if possible, to improve signal integrity
- Consider source-terminating signals if sent over 12 cm (4700 mil) or longer traces
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

## Recommended Parts

| Part Number | Automotive Qualified | RGMII Voltage Translation Range | Device Maximum Data Rate (Mbps) | Features |
|---|---|---|---|---|
| SN74AXC8T245 | | 2.5 V to 3.3 V | 380 Mbps | Glitch-free power supply sequencing<br>Outputs are disabled when either supply is 0 V<br>Active translation architecture |
| SN74AXC8T245-Q1 | ✓ | | | |
| SN74AVC8T245 | | 1.8 V to 3.3 V | 320 Mbps | Active translation architecture |
| SN74AVC8T245-Q1 | ✓ | | | |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for MDIO

Management Data Input or Output (MDIO) is a control protocol designed primarily for use with ethernet PHY devices. It typically utilizes an unidirectional 2.5 MHz clock signal (MDC) and bidirectional data bus line (MDIO). For details on the accompanying RGMII translation, see *Translate Voltage for RGMII*.

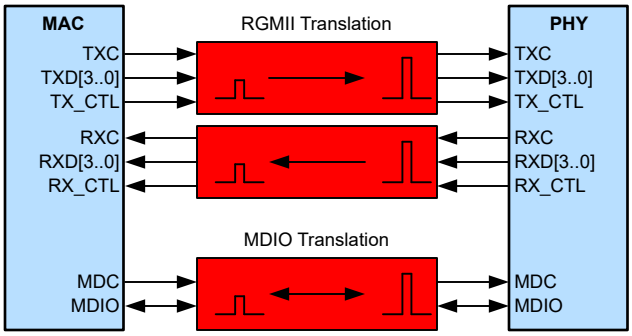



**Figure 8. Example MAC to PHY Voltage Translation Block Diagram**

See more about auto-bidirectional voltage translation in *Translation Between Communication Modules and System Controllers*

## Design Considerations

- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Use a fixed-direction translator for the clock (MDC) if higher speeds are required; some newer devices use a clock as high as 50 MHz
- Open-drain compatible translators are required for the data line; although the protocol is not open-drain, pull-up resistors are required on the MDIO signal bus because there are times when the bus is not actively driven
- See answers to our most frequently asked technical questions on *[FAQ] Voltage Translators*
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

## Recommended Parts

| Part Number | AEC-Q100 Qualified | Voltage Translation Range | Features |
|---|---|---|---|
| SN74AXC1T45 | | 0.65 V – 3.6 V | Glitch-free power supply sequencing<br>Outputs are disabled when either supply is 0 V<br>Active translation architecture<br>Up to 500 Mbps for 1.8 V to 3.3 V translation |
| SN74AXC1T45-Q1 | ✓ | | |
| TXS0102 | | 1.65 V – 5.5 V | Auto-bidirectional<br>Open-drain compatible<br>Integrated pull-up resistors |
| TXS0102-Q1 | ✓ | | |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

## Translate Voltages for a SIM Card

Subscriber Identity Modules, commonly called SIM cards, are used to store secure information in mobile devices for use in communications. This type of voltage translation applies to SIM, USIM, and UICC.

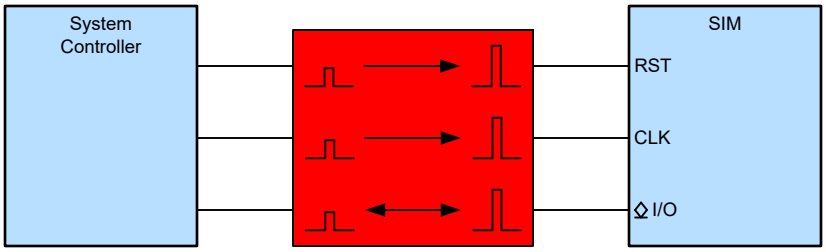



**Figure 9. Example SIM Card Voltage Translation Block Diagram**

## Design Considerations

### Design Considerations

- Clock signals can be up to 5 MHz
- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- [FAQ] How does a slow or floating input affect a CMOS device?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

**Table 2. Recommended Parts**

| Part Number | Automotive Qualified | Supported Card Types | | | Features |
|---|---|---|---|---|---|
| | | Class A 5 V | Class B 3 V | Class C 1.8 V | |
| TXS0104E | | ✓ | ✓ | ✓ | Auto-bidirectional voltage translation for all channels<br>Supports all voltages and frequencies for SIM/UICC<br>Increased ESD protection on B ports |
| TXS0104E-Q1 | ✓ | ✓ | ✓ | ✓ | |
| TXS4555 | | | ✓ | ✓ | Complete SIM/UICC translator solution<br>Integrated LDO regulator<br>Increased ESD protection on card-side |
| TXS02326A | | | ✓ | ✓ | Complete dual SIM/UICC translator and multiplexer solution<br>Dual integrated LDO regulators<br>$I^2C$ communication with baseband processor<br>Increased ESD protection on card-side |

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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