

Using TPS65086x PMIC to Power Xilinx® Zynq® UltraScale+® MPSoCs



ABSTRACT

This application note provides the four variants of the TPS65086x power management IC (PMIC) that power the Xilinx® Zynq® UltraScale+® line of MPSoCs. The report outlines the benefits of the TPS65086x line of PMICs and includes a selection guide for comparing the four variants. Then, example power maps are provided for each of the four Xilinx Zynq UltraScale+ configurations.

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1 Introduction

Xilinx's Zynq UltraScale+ MPSoC line offers a high level of flexibility, with a range of devices that scale in complexity to suit a wide variety of applications. As such, the solutions that power the Zynq UltraScale+ must be equally adaptable to meet the power needs of a complex line.

This application note reviews four different variants of TI's TPS65086x power management IC (PMIC) used to power the Zynq UltraScale+ (ZU+) line to provide a selection guide for comparing the different variants. The report also covers the value the TPS65086x PMICs bring to the overall system, and provide example power maps for each of the four main ZU+ power configurations.

2 TPS65086x Overview

The TPS65086x PMICs integrate 3 buck converters, 3 buck controllers, 4 LDOs, and 3 load switches in a small 8 mm × 8 mm VQFN package. The buck controllers allow customers to tailor their TPS65086x solution to the specific current needs of their system, which minimizes BOM size and cost. The integrated load switches enable extremely flexible power sequencing, allowing TPS65086x to fulfill the power requirements of the ZU+ line without external sequencers. The QFN package provides enhanced thermal performance at higher loads and simplifies routing, which reduces manufacturing time and cost. The TPS65086x also features the widest input voltage range on the market, from 5.6–21 V, which allows TPS65086x to support a variety of end applications across multiple battery types. The TPS65086x also supports the largest range of ZU+ devices, from ZU2CG all the way through ZU19EG. For more information on the different ZU+ devices, please refer to the [Xilinx Zynq UltraScale+ site](#).

Furthermore, the TPS65086x family offers both pre-programmed and user-programmable variants to power the ZU+ family. The three pre-programmed variants simplify the design process for basic use cases, allowing you to directly implement the given power configuration with no modifications needs. For more unique power requirements, the user programmable variant gives you the freedom to fully customize the power solution to fit your system needs.

3 TPS65086x Variants

In total, there are four variants of the TPS65086x PMIC for the Zynq UltraScale+, as shown in [Table 3-1](#).

Table 3-1. TPS65086x Variant Voltage Comparison

	Programmability	Buck 1	Buck 2 ¹	Buck 3 ¹	Buck 4	Buck 5	Buck 6 ¹	LDOA1	LDOA2	LDOA3
TPS6508640	Pre-programmed	3.3 V	0.85, 0.9 V	1.2 V	0.9 V	1.8 V	1.2, 1.35 V	2.5 V	1.5 V	1.2 V
TPS65086401	Pre-programmed	1.8 V	0.85 V	0.85 V	3.3 V	3.3 V	1.1, 1.2, 1.5 V	1.8 V	1.2 V	1.2 V
TPS6508641	Pre-programmed	External Feedback	0.85 V	1.1, 1.2 V	3.3 V	1.2 V	1.8V	1.8 V	1.2V	1.2V
TPS650861	User programmable	0.41 - 3.575 V						1.35-3.3 V	0.7 - 1.5 V	

1. Multiple voltages may be available through pin strapping; if so, they are separated with a comma.

The first three variants in the table are pre-programmed, varying in their set voltages and sequencing to match the different Xilinx ZU+ MPSoC specifications. The different MPSoCs each variant supports are outlined in the next section. The fourth, the TPS650861 (also denoted TPS65086100), is the user-programmable *DIY* version, and will be discussed in greater detail in [Section 5](#). All four variants share the same current capabilities, which are shown in [Table 3-2](#).

Table 3-2. TPS65086x Current Specifications

Buck 1	Buck 2	Buck 3	Buck 4	Buck 5	Buck 6	LDOA1	LDOA2	LDOA3
Scalable	Scalable	3.0 A	3.0 A	3.0 A	Scalable	0.2 A	0.6 A	0.6 A

For more information, please see the [TPS650864](#) and [TPS650861](#) data sheets.

4 TPS65086x Selection Guide

[Table 4-1](#) details a selection guide for choosing between the four TPS65086x variants. The choice depends both on the desired power configuration as well as the exact device used. Due to its configurability, the TPS650861 user programmable variant provides the greatest coverage across all speed grades and devices, while the pre-programmed variants offer pre-programmed voltages and sequencing for greatest convenience.

Table 4-1. TPS65086x Xilinx® ZU+ MPSoC Selection Guide

		TPS6508640	TPS65086401	TPS6508641	TPS650861
Always On: Power and Efficiency Optimized (-1L, -2L)	ZU2CG - ZU9EG ¹	X	✓*	✓*	✓ or ✓*
	ZU11EG - ZU19EG	X	✓*	✓*	✓ or ✓*
Always On: Cost Optimized (-1, -2)	ZU2CG - ZU9EG ¹	✓	✓	✓	✓ or ✓*
	ZU11EG - ZU19EG	X	✓*	✓*	✓ or ✓*
Always On: PL Performance Optimized (-3)	ZU2CG - ZU9EG ¹	✓	X	X	✓ or ✓*
	ZU11EG - ZU19EG	✓*	X	X	✓ or ✓*
Full Power Domain Flexibility (-1L, -2L, -1, -2, -3)	ZU2CG - ZU9EG ¹	X	X	✓	✓ or ✓*
	ZU11EG - ZU19EG	X	X	✓*	✓ or ✓*

1. Range includes all CG devices, all EV devices, and ZU2-ZU9 EG

- ✓ – covered by TPS65086x
- ✓* – covered by TPS65086x + discrete buck
- X – not covered

5 TPS650861 Programming Information

The user-programmable TPS650861 has two banks of one-time programmable (OTP) memory that allow you to fully customize the output voltages, sequencing, GPIO control, and more to best meet your system needs. The entire programming process is outlined in the [TPS65086100 Non-Volatile Memory Programming Guide](#). Other resources to support the TPS650861 programming process include:

- The [TPS65086100 OTP Generator](#) takes in your specific requirements and then automatically generates the I²C commands needed to program the TPS650861.
- The [BOOSTXL-TPS650861 BoosterPack™](#), which enables custom programming of the OTP memory of the TPS650861 for rapid prototyping and quicker time to market.
- The [BOOSTXL-TPS650861 EVM User's Guide](#), which provides a guideline to program the OTP memory of the TPS650861 using BOOSTXL-TPS650861 BoosterPack™, an [MSP430F5529 LaunchPad™ development kit](#), and [IPG-UI EVM GUI software](#).
- [Training videos](#) on TI.com that provide an overview and step through the DIY PMIC programming process.

When generating a custom OTP file for programming, TI recommends starting with one of the template OTP files from the TPS650864x pre-programmed variants if only modifying a few rails. These pre-programmed OTP Generator files are available on the TPS650861 product folder, under the [Design and development](#) section.

6 Example Power Maps

The following sections provide an example power map for each of the four Xilinx power configurations outlined in [Table 4-1](#). For each configuration, both a pre-programmed variant and the user-programmable TPS650861 can be used.

For more information on the power configurations and rail consolidations, please refer to [Xilinx Zynq UltraScale+ and UltraScale Architecture PCB Design](#).

6.1 Always On: Power and Efficiency Optimized (-1L and -2L devices)

Figure 6-1 shows an example power map for the Power and Efficiency Optimized configuration. The rails shown follow the settings of the pre-programmed TPS6508641; however, as discussed in Section 5, the TPS650861 can also be used in this configuration.

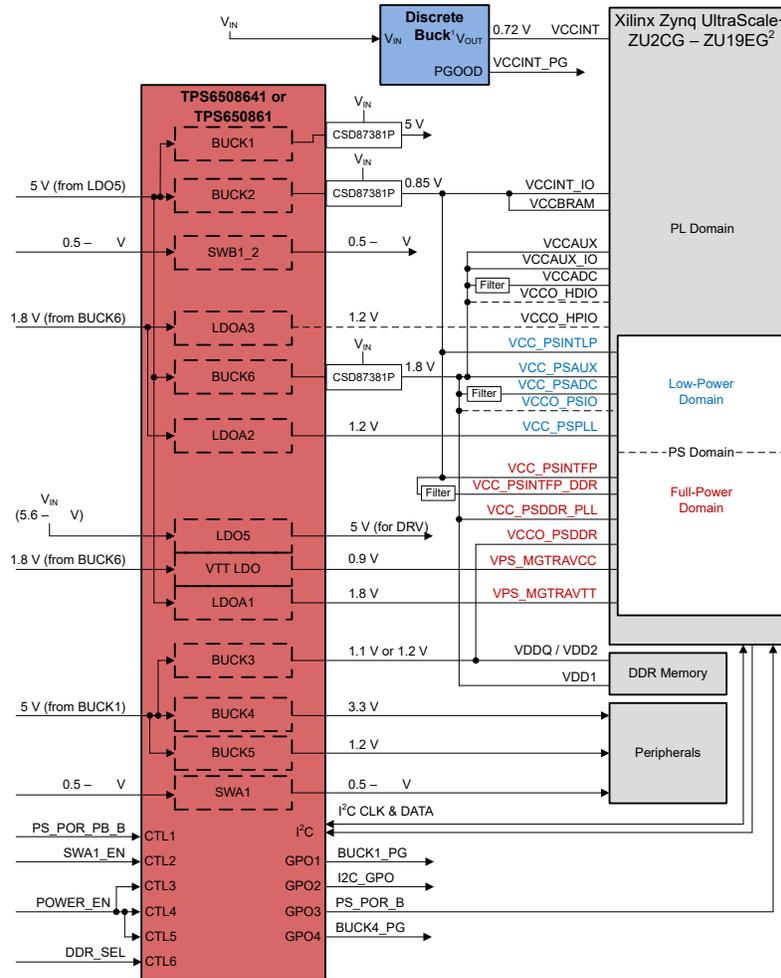


Figure 6-1. Always On, Power and Efficiency Optimized Power Map Using the TPS6508641 or TPS650861

1. See Table 6-1 for discrete buck selection guide.
2. For EV devices: if using the TPS650861, set either Buck 4 or 5 to 0.9 V. If using the TPS6508641, add the TPS543620 discrete buck to power the VCCINT_VCU rail

Table 6-1. Discrete Buck Selection Guide

Current Range	Discrete Buck	V _{in}
3 - 6 A	TPS543620 ¹	4 - 18 V
6 - 8 A	TPS543820 ¹	4 - 18 V
8 - 15 A	TPS542A52	4 - 18 V
15 - 25 A	TPS543B20 ²	4 - 19 V
25 - 40 A	TPS543C20A ²	4 - 16 V

1. TPS543620 and TPS543820 are pin to pin compatible
2. TPS543B20 and TPS543C20A are pin to pin compatible

6.2 Always On: Cost Optimized (-1 and -2 devices)

For the next three cases, the regulator used for VCCINT and the external FET used for Buck 2 will vary depending on the exact power requirements, as shown in Figure 6-2, Figure 6-3, and Figure 6-4. For a general selection guideline based on Zynq UltraScale+ devices, see Table 6-2. Please note that several configurations can be applicable to a given device, depending on the use case.

Table 6-2. VCCINT and FET Selection Guide

Device	VCCINT Regulator	Buck 2 FET
ZU2 - ZU5 (CG, EG)	Buck 2	CSD87381P (<15 A)
ZU4 EV		
ZU6 - ZU9 (CG, EG)	Buck 2	CSD87588N (<25 A)
ZU5, ZU7 EV		
ZU11 - ZU19 (EG)	TPS543B20 (<25 A)	CSD87381P (<15 A)
	TPS543C20A (<40 A)	

Note that the external FETs on Buck 1 and 6 can also be modified depending on the load current requirements. Please see the *Selecting the FETs* section of the [TPS650864 data sheet](#) for more information on FET selection.

Figure 6-2 shows an example power map for the Power/Efficiency Optimized configuration. The rails shown follow the settings of the pre-programmed TPS6508641; however, as discussed in Section 5, the TPS650861 can also be used to power this configuration.

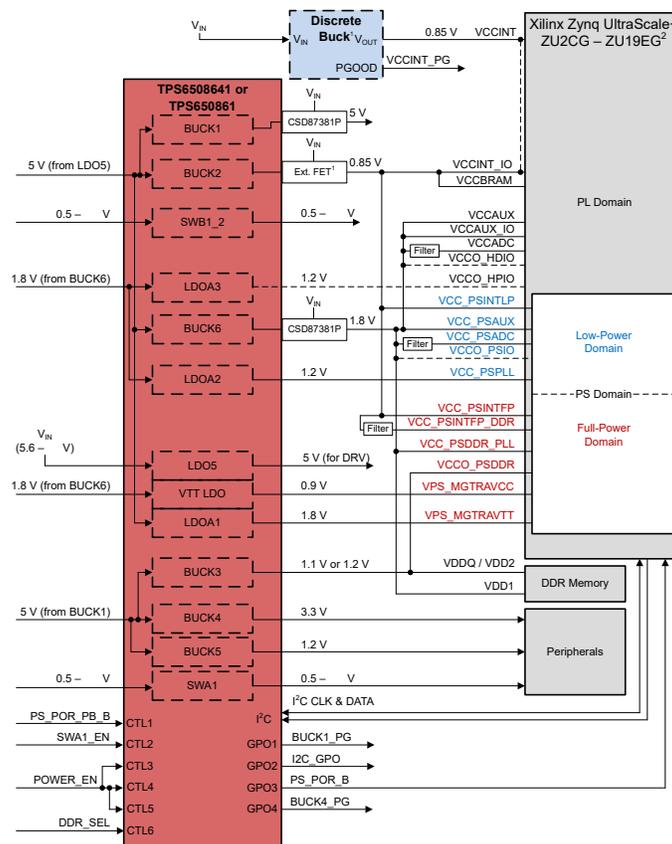


Figure 6-2. Always On, Cost Optimized Power Map Using TPS6508641 or TPS650861

1. See Table 6-2 above for VCCINT regulator and Buck 2 FET selection guide.
2. For EV devices: if using the TPS650861, set either Buck 4 or 5 to 0.9 V. If using the TPS6508641, add the TPS543620 discrete buck to power the VCCINT_VCU rail.

6.3 Always On: PL Performance Optimized (-3 Devices)

Figure 6-3 shows an example power map for the Power/Efficiency Optimized configuration. The rails shown follow the settings of the pre-programmed TPS6508640; however, as discussed in Section 5, the TPS650861 can also be used to power this configuration.

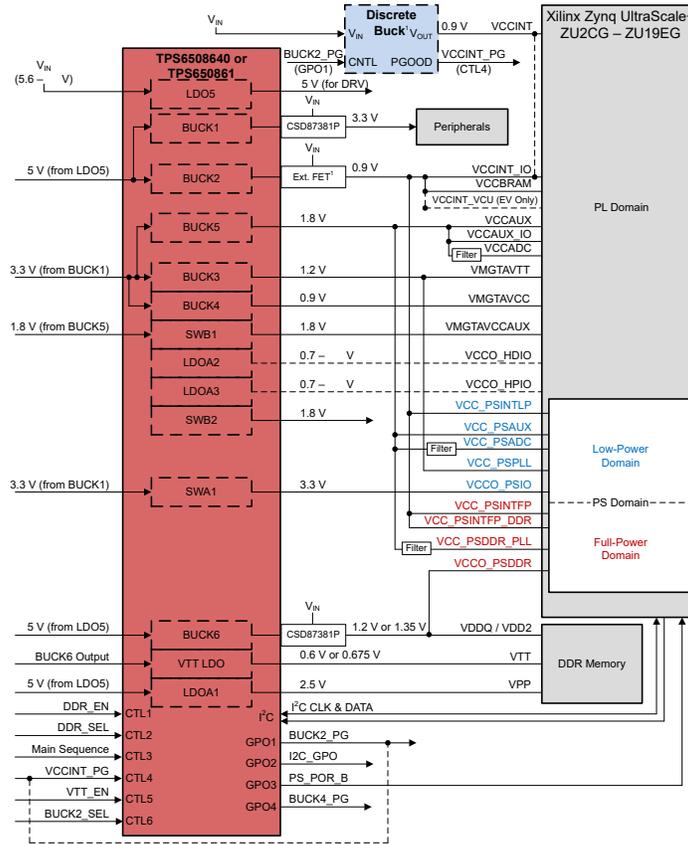


Figure 6-3. Always On, PL Domain Optimized Power Map using TPS6508640 or TPS650861

1. See Table 6-2 for VCCINT regulator and Buck 2 FET selection guide

6.4 Full Power Domain (All speed grades)

Figure 6-4 shows an example power map for the Power/Efficiency Optimized configuration. The rails shown follow the settings of the pre-programmed TPS6508641; however, as discussed in Section 5, the TPS650861 can also be used to power this configuration.

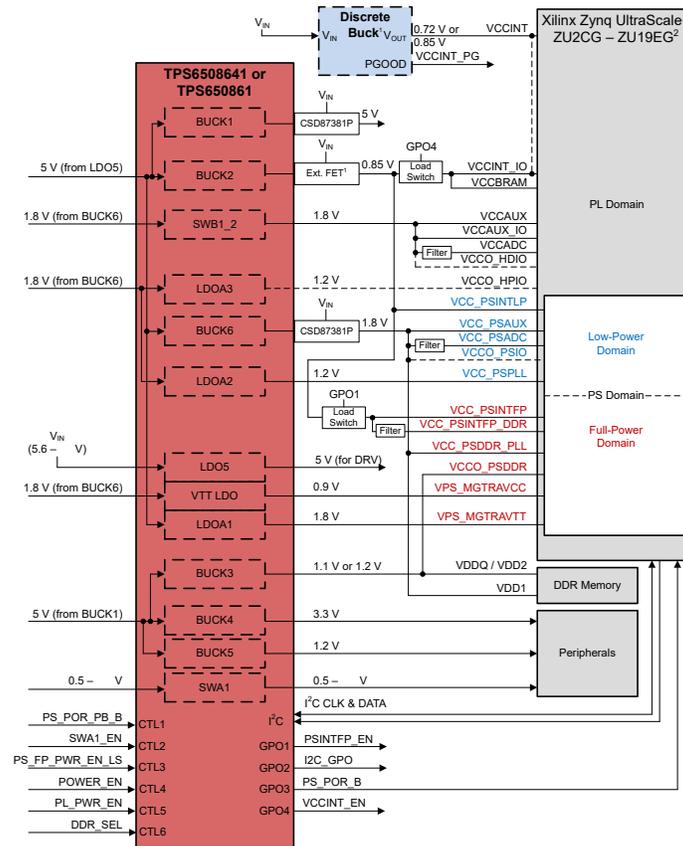


Figure 6-4. Full Power Management Flexibility Power Map using the TPS6508641 or TPS650861

1. See Table 6-2 for VCCINT regulator and Buck 2 FET selection guide.
2. For EV devices: if using the TPS650861, set either Buck 4 or 5 to 0.9 V. If using the TPS6508641, add the TPS543620 discrete buck to power the VCCINT_VCU rail.

7 Conclusion

The TPS65086x family provides four different variants to support the wide power needs and use cases of the Zynq UltraScale+ MPSoC line of Xilinx processors. Both the pre-programmed as well as user programmable variants are capable of supporting the full range of Xilinx Zynq UltraScale+ devices, translating into board and BOM cost savings. This capability, combined with our robust set of documentation makes it very easy to configure the OTP memory of the user programmable TPS650861. This programmability allows for rapid prototyping and a faster time to market, in addition to the technical benefits the entire TPS65086x PMIC family provides.

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