Application Report
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Selecting the Right Level-Translation Solution

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ABSTRACT

Supply voltages continue to migrate to lower nodes to support today's low-power, high-performance applications. While some devices are capable of running at lower supply nodes, others might not have this capability. To have switching compatibility between these devices, the output of each driver must be compliant with the input of the receiver that it is driving. There are several level-translation schemes to interface these devices with one another. Depending on application needs, one approach might be more suitable than the other. This application report gives an overview of the methods and products used to translate logic levels and lists the advantages and disadvantages of each Texas Instruments (TI) level-translation solution.

Keywords: Dual-supply, split-rail, level translation, level shifter, mixed-voltage, T45, T245, 4245, 3245, open-drain, overvoltage tolerant, TTL, CMOS, TVC, CB3T, CBTD

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1 Introduction

The need for voltage level translation is prevalent on most electronic systems today. For example, an ASIC might be operating with supply-voltage V_{CCA}, while an I/O device operates with supply-voltage V_{CCB}. To enable these devices to communicate with each other, a level-translation solution is needed as shown in Figure 1.

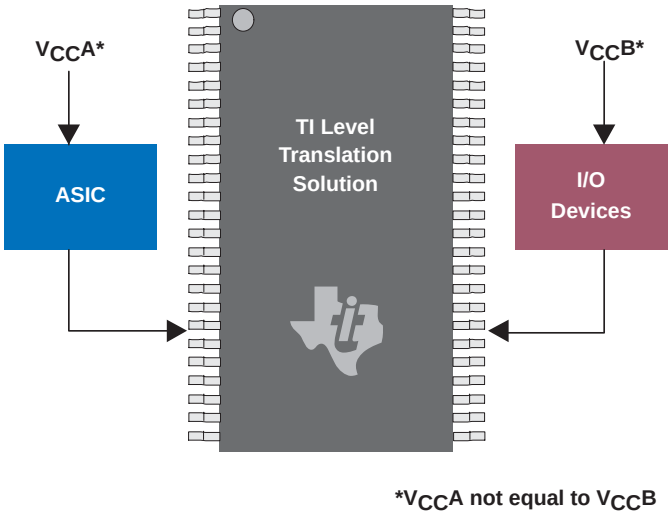

Figure 1. Typical Situation in Which a Level Translator Is Needed

Input-voltage thresholds and output-voltage levels of electronic devices vary, depending on the device technology and supply voltage used. Figure 2 shows the threshold levels for different supply voltages and device technologies. To interface two devices successfully, certain requirements must be met:

1. The V_{OH} of the driver must be greater than the V_{IH} of the receiver.
2. The V_{OL} of the driver must be less than the V_{IL} of the receiver.
3. The output voltage from the driver must not exceed the I/O voltage tolerance of the receiver.

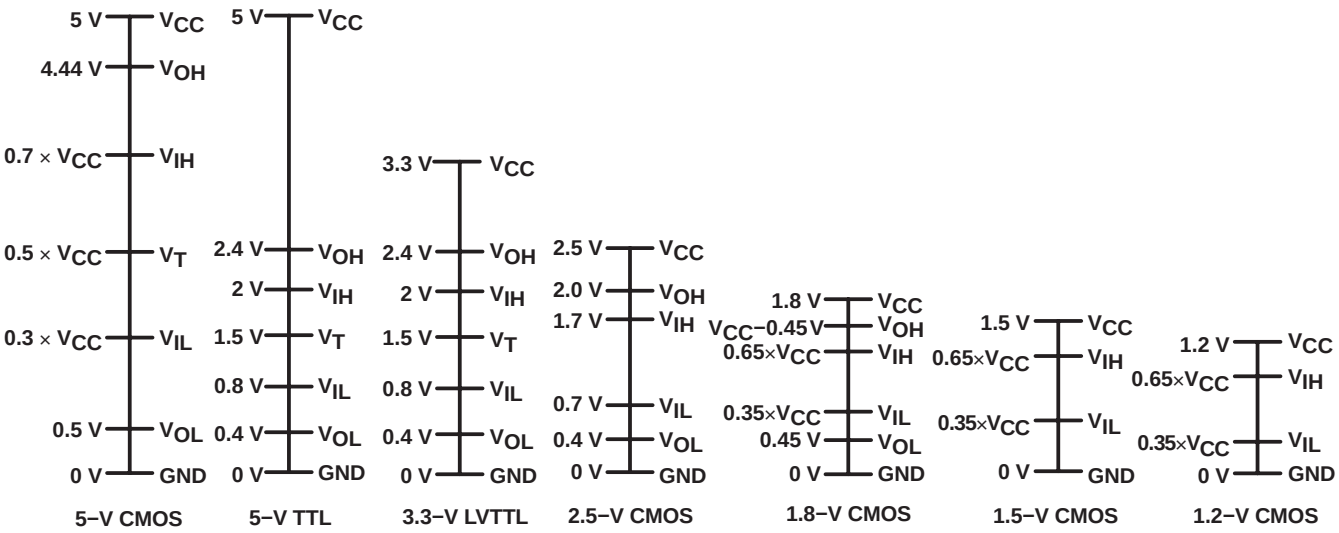

Figure 2. Digital Switching Levels

2 Dual-Supply Level Translators

2.1 Features

Dual-supply devices are designed for asynchronous communication between two buses or devices operating at different supply voltages. These devices use two supply voltages: V_{CCA} to interface with the A side and V_{CCB} to interface with the B side. For bidirectional level translators, data is transmitted from A to B or B to A, depending on the logic level at the DIR input. On devices with an output enable (OE) control input, the A and B buses effectively are isolated when OE is inactive.

Dual-supply devices from TI are available in a variety of bit widths and cover nearly every supply-voltage node in use today. These devices are flexible, easy to use, and can translate bidirectionally (up-translate and down-translate), which makes them an ideal choice for most level-translation applications. Their active current-drive capability makes them suitable for applications with long trace lengths and heavy output loads.

The SN74AVCB324245 is a 32-bit dual-supply level translator that is organized as four banks of eight bits each. Figure 3 shows one bank of the SN74AVCB324245 translating from 1.8 V to 3.3 V while, at the same time, another bank translates from 3.3 V to 1.8 V.

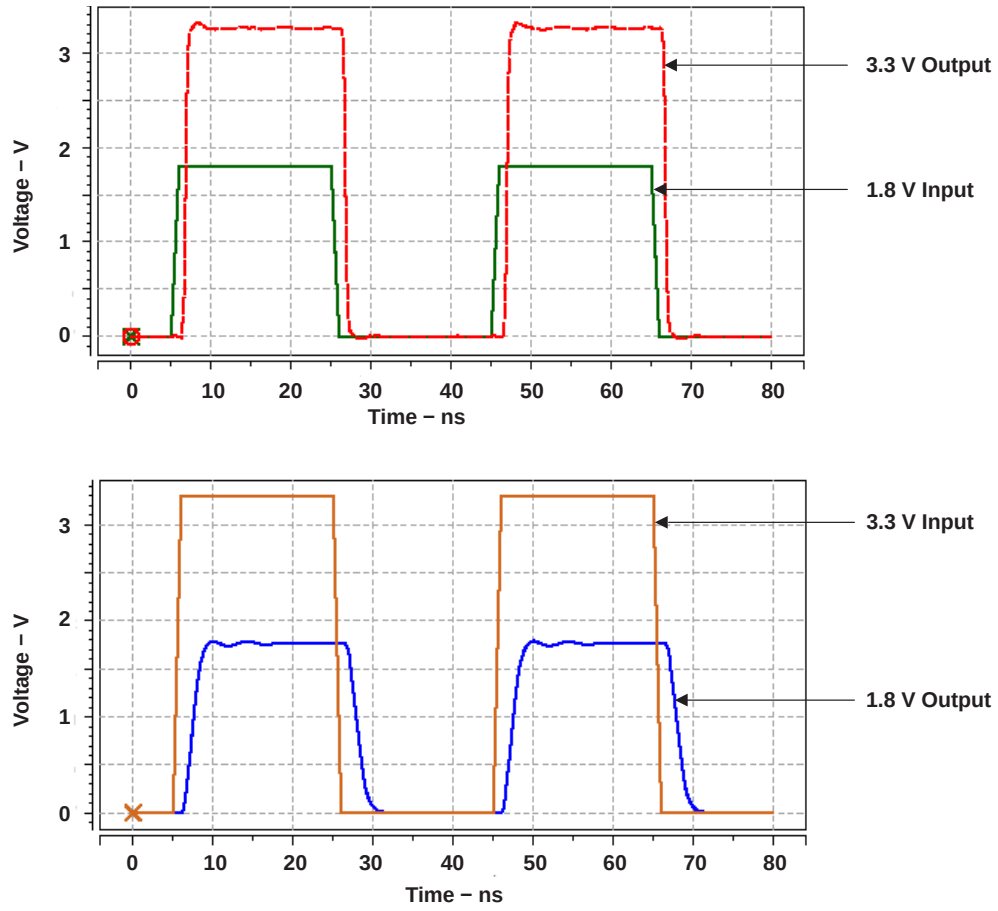

Figure 3. SN74AVCB324245 Translating From 1.8 V to 3.3 V (Bank 1) and 3.3 V to 1.8 V (Bank 2) at the Same Time (C_L = 15 pF, R_L = 2 kΩ)

Advantages of dual-supply devices:

- Flexibility in translating to/from a variety of voltage nodes
- Active current drive capability
- Available in a variety of bit widths

2.2 Product Portfolio

Table 1 summarizes TI's dual-supply device offerings.

Table 1. Possible Voltage-Translation Combinations Using Dual-Supply Translators

Device	Supply Voltage	Possible Voltage-Translation Combinations	
		A Port	B Port
SN74LVCC3245A	2.3 V ≤ V_{CCA} ≤ 3.6 V 3 V ≤ V_{CCB} ≤ 5.5 V	2.5-V CMOS	3.3-V LVTTL/LVCMOS
		3.3-V LVTTL/LVCMOS	5-V CMOS
SN74LVC4245A	4.5 V ≤ V_{CCA} ≤ 5.5 V 2.7 V ≤ V_{CCB} ≤ 3.6 V	5-V CMOS	3.3-V LVTTL/LVCMOS
SN74LVCC4245A	4.5 V ≤ V_{CCA} ≤ 5.5 V 2.7 V ≤ V_{CCB} ≤ 5.5 V	5-V CMOS	3.3-V LVTTL/LVCMOS
		5-V CMOS	5-V CMOS
SN74ALVC164245	2.3 V ≤ V_{CCA} ≤ 3.6 V 3 V ≤ V_{CCB} ≤ 5.5 V	2.5-V CMOS	3.3-V LVTTL/LVCMOS
		3.3-V LVTTL/LVCMOS	5-V CMOS
SN74AVCA164245(1) SN74AVCB164245(1) SN74AVCB324245(1)	1.4 V ≤ V_{CCA} ≤ 3.6 V 1.4 V ≤ V_{CCB} ≤ 3.6 V	1.5-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		1.8-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		2.5-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		3.3-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
SN74AVC1T45(1) SN74AVC2T45(1) SN74AVC4T245(1)(2) SN74AVC8T245(1) SN74AVC16T245(1) SN74AVC20T245(1) SN74AVC24T245(1) SN74AVC32T245(1)	1.2 V ≤ V_{CCA} ≤ 3.6 V 1.2 V ≤ V_{CCB} ≤ 3.6 V	1.2-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		1.5-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		1.8-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		2.5-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS
		3.3-V CMOS	1.5-V CMOS, 1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS

(1) Bus-hold option available
(2) In development, check http://www.ti.com/trans for availability.

Table 1. Possible Voltage-Translation Combinations Using Dual-Supply Translators (Continued)

Device	Supply Voltage	Possible Voltage-Translation Combinations	
		A Port	B Port
SN74LVC1T45 SN74LVC2T25 SN74LVC8T25(1)(2) SN74LVC16T25(1)(2)	1.65 V ≤ V_{CCA} ≤ 5.5 V 1.65 V ≤ V_{CCB} ≤ 5.5 V	1.8-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS, 5-V CMOS
		2.5-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS, 5-V CMOS
		3.3-V LVCMOS/LVTTL	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS, 5-V CMOS
		5-V CMOS	1.8-V CMOS, 2.5-V CMOS, 3.3-V LVTTL/LVCMOS, 5-V CMOS

(1) Bus-hold option available
(2) In development, check http://www.ti.com/trans for availability.

TI has adopted an easy-to-understand naming convention for its dual-supply level-translation devices that have been released since January 2004. Figure 4 shows the interpretation of the SN74AVC8T245 device name. Translators using this naming convention have control circuitry powered by V_{CCA}, unless otherwise stated in the data sheet.

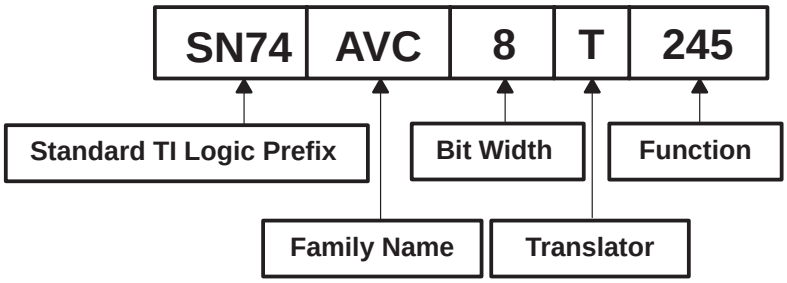

Figure 4. Dual-Supply Level-Translation Device Nomenclature

3 Open-Drain Devices

Devices with open-drain outputs have an N-channel transistor between the output and GND. These devices can be used in level-translation applications as shown in Figure 5. The output voltage is determined by $V_{CCB.}$ V_{CCB} can be greater than the input high-level voltage (up-translation) or lower than the input high-level voltage (down-translation).

Open-drain devices are useful in translating to and from a variety of supply-voltage nodes. However, there are some drawbacks to this method of level translation. When the output of the driver is low, i.e., when the output N-channel transistor is on, there is a constant current flow from V_{CCB} to GND through the resistor R_{pullup} and transistor T1. This contributes to higher system power consumption.

Using a higher-value pullup resistor can minimize this current flow. However, a larger resistor also slows down the rise time of the output signal because of the higher RC time constant of the resistor R_{pullup} and the output load.

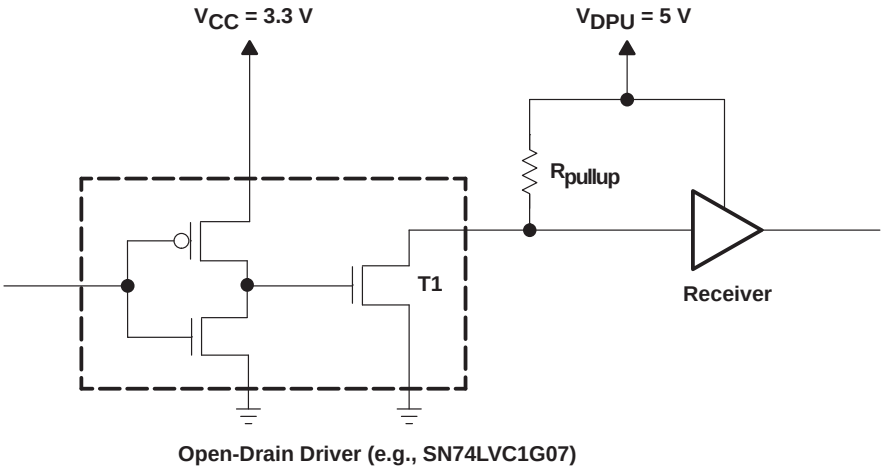

Figure 5. Level Translation Using an Open-Drain Device

Advantages of open-drain devices:

- Can be used to up-translate and down-translate to/from a variety of voltage nodes
- Can be used in a wired-OR interface

3.1 Application Example − Level Translation Using the SN74LVC2G07

Figure 6 shows one buffer of the SN74LVC2G07 translating up from 1.8 V to 5 V, while the other translates down from 3.3 V to 1.8 V.

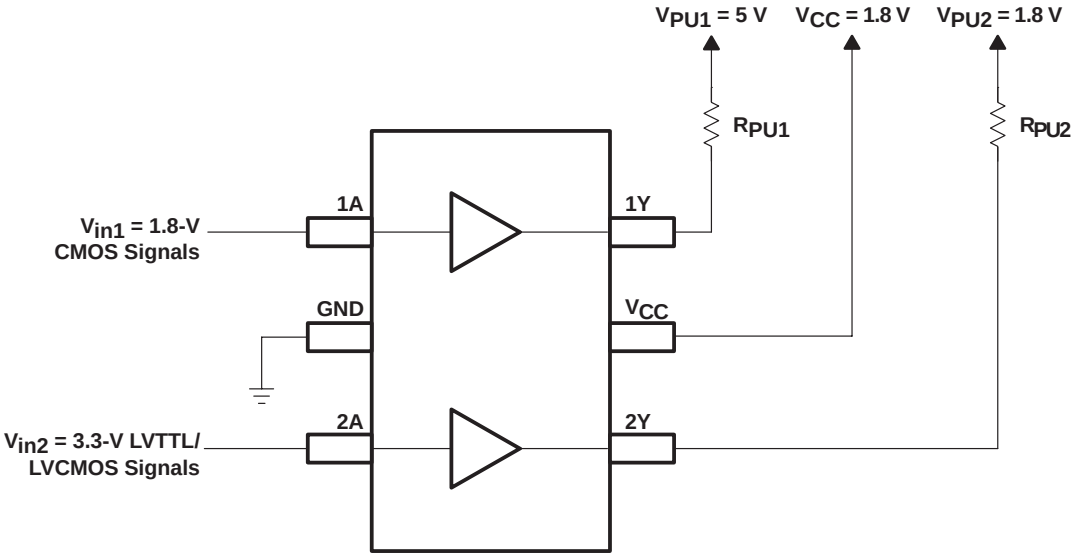

Figure 6. Use of an Open-Drain Device in a Level-Translation Application

A supply voltage of 1.8 V is used, which enables the device to recognize the lowest V_{IH} expected at the input of the device as a valid high signal. The minimum value of the output pullup resistor is restricted by the maximum current-sinking capability (I_{OL} max) of the open-drain device, whereas the maximum value is limited by maximum allowable rise time of the output signal.

$$R_{PU(min)} = \frac{V_{PU} - V_{OL}}{I_{OL(max)}}$$

For the SN74LVC2G07 case shown in Figure 6, assuming V_{PU1} = 5 V ± 0.5 V, V_{PU2} = 1.8 V ± 0.15 V, and using resistors with 5% tolerance:

$$R_{PU1(min)} = \frac{5.5\ V - 0.45\ V}{4\ mA} \times \frac{1}{0.95} = 1.33\ k\Omega$$

The closest (next highest) value of a standard resistor with 5% tolerance is 1.5 kΩ.

$$R_{PU2(min)} = \frac{1.8\ V - 0.45\ V}{4\ mA} \times \frac{1}{0.95} = 394.73\ \Omega$$

The closest (next highest) value of a standard resistor with 5% tolerance is 430 Ω.

Figure 7 shows the output waveforms with a capacitive load of 10 pF and different values of pullup resistors. As the pullup resistor value is increased, the rise time of the output signal increases.

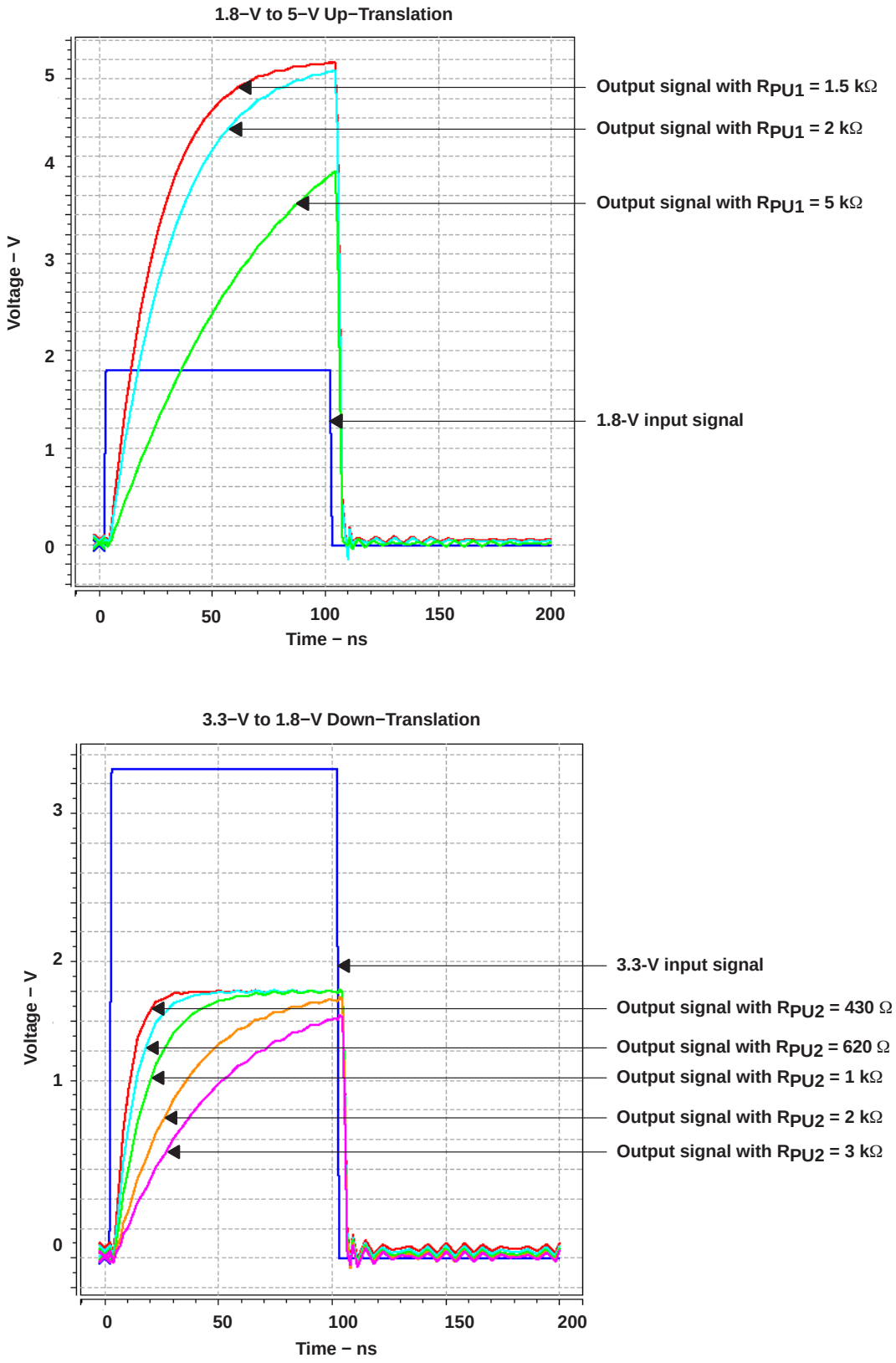

Figure 7. Output Edge Slows With Increasing Value of R_{PU}

3.2 Do Not Use Pullup Resistors at Outputs of CMOS Drivers

To achieve level translation, system designers should not use a pullup resistor at the output of a device with CMOS (push-pull) outputs. This technique has several flaws and should be avoided. One drawback is increased power consumption whenever the output switches low, as discussed at the beginning of section 3. Another problem occurs when the output of the CMOS driver is high. In this state, the lower N-channel transistor is off, while the upper P-channel transistor is on. There is a backflow of current from the high supply to the low supply through the resistor R and the upper P-channel transistor. This current flow into the low supply could cause undesirable effects.

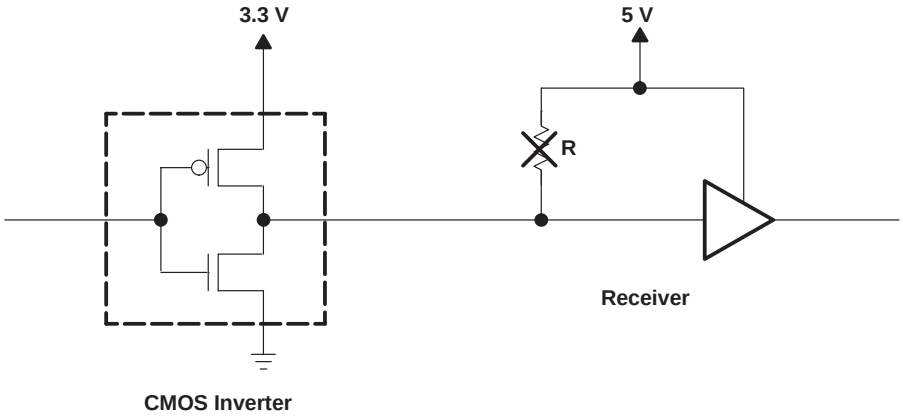

Figure 8. Use of Pullup Resistors at Output of CMOS Drivers Is Not Recommended

4 FET Switches

Bus switches from TI's CB3T, CBT, CBTD, and TVC families can be used in level-translation applications. FET switches are ideal for translation applications in which active current drive is not required or where very fast propagation delays are desired.

Advantages of FET switches:

- Fast propagation delays
- TVC devices (or CBT configured as TVC) can be used for bidirectional level translation without direction control.

Devices from TI's CB3T family can be used for down-translation from 5 V to 3.3 V when operated with V_{CC} = 3.3 V and for down-translation from 5 V or 3.3 V to 2.5 V when operated with V_{CC} = 2.5 V. CB3T devices can be used for bidirectional translation in some applications as shown in Figure 9.

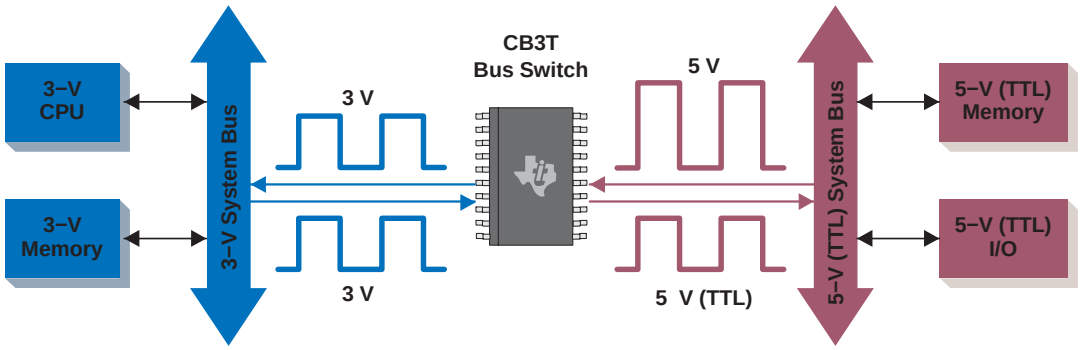

Figure 9. CB3T Device Used to Interface a 3-V Bus With a 5-V (TTL) Bus

In Figure 9, the SN74CB3T3306 is used to interface a 3-V bus with a 5-V (TTL) bus. The CB3T device is operated with a supply voltage of 3 V. When channeling a signal from the 5-V bus to the 3-V bus, the CB3T device clamps the output voltage to V_{CC} (3 V). When channeling a signal from the 3-V bus to the 5-V bus, the output signal on the 5-V side is clamped to about 2.8 V, which is a valid V_{IH} level for a 5-V TTL device. Two drawbacks of this approach must be considered:

1. The 2.8-V V_{OH} level from the ‘CB3T3306 poses a reduced high-level noise margin on the 5-V side. In this case, the noise margin would be 2.8 V – 2.0 V = 800 mV.
2. Because the high output from the CB3T device is not driven all the way to the V_{CC} rail, the 5-V receiver exhibits excess power consumption called ΔI_{CC} current (more discussion about ΔI_{CC} is presented in Section 6).

NOTE: The 2.8-V V_{OH} level is with V_{CC} = 3 V, T_A = 25°C, I_O = 1 µA. This 2.8 V would not be a valid V_{IH} level for a 5-V CMOS receiver; therefore, CB3T devices cannot be used to up-translate when interfacing a 3-V bus with a 5-V CMOS bus (without the use of a pullup resistor).

4.1 CBT and CBTD Devices

Devices from the CBT and CBTD families can be used to interface 5-V systems with 3.3-V systems. These devices can only be used to down-translate when interfacing a 5-V CMOS system with a 3.3-V system. They can be used for bidirectional translation when interfacing a 5-V TTL system with a 3.3-V system.

Figure 10 shows the SN74CBT1G384 used for 5-V to 3.3-V translation. An external diode must be connected between the 5-V supply and the V_{CC} pin of the device. The external diode drops the gate voltage of the pass transistor down to 4.3 V. An additional V_{GS} drop of 1 V results in 3.3 V on Pin 2. Additional diodes can be used to limit the output to even lower voltages. In some cases, the quiescent current (I_{CC}) flowing through the diode may not be enough to turn on the diode, and resistor R is added to ground to ensure enough bias current through the diode.

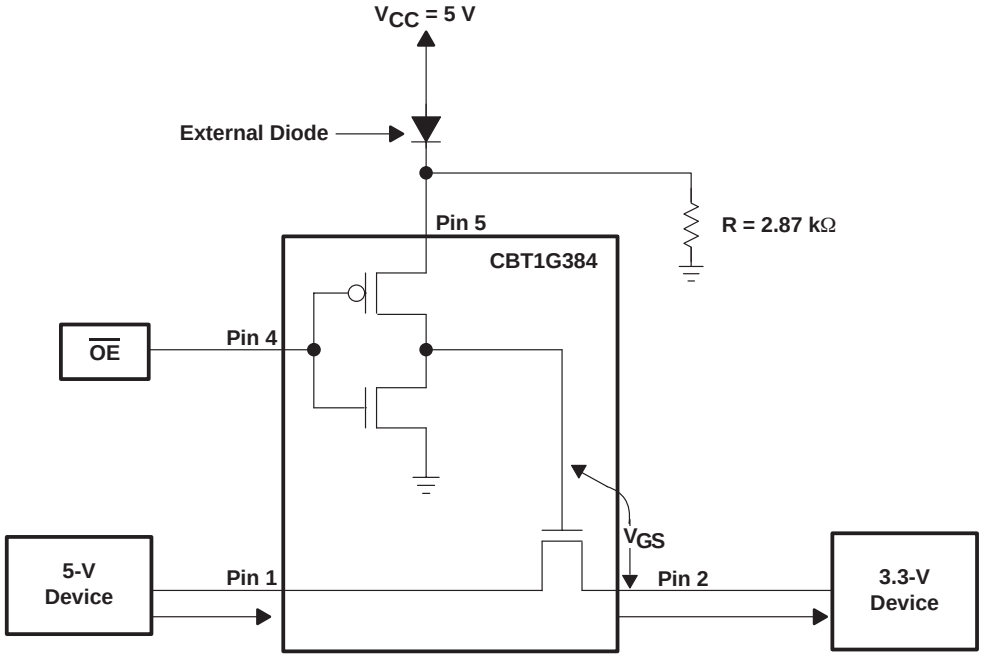

Figure 10. SN74CBT1G384 In 5-V to 3.3-V Application

Figure 11 shows the waveforms for this 5-V to 3.3-V down-translation; the propagation delay from input to output is very minimal. CBT devices also can be configured like Translation Voltage Clamp (TVC) devices for flexible, bidirectional translation without direction control. This is discussed in detail in the TI application report, *Flexible Voltage-Level Translation With CBT Devices,* literature number SCDA006.

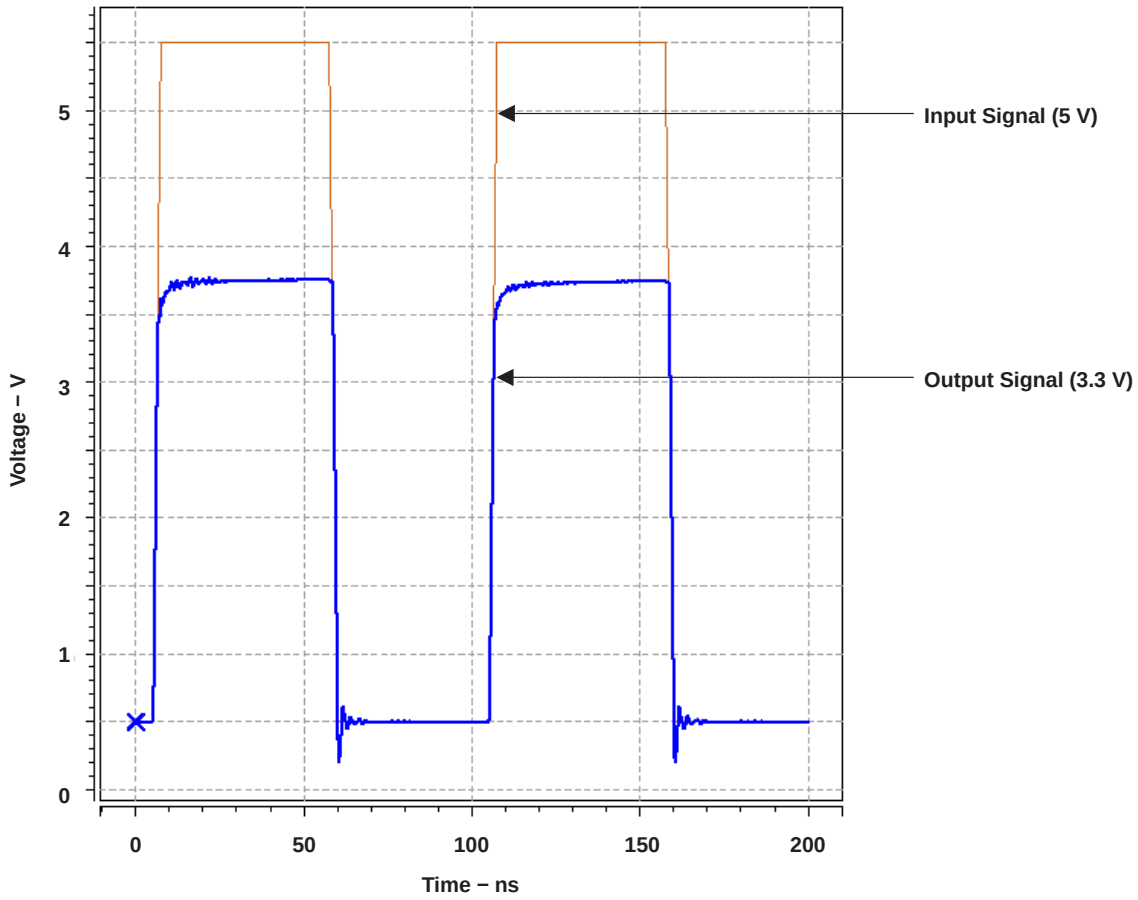

Figure 11. 5-V to 3.3-V Translation Using CBT Device

4.2 Using Translation Voltage Clamp (TVC) Devices

TVC devices can be used for bidirectional level translation. These devices do not need a direction control signal. Each TVC device consists of an array of N-channel pass transistors with their gates tied together internally as shown in Figure 12.

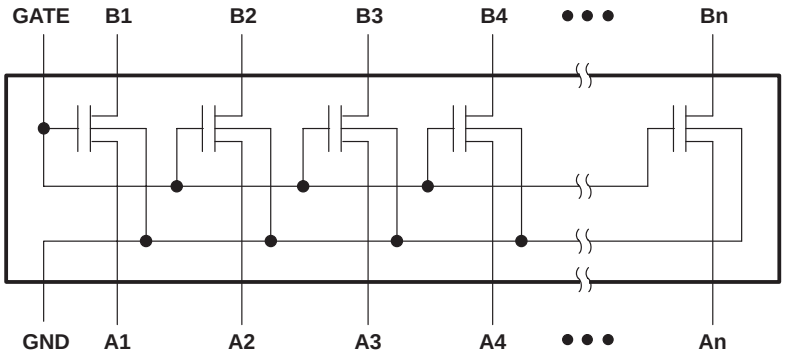

Figure 12. Simplified Schematic of a Typical TVC-Family Device

In a translating application, one of the FETs is connected as a reference transistor, and the other transistors are used as pass transistors. The most positive voltage on the low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. All of the transistors in the array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because the transistors are fabricated symmetrically, and the I/O signals are bidirectional through each FET, either port connection of each bit can be used as the low-voltage side.[1]

The drain of the reference transistor must be connected to V_{DDREF} through a resistor as shown in Figure 13, and V_{REF} must be less than or equal to (V_{BIAS} − 1) to bias the reference transistor into conduction. The gate of the reference transistor is tied to its drain to saturate the transistor.

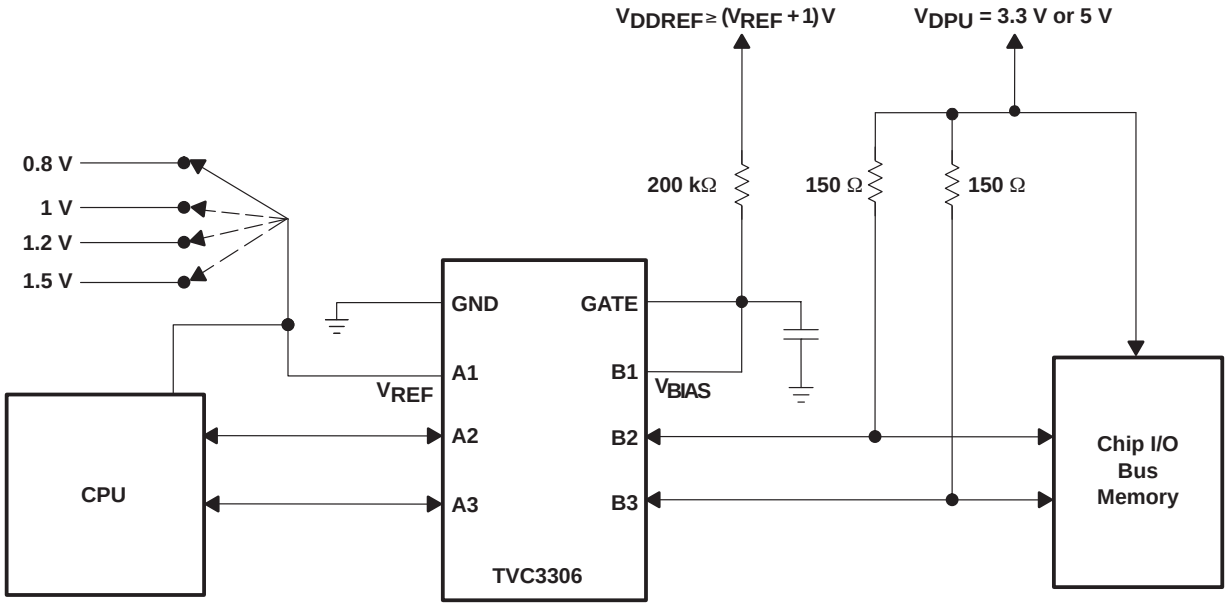

Figure 13. SN74TVC3306 Used in a Level-Translation Application

In the example shown in Figure 13, V_{REF} is set equal to the I/O voltage level of the CPU, whereas V_{DPU} is set to the voltage level desired on the B side. When down-translating from the B side to the A side, the voltage on the A side is clamped off at V_{REF}. When up-translating from A2 (A3) to B2 (B3), as the voltage on the A side approaches V_{REF}, the pass transistor between A2 (A3) and B2 (B3) switches off, and the voltage on B2 (B3) is pulled up to V_{DPU} through the 150-Ω pullup resistor.

See Figure 14 for the waveforms for bidirectional translation using a TVC device and Tables 2 and 3 for possible voltage-translation combinations.

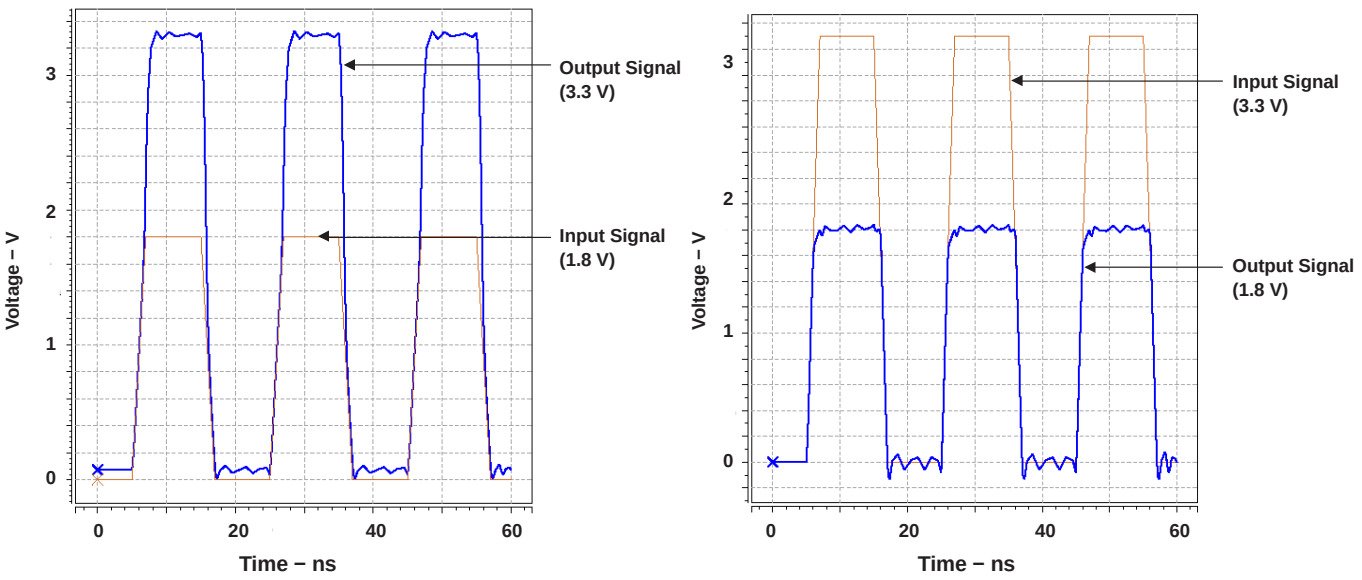

Figure 14. Waveforms For Bidirectional Translation Using a TVC Device

Table 2. Possible Voltage-Translation Combinations Using an FET Switch

FET Switch Family	V_{CC} Range	From	To	V_{CC} Used
CBT (with external diode)	4 V ≤ V_{CC} ≤ 5.5 V	5-V CMOS	3.3-V LVTTL/LVCMOS	5 V
CBTD	4.5 V ≤ V_{CC} ≤ 5.5 V	5-V CMOS	3.3-V LVTTL/LVCMOS	5 V
CB3T	2.3 V ≤ V_{CC} ≤ 3.6 V	5-V CMOS	3.3-V LVTTL/LVCMOS	3.3 V
			2.5-V LVCMOS	2.5 V
		3.3-V LVTTL/LVCMOS	2.5-V LVCMOS	2.5 V

Table 3. Possible Voltage-Translation Combinations Using a TVC Device

Switch Family	V_{REF} Range	Bidirectional Translation Between		Min V_{DDREF}	V_{REF}	V_{DPU}
TVC (or CBT device used as TVC)	0 V ≤ V_{REF} ≤ 5.5 V	5-V CMOS	3.3-V LVTTL/LVCMOS	4.3 V	3.3 V	5 V
			2.5-V CMOS	3.5 V	2.5 V	
			1.8-V CMOS	2.8 V	1.8 V	
			1.5-V CMOS	2.5 V	1.5 V	
			1.2-V CMOS	2.2 V	1.2 V	
			0.8-V CMOS	1.8 V	0.8 V	
		3.3-V LVTTL/ LVCMOS	5-V CMOS	4.3 V	3.3 V	5 V
			2.5-V CMOS	3.5 V	2.5 V	3.3 V
			1.8-V CMOS	2.8 V	1.8 V	
			1.5-V CMOS	2.5 V	1.5 V	
			1.2-V CMOS	2.2 V	1.2 V	
			0.8-V CMOS	1.8 V	0.8 V	
		2.5-V CMOS	5-V CMOS	3.5 V	2.5 V	5 V
			3.3-V LVTTL/LVCMOS			3.3 V
			1.8-V CMOS	2.8 V	1.8 V	2.5 V
			1.5-V CMOS	2.5 V	1.5 V	
			1.2-V CMOS	2.2 V	1.2 V	
			0.8-V CMOS	1.8 V	0.8 V	
		1.8-V CMOS	5-V CMOS	2.8 V	1.8 V	5 V
			3.3-V LVTTL/LVCMOS			3.3 V
			2.5-V CMOS			2.5 V
			1.5-V CMOS	2.5 V	1.5 V	1.8 V
			1.2-V CMOS	2.2 V	1.2 V	
			0.8-V CMOS	1.8 V	0.8 V	
		1.5-V CMOS	5-V CMOS	2.5 V	1.5 V	5 V
			3.3-V LVTTL/LVCMOS			3.3 V
			2.5-V CMOS			2.5 V
			1.8-V CMOS			1.8 V
			1.2-V CMOS	2.2 V	1.2 V	1.5 V
			0.8-V CMOS	1.8 V	0.8 V	
		1.2-V CMOS	5-V CMOS	2.2 V	1.2 V	5 V
			3.3-V LVTTL/LVCMOS			3.3 V
			2.5-V CMOS			2.5 V
			1.8-V CMOS			1.8 V
			1.5-V CMOS			1.5 V
			0.8-V CMOS	1.8 V	0.8 V	1.2 V
		0.8-V CMOS	5-V CMOS	1.8 V	0.8 V	5 V
			3.3-V LVTTL/LVCMOS			3.3 V
			2.5-V CMOS			2.5 V
			1.8-V CMOS			1.8 V
			1.5-V CMOS			1.5 V
			1.2-V CMOS			1.2 V

5 Overvoltage-Tolerant Devices

Devices with overvoltage-tolerant inputs can tolerate input voltages greater than the device supply voltage. This is made possible by eliminating the input clamp diode to V_{CC} and using thicker gate oxides that tolerate voltage levels higher than V_{CC}. These devices can be used to perform down-translation as shown in Figure 15. There are two ways to identify a device with overvoltage-tolerant inputs:

- Look at the input voltage (V_I) parameter under the recommended operating conditions in the data sheet. Devices with overvoltage-tolerant inputs have a max V_I value that is independent of V_{CC}. It is specified as a definite number, for example, 5.5 V.
- Look at the input diode current (I_{IK}) under absolute maximum ratings. Devices with overvoltage-tolerant inputs have only a minus sign in front of the number, for example, −20 mA instead of ±20 mA. This implies that only a GND clamp diode is present at the input, and that the input clamp diode to V_{CC} is absent.

Devices from the AUC, LVC, LV-A, and AHC families have overvoltage-tolerant inputs. For transceiver functions within these families, I/Os are overvoltage-tolerant only if the device has the I_{OFF} feature.

NOTE: Devices from the AHC family do not have the I_{OFF} feature; therefore, transceiver functions from this family do not have overvoltage-tolerant I/Os.

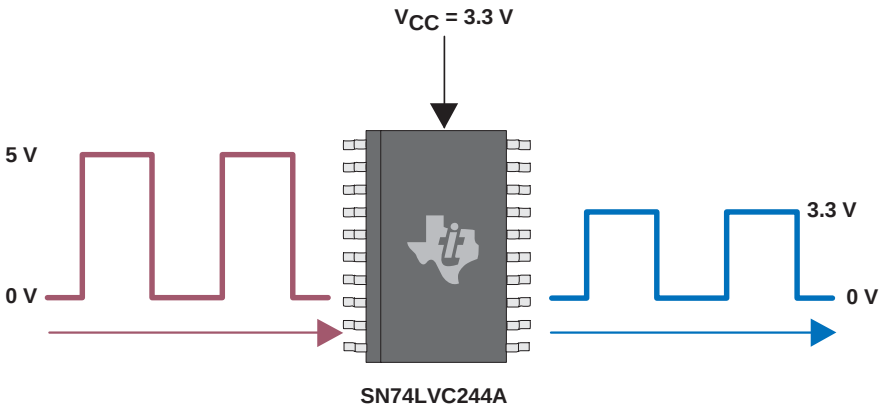

Figure 15. Down-Translation Using a Logic Device With Overvoltage-Tolerant Inputs

When using overvoltage-tolerant devices for level translation, if the input signal has slow edges, then the duty cycle of the output signal might be affected. For the example shown in Figure 15, the inputs swing from 0 to 5 V and 5 to 0 V, but because the device is operated with V_{CC} = 3.3 V, it switches at 3.3-V threshold levels. If the input signal has slow rise and fall times, this will result in a change in the output duty cycle as shown in Figure 16. Therefore, overvoltage-tolerant devices might not be the ideal translation solution in applications where output duty cycle is critical, for example, certain clock applications.

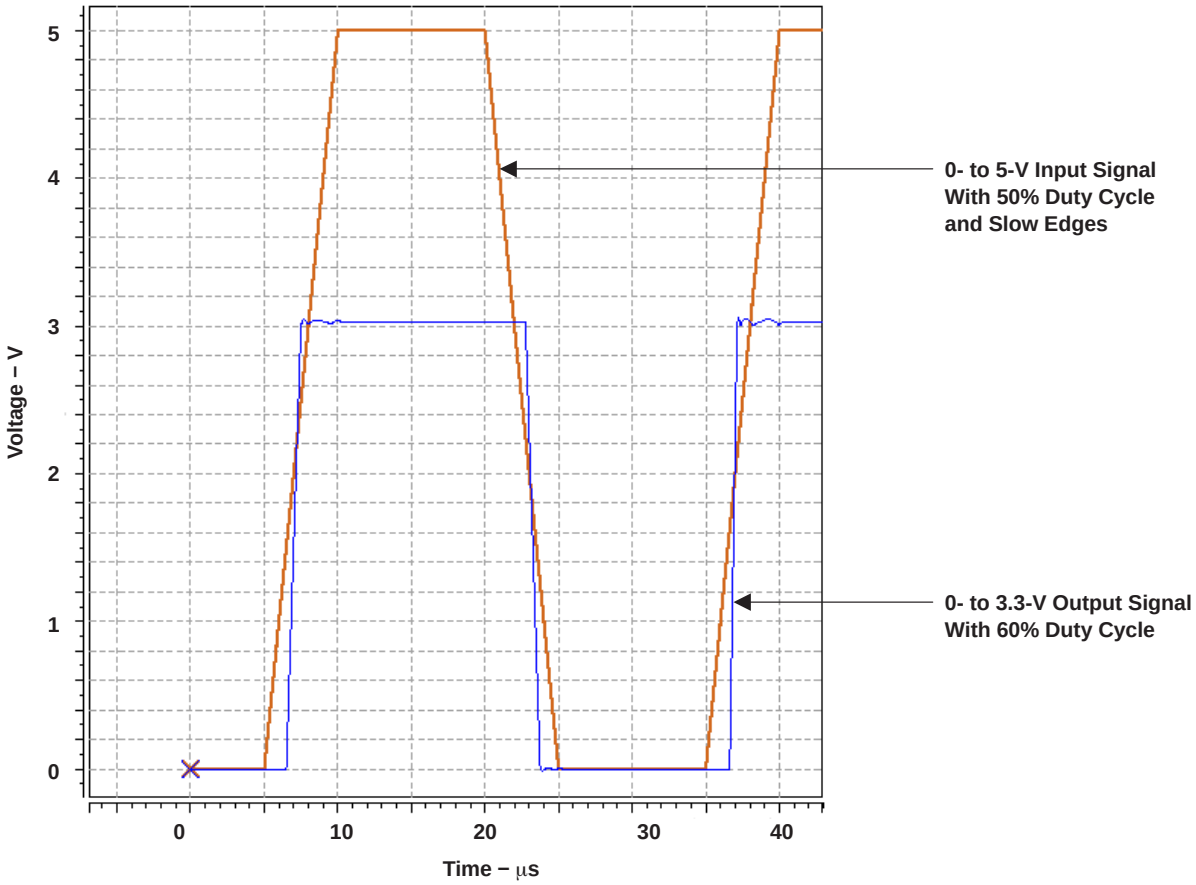

Figure 16. Shift in Output Duty Cycle When Using An Overvoltage-Tolerant Device For Level Translation

Advantages of overvoltage-tolerant devices:

- Only one supply voltage needed
- Broad portfolio of AHC, AUC, AVC, LV-A, and LVC devices

See Table 4 for possible voltage-translation combinations.

Table 4. Possible Voltage-Translation Combinations Using Overvoltage-Tolerant Devices

Device Family	V_{CC} Range	From	To	V_{CC} Used
AHC, LV-A	$2\ V \le V_{CC} \le 5.5\ V$	5-V CMOS	3.3-V LVTTL/LVCMOS	3.3 V
			2.5-V CMOS	2.5 V
		3.3-V LVTTL/LVCMOS	2.5-V CMOS	2.5 V
LVC	$1.65\ V \le V_{CC} \le 3.6\ V$ $1.65\ V \le V_{CC} \le 5.5\ V$ (Little Logic)	5-V CMOS	3.3-V LVTTL/LVCMOS	3.3 V
			2.5-V CMOS	2.5 V
			1.8-V CMOS	1.8 V
		3.3-V LVTTL/LVCMOS	2.5-V CMOS	2.5 V
			1.8-V CMOS	1.8 V
		2.5-V CMOS	1.8-V CMOS	1.8 V
AVC	$1.4\ V \le V_{CC} \le 3.6\ V$	3.3-V LVTTL/LVCMOS	2.5-V CMOS	2.5 V
			1.8-V CMOS	1.8 V
			1.5-V CMOS	1.5 V
		2.5-V CMOS	1.8-V CMOS	1.8 V
			1.5-V CMOS	1.5 V
		1.8-V CMOS	1.5-V CMOS	1.5 V
AUC	$0.8\ V \le V_{CC} \le 2.5\ V$	3.3-V LVTTL/LVCMOS	2.5-V CMOS	2.5 V
			1.8-V CMOS	1.8 V
			1.5-V CMOS	1.5 V
			1.2-V CMOS	1.2 V
			0.8-V CMOS	0.8 V
		2.5-V CMOS	1.8-V CMOS	1.8 V
			1.5-V CMOS	1.5 V
			1.2-V CMOS	1.2 V
			0.8-V CMOS	0.8 V
		1.8-V CMOS	1.5-V CMOS	1.5 V
			1.2-V CMOS	1.2 V
			0.8-V CMOS	0.8 V
		1.5-V CMOS	1.2-V CMOS	1.2 V
			0.8-V CMOS	0.8 V
		1.2-V CMOS	0.8-V CMOS	0.8 V

6 Devices With TTL-Compatible Inputs

Devices from the HCT, AHCT, ACT, ABT, and FCT families can accept TTL-level input signals and output 5-V CMOS signals. Because 5-V TTL and 3-V LVTTL/LVCMOS switching thresholds are equal (see Figure 2), these devices can be used to translate from 3.3 V to 5 V. However, because the input high signals are not driven all the way to the 5-V rail, the input stages of the receiver device draw extra static current called the ΔI_{CC} current. Figure 16 shows a plot of the I_{CC} vs V_{IN} characteristics of the SN74HCT541. For a static 3.3-V input signal, the device draws a continuous excess current of about 290 μA per input.

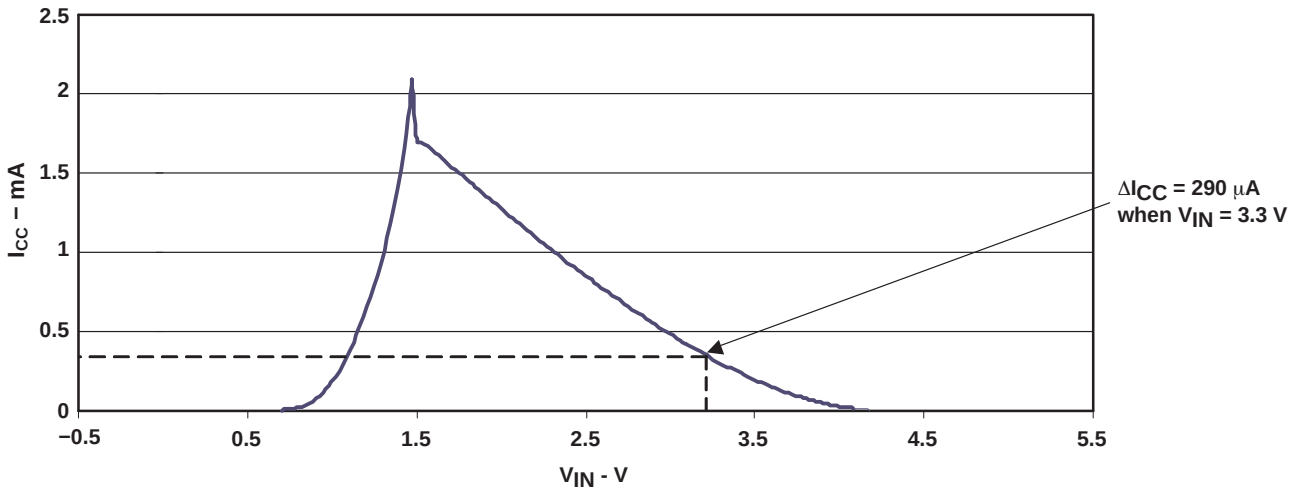

Figure 17. V_{IN} vs I_{CC} Characteristics of SN74HCT541

Advantages of devices with TTL-compatible inputs:

- Only one supply voltage needed
- Broad portfolio of HCT, AHCT, ACT, ABT, and FCT devices to choose from

7 Summary of Translation Solutions

Dual-supply devices: This is the best choice for most voltage level-translation applications. These devices can perform bidirectional level translation between a variety of voltage nodes. They offer low power consumption, fast propagation delays, and active current drive.

Open-drain devices: Open-drain devices can be used to up-translate or down-translate, with the use of an external pullup resistor at the output. This solution is very flexible, but it is not very power efficient.

Devices with overvoltage-tolerant inputs: These devices are a good option to easily down-translate a signal. If the input signal has slow rising and falling edges, then the duty cycle of the output signal might be affected.

CB3T devices: These FET switches are ideal for 5-V to 2.5-V, 5-V to 3.3-V, and 3.3-V to 2.5-V down-translation applications. CB3T devices offer sub 1-ns propagation delays and very low power consumption. These devices do not provide drive current, and a dual-supply translator should be used if buffering is needed.

CBT/CBTD devices: CBT (with an external diode) or CBTD devices can be used to perform 5-V to 3.3-V down-translation. These devices offer fast propagation delays and low power consumption. These devices do not provide current drive, and an alternate solution should be used if buffering is needed.

TVC devices: TVC devices allow bidirectional level translation without the need for a direction control signal. This solution requires the use of external pullup resistors. Power consumption depends on the values of external pullup resistors. A CBT device can be configured to operate as a TVC device as well.

Devices with TTL-compatible inputs: Devices from the HCT, AHCT, ACT, ABT, and FCT families can be used for 3.3-V to 5-V up-translation. This solution causes excess system power consumption and should be avoided in applications where power consumption is a major concern.

8 Conclusion

There are several ways to achieve logic-level translation, and each approach has its own merits and demerits. Using dual-supply level translators usually is the best option for most level-translation applications. TI offers a broad portfolio of dual-supply level translators to meet all your mixed-voltage interfacing needs. In situations where these devices might not be the most optimal solution, other solutions should be considered. Open-drain devices can be used for up- and down-translation in applications where power consumption is not a major concern. Bus switches and overvoltage-tolerant devices should be considered for down-translation applications, and devices with TTL-compatible inputs can be used for 3.3-V to 5-V up-translation if increased system power consumption is acceptable.

9 References

1. Thomas V. McCaughey, Stephen M. Nolan, and John D. Pietrzak, *Flexible Voltage-Level Translation With CBT Family Devices*, TI literature number SCDA006.

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