

# **Texas Instruments Little Logic Application Report**

---

*Chris Cockrill, Shawn Cohee, and Tomdio Nana*

*Standard Linear & Logic*

## **ABSTRACT**

Portable and consumer electronic systems' needs present greater challenges today than ever before. Engineers strive to design smaller, faster, lower-cost systems to meet the market demand. Consequently, the semiconductor industry faces a growing need to increase operating speed, minimize power consumption, and reduce packaging size. Texas Instruments manufactures a variety of Little Logic semiconductor devices that are ideal for such applications. This application report provides in-depth analysis of each of the various TI Little Logic product families by examining performance and features, along with the variety of available package options. The information provided in this report will assist designers of new and existing designs in selecting the correct Little Logic device for their application.

Keywords: 0.8 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V, 5.0 V, AHC, AHCT, AUC, CBT, CBTLV, electrical performance, LVC, Little Logic, NanoStar, NanoFree, power consumption

---

## **Contents**

<b>1</b>	<b>Introduction</b> .....	<b>2</b>
<b>2</b>	<b>Product Portfolio</b> .....	<b>4</b>
	2.1 AUC Little Logic .....	4
	2.2 LVC Little Logic .....	4
	2.3 AHC and AHCT Little Logic .....	4
	2.4 CBT Little Logic .....	4
<b>3</b>	<b>Features and Characteristics</b> .....	<b>5</b>
	3.1 Electrical Performance .....	5
	3.2 Propagation Delay and Maximum Operating Speed .....	5
	3.3 Input and Output Transition Time .....	9
	3.4 Power Consumption .....	10
<b>4</b>	<b>Package Information</b> .....	<b>15</b>
<b>5</b>	<b>Features and Benefits</b> .....	<b>17</b>
<b>6</b>	<b>Conclusion</b> .....	<b>17</b>
<b>7</b>	<b>Frequently Asked Questions (FAQs)</b> .....	<b>18</b>
<b>8</b>	<b>References</b> .....	<b>19</b>
<b>9</b>	<b>Glossary</b> .....	<b>19</b>
	<b>Appendix – Package Mechanical Data</b> .....	<b>21</b>

## List of Figures

1	Principle Behind Little Logic	3
2	Typical Little Logic Applications	3
3	$t_{pd}$ vs $C_L$ for SN74AUC1G00 at 0.8-V and 1.2-V $V_{CC}$	6
4	$t_{pd}$ vs $C_L$ for SN74AUC1G00 at 1.5-V, 1.8-V, and 2.5-V $V_{CC}$	7
5	$t_{pd}$ vs $C_L$ for SN74LVC1G00 at 1.8-V and 2.5-V $V_{CC}$	7
6	$t_{pd}$ vs $C_L$ for SN74LVC1G00 at 3.3-V and 5-V $V_{CC}$	8
7	Output Transition Time for TI Little Logic Devices	10
8	CMOS Input-Stage Circuit	11
9	Typical Current Consumption for SN74AUC1G32	12
10	Typical Current Consumption for SN74LVC1G32	12
11	Typical Current Consumption for SN74AHC1G32	13
12	Typical Power-Dissipation Capacitance for TI Little Logic Devices	14
13	TI Little Logic Package Options	15
14	Little Logic Industry Packaging Comparison	16
15	5-Pin DBV – Small-Outline Package (SOP)	21
16	5-Pin DCK – Small-Outline Package (SOP)	22
17	6-Pin DBV – Small-Outline Package (SOP)	23
18	6-Pin DCK – Small-Outline Package (SOP)	24
19	8-Pin DCT – Shrink Small-Outline Package (SSOP)	25
20	8-Pin DCU – Very Thin Shrink Small-Outline Package (VSSOP)	26
21	5-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†	27
22	6-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†	28
23	8-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†	29

## List of Tables

1	Little Logic Electrical-Performance Summary	5
2	Laboratory-Measured Frequencies for TI Little Logic Devices	9
3	Input Transition Rates for TI Little Logic Devices	9
4	TI Little Logic Packages Size and Weight	15
5	Little Logic Package Size and Weight Comparison	16
6	Features and Benefits of TI Little Logic Devices	17

## 1 Introduction

Little Logic is a product segment of single, dual, and triple gates available in several standard logic functions and packages. The principle driving Little Logic is derived from the standard quad gate, which once was the smallest number of gate functions on one device. Little Logic improves upon previous quad-gate technology by allowing the designer to use only what is needed (see Figure 1). One is no longer penalized additional cost and board space by having to include extra gates that never will be used.

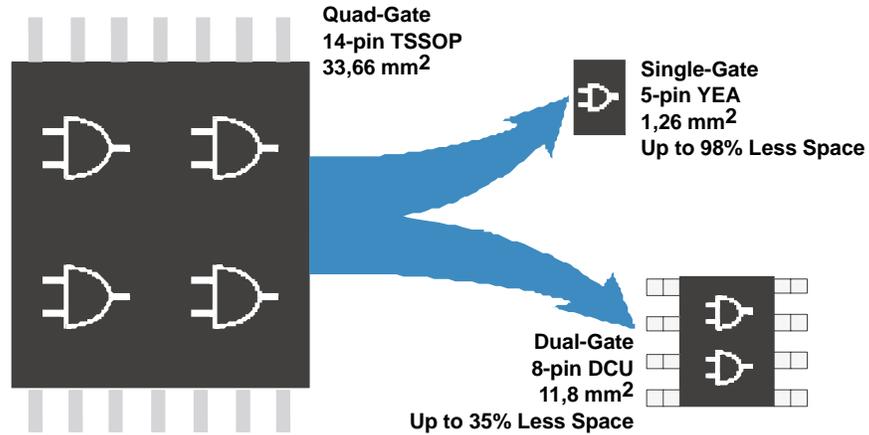


Figure 1. Principle Behind Little Logic

Little Logic devices are the pieces that help complete the design puzzle. Their extremely small size allows system designers to simplify design routing and maximize ASIC design development (see Figure 2).

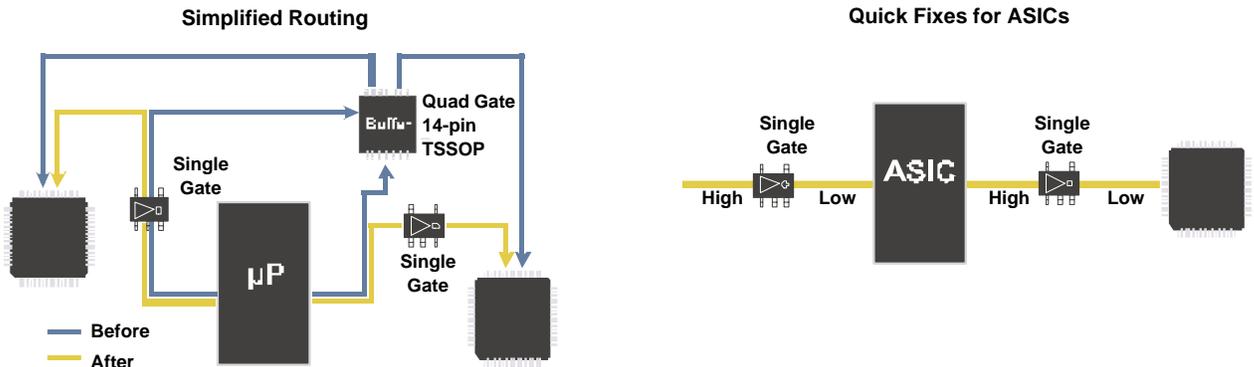


Figure 2. Typical Little Logic Applications

As portable consumer electronic products continue to decrease in size and require advancements in semiconductor process technology, IC packaging must answer the demand for board area and increased performance. As the number of gates decrease per device, so do the package sizes. Texas Instruments offers Little Logic devices in 5-pin SOT-23 (DBV), 5-pin SC-70 (DCK), 6-pin SOT-23 (DBV), 6-pin SC-70 (DCK), 8-pin SM-8 (DCT), 8-pin US-8 (DCU), and the smallest logic packages available today, NanoStar™ (YEA) and NanoFree™ (YZA). NanoStar and NanoFree devices are manufactured using a wafer-chip-scale package (WCSP) process, also known as die-size ball grid array (DSBGA, JEDEC MO-211) and offer a 70% reduction in area, as compared to the 5-pin SC-70 package.

Besides being offered in many different packages, Little Logic devices are processed across several product technologies. Devices are available in the following distinct product families: AUC, LVC, AHC, AHCT, and CBT.

## 2 Product Portfolio

### 2.1 AUC Little Logic

The advanced ultra-low-voltage CMOS (AUC) logic is optimized at 1.8 V, with operation from 0.8 V to 2.7 V and I/O tolerant to 3.6 V. AUC offers an 8-mA output drive and a typical propagation delay of 2 ns at 1.8-V supply voltage. AUC devices also are specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. AUC meets a variety of demands that have been placed on logic designers by offering low-voltage operation, faster speed, and lower power consumption, while still maintaining overall signal integrity. AUC was designed to meet advanced system performance requirements in applications such as telecommunications equipment, high-performance workstations, PCs and networking servers, and next-generation portable consumer electronics. As designers migrate to lower voltages for their core processors and ASICs, they will require the low-voltage logic functions provided by AUC Little Logic devices.

### 2.2 LVC Little Logic

The low-voltage CMOS (LVC) logic is optimized at 3.3 V, with operation from 1.65 V to 5.5 V. LVC offers a 24-mA output drive and a typical propagation delay of 3.5 ns at 3.3-V supply voltage. Due to its wide operating voltage range, LVC devices offer a versatile solution for several different system levels. LVC devices also are specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 2.3 AHC and AHCT Little Logic

The advanced high-speed CMOS (AHC) logic and advanced high-speed CMOS TTL (AHCT) logic were the first TI logic families to offer Little Logic devices. AHC and AHCT both are optimized at 5 V, but have different supply-voltage operating ranges. AHC is specified for operation from 2 V to 5.5 V, whereas AHCT is specified for TTL operation at 4.5 V to 5.5 V. AHC and AHCT provide 8-mA output drive and a typical propagation delay of 5 ns at 5-V supply voltage.

### 2.4 CBT Little Logic

The crossbar technology (CBT) logic family provides bus-switch solutions for easy communication between devices. TI offers Little Logic bus-switch devices in the CBT, CBTD and CBTLV product families. CBT and CBTD are optimized at 5 V with operation from 4.5-V to 5.5-V supply voltage and have inherent  $I_{\text{off}}$  protection due to the bus-switch characteristics. CBTD devices have an integrated diode to  $V_{\text{CC}}$  that allows level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs. CBTLV is the low-voltage bus-switch solution, with an operating range from 2.3-V to 3.6-V supply voltage. CBTLV features  $I_{\text{off}}$  protection circuitry, which isolates the current through the switch. All three product options provide a typical propagation delay of 0.25 ns at their respective optimized voltage levels.

## 3 Features and Characteristics

### 3.1 Electrical Performance

TI Little Logic provides optimal performance across a wide range of operating levels. As logic design requirements have progressed over time, TI has provided a solution by offering a new product technology. The first Little Logic family available was AHC and AHCT, which is optimized at 5 V. As systems migrated to 3.3-V levels, TI provided a solution with LVC products. With the increasing demand for lower-voltage operation, faster speed, and reduced power consumption, TI released the AUC family.

Table 1 summarizes the electrical-performance specifications for each of the Little Logic product families.

**Table 1. Little Logic Electrical-Performance Summary**

Family	Operating Voltage Range	Optimized Voltage	Propagation Delay (typical)	Output Drive	Input Tolerance	I <sub>off</sub> Circuitry
AUC	0.8 V – 2.7 V	1.8 V	2.0 ns	8 mA	3.6 V	Yes
LVC	1.65 V – 5.5 V	3.3 V	3.5 ns	24 mA	5.5 V	Yes
AHC	2.0 V – 5.5 V	5 V	5.0 ns	8 mA	5.5 V	No
AHCT	4.5 V – 5.5 V	5 V	5.0 ns	8 mA	5.5 V	No
CBT	4.5 V – 5.5 V	5 V	0.25 ns <sup>†</sup>	‡	5.5 V	Yes
CBTD	4.5 V – 5.5 V	5 V	0.25 ns <sup>†</sup>	‡	5.5 V	Yes
CBTLV	2.3 V – 3.6 V	3.3 V	0.25 ns <sup>†</sup>	‡	3.6 V	Yes

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance). The value listed is a maximum.

<sup>‡</sup> The FET switch has no output drive. The drive current at the output terminal is determined by the drive current of the device connected at the input terminal of the FET switch.

### 3.2 Propagation Delay and Maximum Operating Speed

The useful speed of a logic family is essentially the I/O propagation delay ( $t_{pd}$ ) of both low-to-high and high-to-low signal transitions from input to output. Propagation delay is affected by the number of bits switching, supply voltage, and capacitive load.

TI Little Logic data sheets specify propagation delay only for single bit switching. However, a major concern of circuit designers is the change in propagation delay when more outputs are switching. This data is very useful because a typical application would use all outputs simultaneously.

For Little Logic devices, the issue of simultaneous switching is less of a problem, as only one output is expected to switch for single gates, and a maximum of three outputs can switch in the triple gates. Therefore, simultaneous switching is not discussed in this application report.

Another important parameter that affects propagation delay is the supply voltage of the device. The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential,  $V_{GS}$ . The  $V_{GS}$  voltage is equal to the power supply voltage,  $V_{CC}$ . Therefore, a reduction in  $V_{CC}$  adversely affects the drain characteristics, which, in turn, increases the propagation delays. An increase in  $V_{CC}$  decreases the propagation delays.

Last, but not least, propagation delay is affected by capacitive loading. Typically, speeds derate linearly with increasing load capacitance. This data is very useful because a typical application requires different loading conditions than the data sheet specifies. TI data sheets do not show the performance of the device with different loads; they use only the standard load specified in the data sheet.

A true comparison of the propagation delays of the TI Little Logic devices at different voltage nodes is obtained by measuring the propagation delays at different voltage nodes when the device is under the same loading condition. Figure 3 shows typical variations of propagation delay with respect to capacitive loading for 0.8-V and 1.2-V  $V_{CC}$  for SN74AUC1G00. In both cases, a resistive load of 1 M $\Omega$  was connected between the output and ground. The data were collected under nominal-process conditions at 25°C. Similarly, Figure 4 shows typical variation of propagation delay with respect to capacitive loading for 1.5-V, 1.8-V, and 2.5-V  $V_{CC}$  for SN74AUC1G00. The data also were collected under the same conditions as for Figure 3.

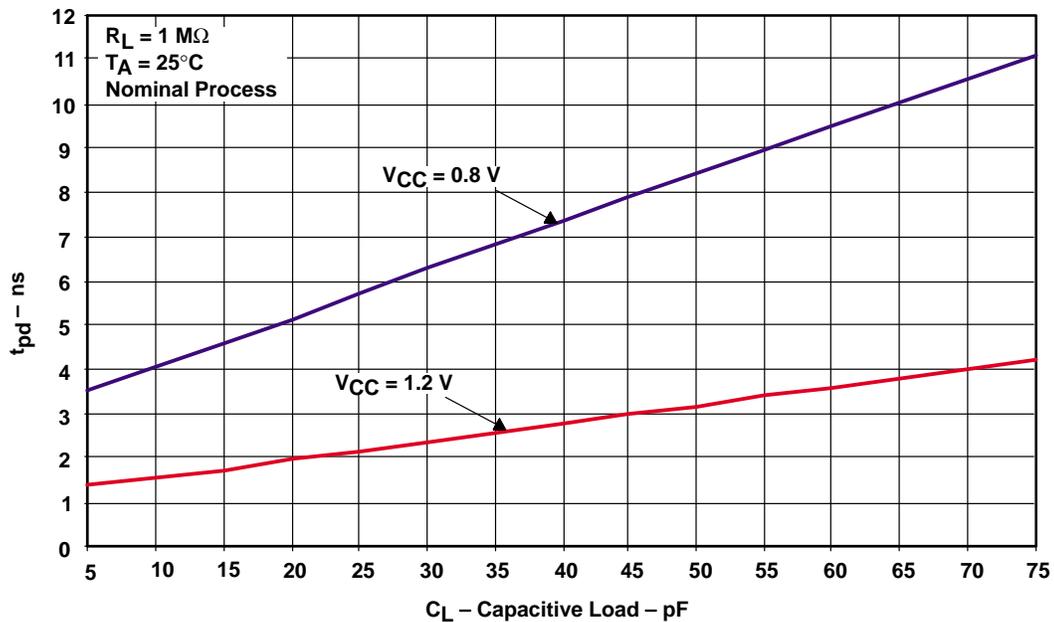


Figure 3.  $t_{pd}$  vs  $C_L$  for SN74AUC1G00 at 0.8-V and 1.2-V  $V_{CC}$

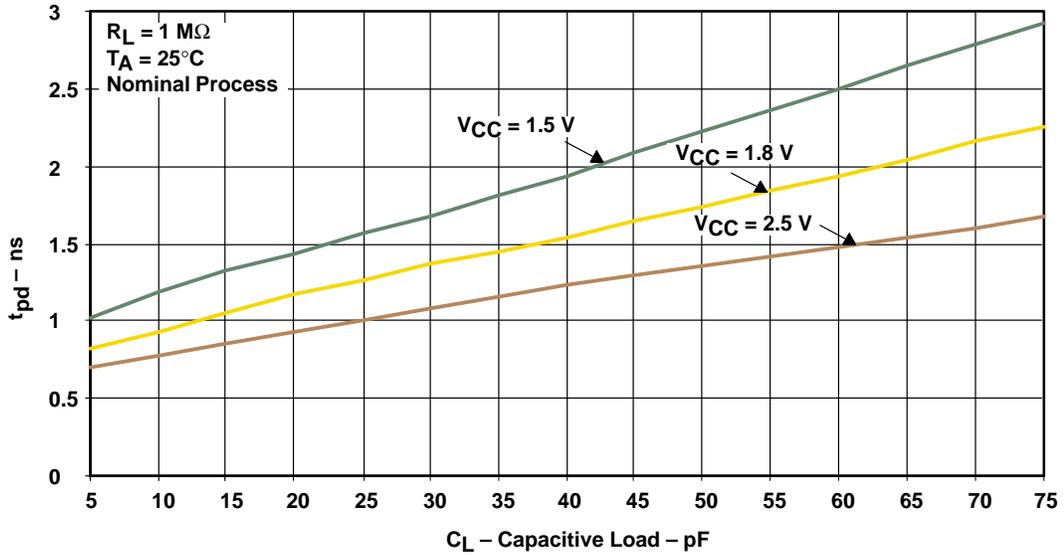


Figure 4.  $t_{pd}$  vs  $C_L$  for SN74AUC1G00 at 1.5-V, 1.8-V, and 2.5-V  $V_{CC}$

Figure 5 shows typical variations of propagation delay with respect to capacitive loading for 1.8-V and 2.5-V  $V_{CC}$  for SN74LVC1G00. In both cases, a resistive load of 1 MΩ was connected between the output and ground. The data were collected under nominal-process conditions at 25°C. Similarly, Figure 6 shows typical variation of propagation delay with respect to capacitive loading for 3.3-V and 5-V  $V_{CC}$  for SN74LVC1G00. The data also were collected under the same conditions as for Figure 5.

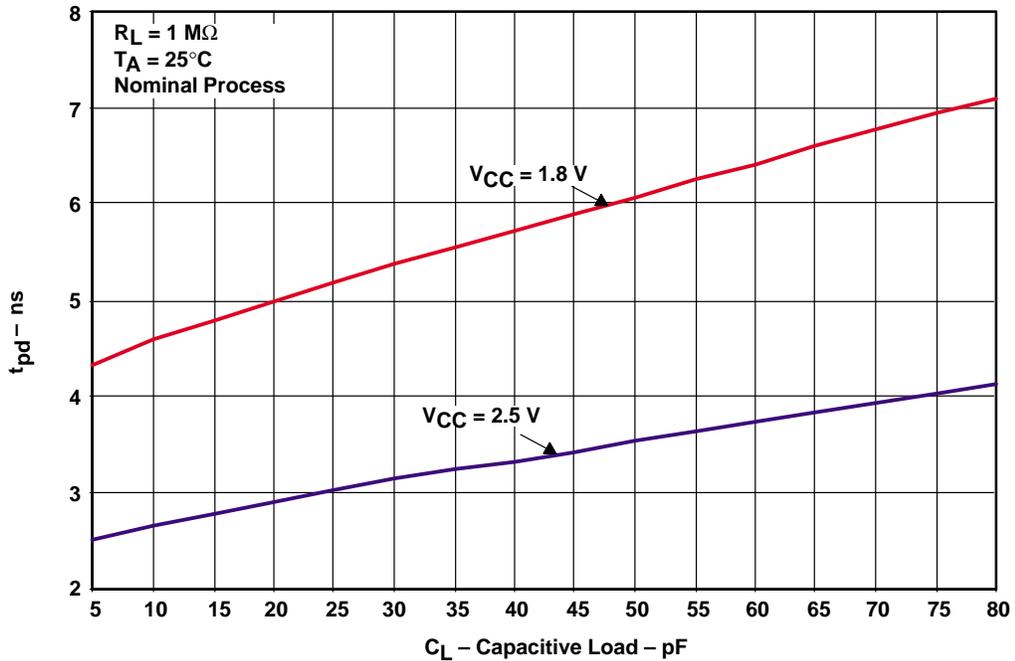
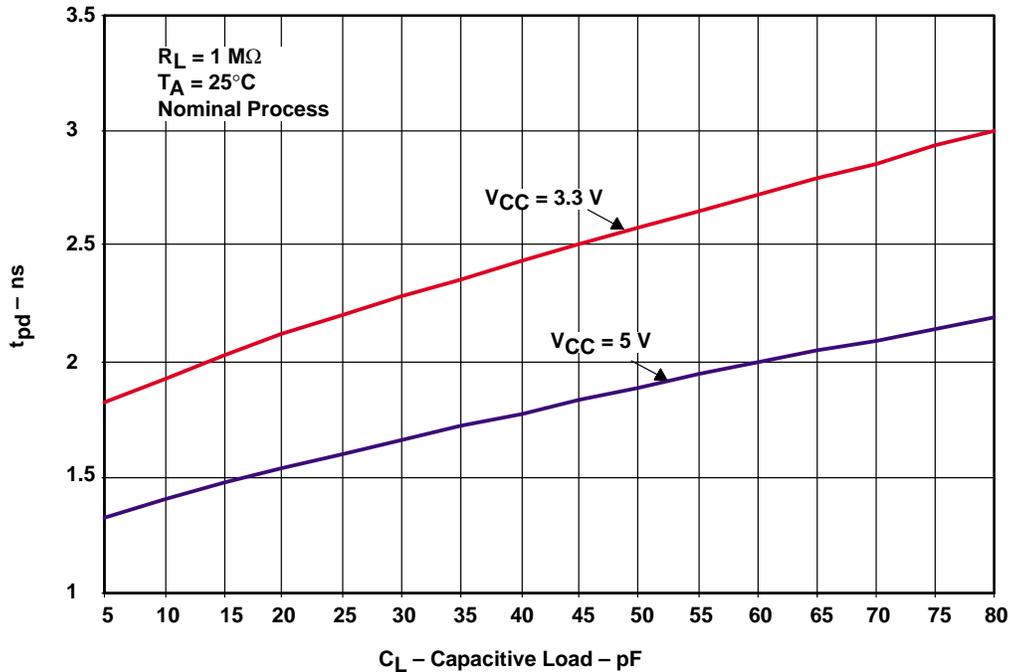


Figure 5.  $t_{pd}$  vs  $C_L$  for SN74LVC1G00 at 1.8-V and 2.5-V  $V_{CC}$



**Figure 6.  $t_{pd}$  vs  $C_L$  for SN74LVC1G00 at 3.3-V and 5-V  $V_{CC}$**

System designers usually are concerned about maximum operating frequencies of devices because this determines the maximum switching rate that the device will tolerate in the application. However, in the system application, the supply voltage and output load of the device affects the maximum operating frequency of a logic device. TI does not specify maximum operating frequency for the nonclocked logic devices (for example, NAND gates). For clocked logic devices (for example, D-type flip-flops) the maximum operating frequency is specified as  $f_{max}$  or  $f_{clock}$ .

As a rule of thumb, the maximum operating frequency for a nonclocked (gate) device is about the same as the maximum operating frequency for a clocked (D-type flip-flop) device of the same family. This is especially true if the complexity of the nonclocked device is less than the complexity of the clocked device. Also, as another rule of thumb, the maximum operating frequency for a nonclocked device can be computed from the low-to-high propagation delay ( $t_{PLH}$ ) and the high-to-low propagation delay ( $t_{PHL}$ ). The sum of the maximum  $t_{PLH}$  and  $t_{PHL}$  is the approximate minimum period for the device. Therefore, the inverse of the sum is the approximate maximum operating frequency of the device. For devices that do not specify  $t_{PLH}$  and  $t_{PHL}$ , but specify the  $t_{pd}$ , the minimum period is twice the specified  $t_{pd}$ .

Laboratory data show TI Little Logic devices operate at high frequencies (see Table 2). The data were collected for different two-input positive-OR Little Logic gates at different supply-voltage nodes with no load at the output of the device. Note that, in real system applications, with a capacitive load at the output of the device, the operating frequency will be derated according to the load at the output.

**Table 2. Laboratory-Measured Frequencies for TI Little Logic Devices**

Device	Laboratory-Measured Operating Frequency (MHz)				
	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V
SN74AUC1G32	150	>200†	>200†	‡	‡
SN74LVC1G32	‡	70	170	>200†	>200†
SN74AHC1G32	‡	‡	130	170	>200†

† Data were collected only up to 200 MHz.

‡ Device is not recommended for operation at this voltage node. Functional operation of the device at this node is not specified.

### 3.3 Input and Output Transition Time

A slow-input test sheds light on the integrity of the device, specifically, how the device responds when the input voltage is ramped slowly from 0 V to V<sub>CC</sub> and, conversely, when the input voltage is ramped slowly from V<sub>CC</sub> to 0 V. As the input voltage is ramping, the output voltage is monitored and, when it begins to switch, the waveform is observed. If monotonic behavior is observed as the output traverses the threshold region, the device may be sensitive to a slow input, which can cause the output to oscillate or cause false triggering.

Table 3 shows the maximum input transition rise or fall rate for some TI Little Logic devices at different voltage nodes. At the optimized voltage node, all TI Little Logic devices show noncritical responses to the slow-input test.

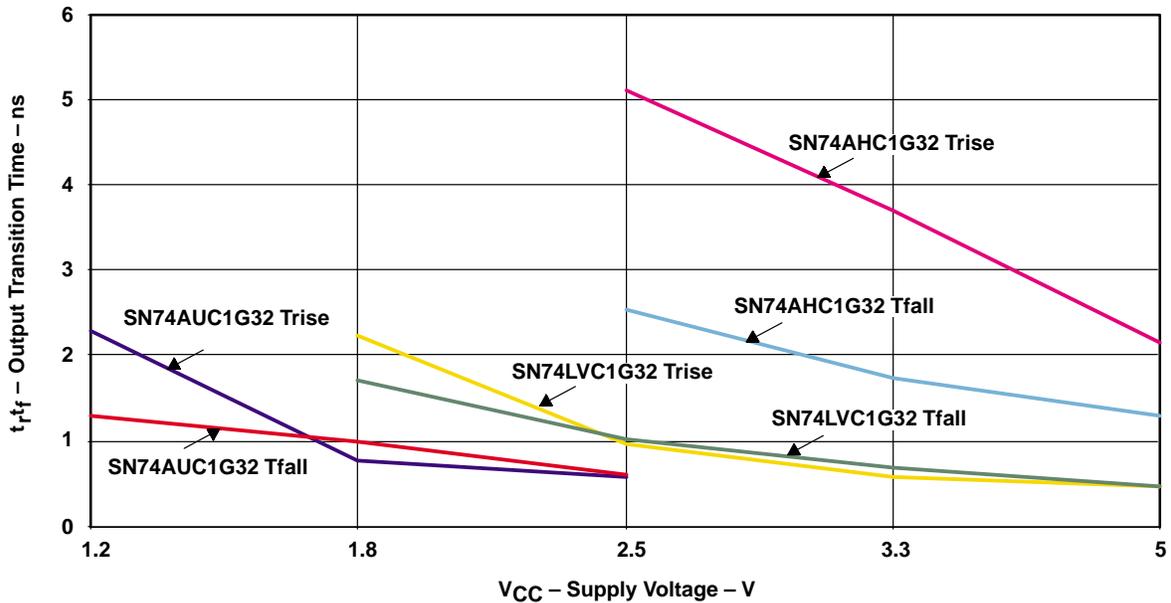
**Table 3. Input Transition Rates for TI Little Logic Devices**

Device	Input Transition Rise or Fall Rate, $\Delta t/\Delta V$ (ns/V)				
	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V
SN74AUC1G32	20	20	20	‡	‡
SN74LVC1G32	†	20	20	10	5
SN74AHC1G32	†	†	100	100	20

‡ Device is not recommended for operation at this voltage node. Functional operation of the device at this node is not specified.

Output transition rate also is an important factor in systems circuit design. The systems designer must ensure that the maximum output transition rate of the driving device be within the input transition rate of the receiving device. However, output transition rate is very much dependent on the load at the output of the device.

Figure 7 shows typical output transition rise times (t<sub>r</sub>) and output transition fall times (t<sub>f</sub>) for some TI Little Logic devices. The data were taken with a 15-pF capacitor and a 50-kΩ resistor, connected from the output of the device to ground. All output transition-time measurements were done from the 20% value to the 80% value of the switching levels.

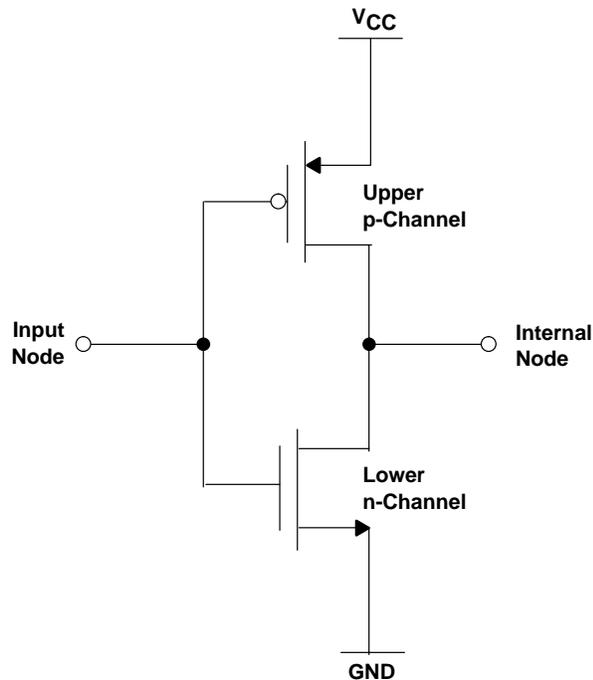


**Figure 7. Output Transition Time for TI Little Logic Devices**

### 3.4 Power Consumption

Several factors affect the current consumption of a device: frequency of operation, number of outputs switching, load capacitance, junction temperature, input edge rate, input voltage level for lows and highs, ambient temperature, and thermal resistance of the device. The effect of switching rate, number of switching bits, input edge rate, and input voltage level to current consumption can be explained by the structure of CMOS inputs.

A typical CMOS input state consists of an upper p-channel transistor and a lower n-channel transistor, connected as shown on Figure 8. If the input voltage is the same as the supply voltage, the p-channel transistor is not conducting, and almost no current flows from  $V_{CC}$  to the output node (or GND). Similarly, the n-channel transistor stops conducting when the input voltage is at GND potential. In this case, little or no current flows from the output node (or  $V_{CC}$  node) to the GND node.



**Figure 8. CMOS Input-Stage Circuit**

If the input voltage is not at the same potential as the supply voltage or GND, the transistors of the input stage operate in a linear region, and both transistors will be more or less conducting. As a result of this situation, the current consumption in static and dynamic operation increases, if the input level is not the same as the supply or the GND potential. During device operation, an increase in the switching rate or number of switching bits, or a decrease in the input edge rate, results in an increase in the time that the n-channel and p-channel transistors stay in the linear region. Thus, current consumption increases.

The current consumption of digital CMOS circuits increases linearly with increasing frequency of operation. Figures 9 through 11 show typical power consumption with single-output switching for different TI family Little Logic devices. The data were collected with one input switching from ground to  $V_{CC}$ . No load was connected at the output and an input edge rate of 1 ns/V was used.

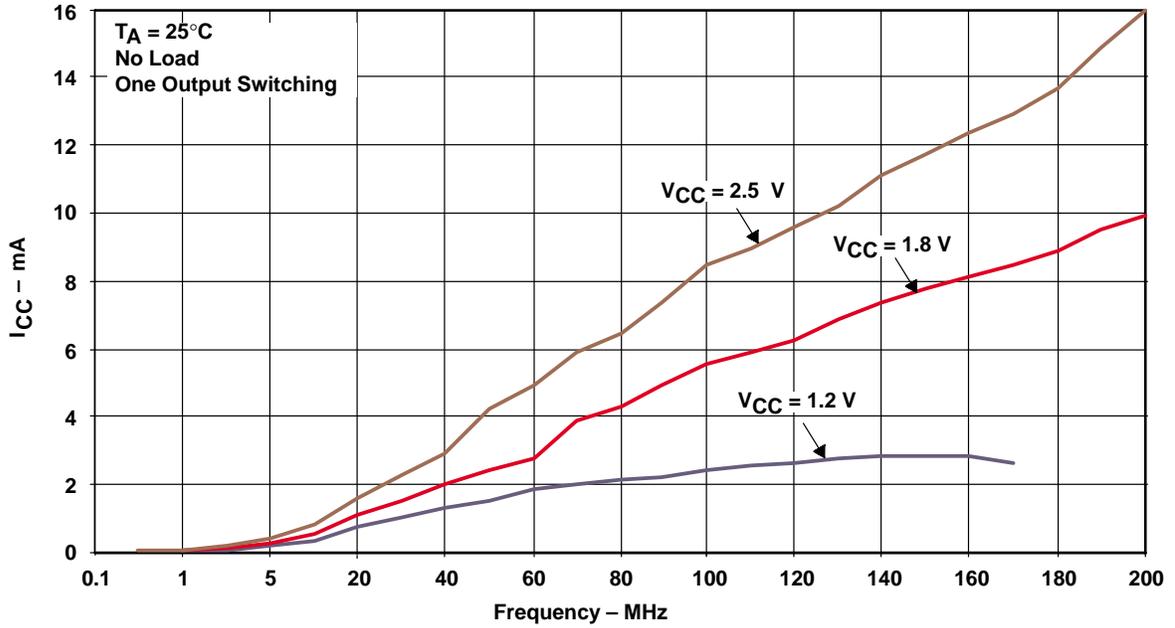


Figure 9. Typical Current Consumption for SN74AUC1G32

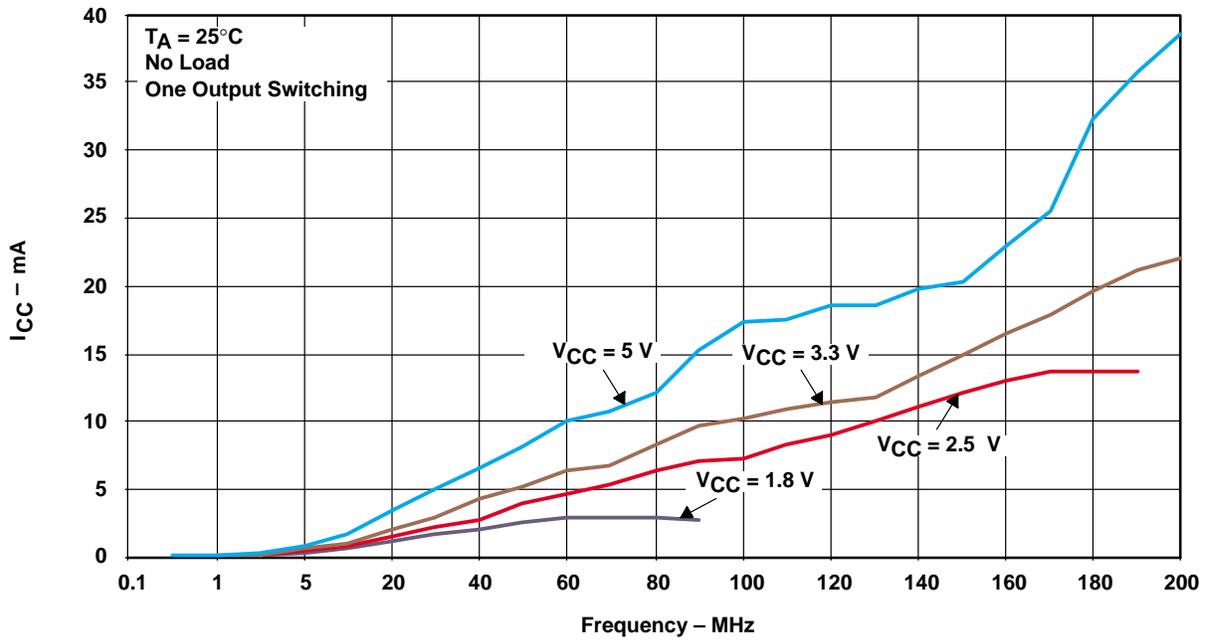
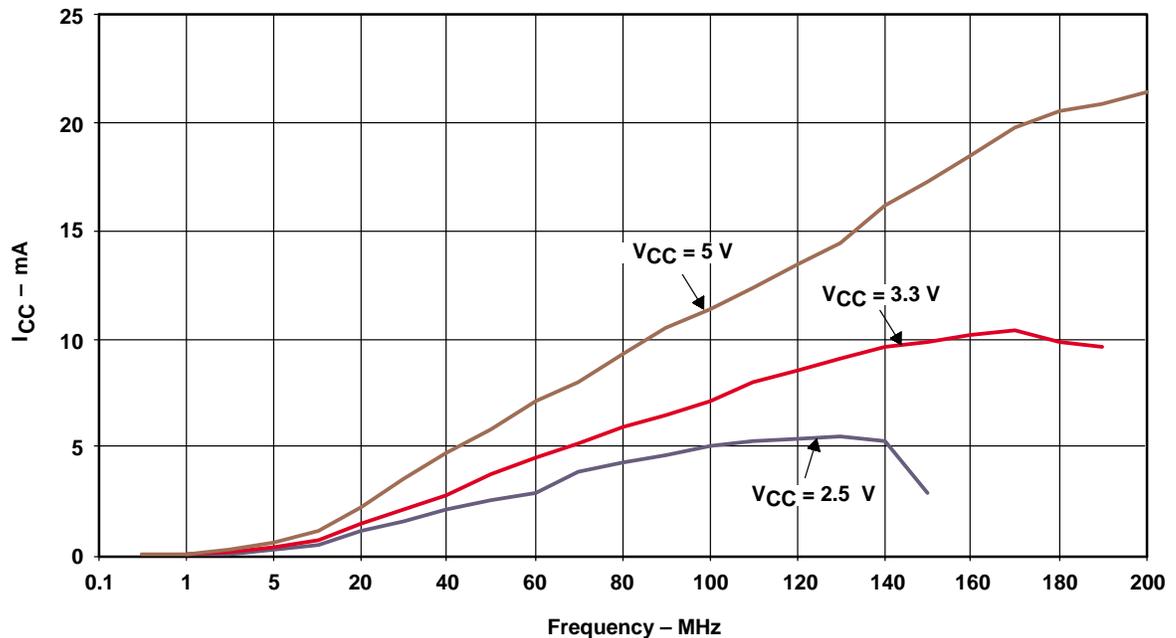


Figure 10. Typical Current Consumption for SN74LVC1G32



**Figure 11. Typical Current Consumption for SN74AHC1G32**

The current-consumption data were collected, up to a frequency of 200 MHz, for those TI Little Logic families that are operable up to 200 MHz. For the Little Logic devices used in this test that do not operate up to 200-MHz frequency, the data were collected up to and beyond the frequency when the  $V_{OH}$  and  $V_{OL}$  failed data-sheet limits for a typical device. For example, at 1.8-V  $V_{CC}$ , the SN74LVC1G32 has been tested to operate only up to 70 MHz (see Table 2). However, the  $I_{CC}$  vs frequency data were collected for frequencies up to 90 MHz (see Figure 10).

If the input signal into a Little Logic device switches faster than the maximum tested operating frequency, the current consumption begins to reduce, and the output of the device does not switch from rail to rail. Beyond the maximum tested operating frequency, the output high will begin to drop from  $V_{CC}$  and the output low will begin to rise higher than GND. For example, at 2.5-V  $V_{CC}$ , the maximum tested frequency for the SN74AHC1G32 is 130 MHz. At this frequency the current consumption is at its peak. At about 140 MHz (and beyond), the current consumption drops rapidly (see Figure 11).

The current-consumption data presented in Figures 9 through 11 is important to the system designer for determining how much energy is consumed during operation (especially important for battery-powered portable applications) and how much heat the integrated circuit dissipates (especially important in personal-computer applications). However, it is misleading to compare the current consumption for the different-family devices at a specific voltage node, as the different families are optimized at different voltages.

A more realistic assessment is to compare the power-dissipation capacitance ( $C_{pd}$ ) of the different devices at their optimized voltage nodes. Comparing the  $C_{pd}$  at the optimized voltage nodes is more sensible than comparing  $I_{CC}$  because  $C_{pd}$  is voltage-normalized. Figure 12 shows a plot of the typical  $C_{pd}$  versus frequency for the SN74AUC1G32, SN74LVC1G32, and SN74AHC1G32 at their respective optimized voltage nodes. The AUC Little Logic devices are optimized at 1.8-V  $V_{CC}$ , the LVC Little Logic devices are optimized at 3.3-V  $V_{CC}$ , and the AHC Little Logic devices are optimized at 5-V  $V_{CC}$ .

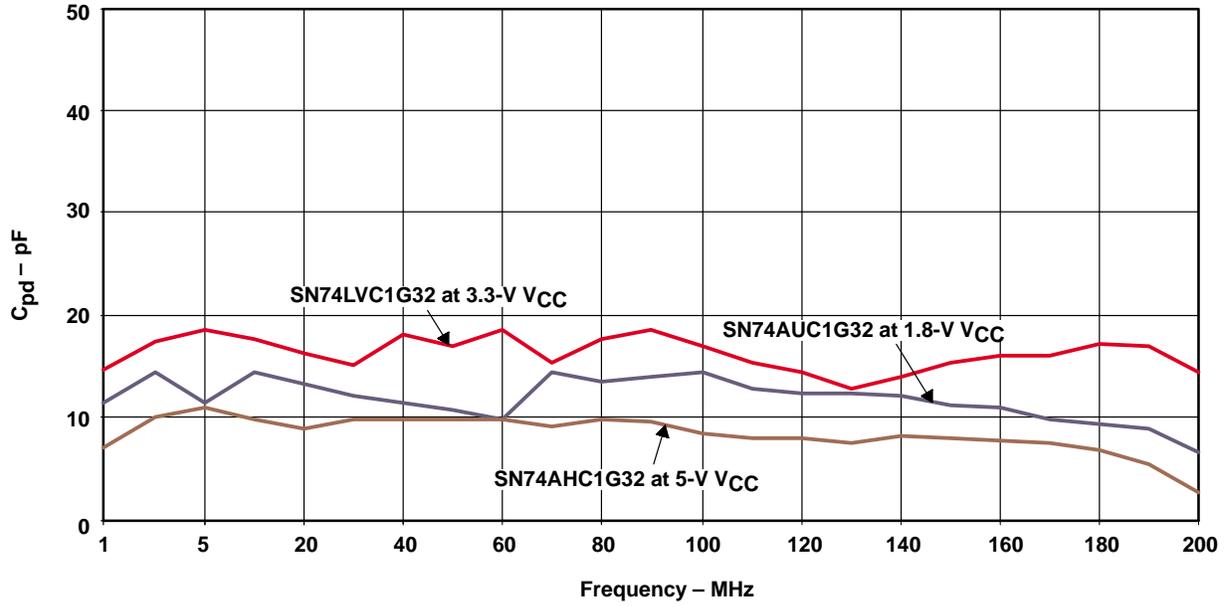


Figure 12. Typical Power-Dissipation Capacitance for TI Little Logic Devices

## 4 Package Information

TI Little Logic devices are available in several small-pin-count package options (see Figure 13). Leadframe devices are offered in 5-pin SOT-23 (DBV), 5-pin SC-70 (DCK), 6-pin SOT-23 (DBV), 6-pin SC-70 (DCK), 8-pin SM-8 (DCT) and 8-pin US-8 (DCU). Wafer chip-scale packaging is available with TI NanoStar (YEA) and NanoFree (YZA) in 5-, 6-, and 8-ball solder-bump configurations. The mechanical data information for these packages is provided in Appendix A of this application report.

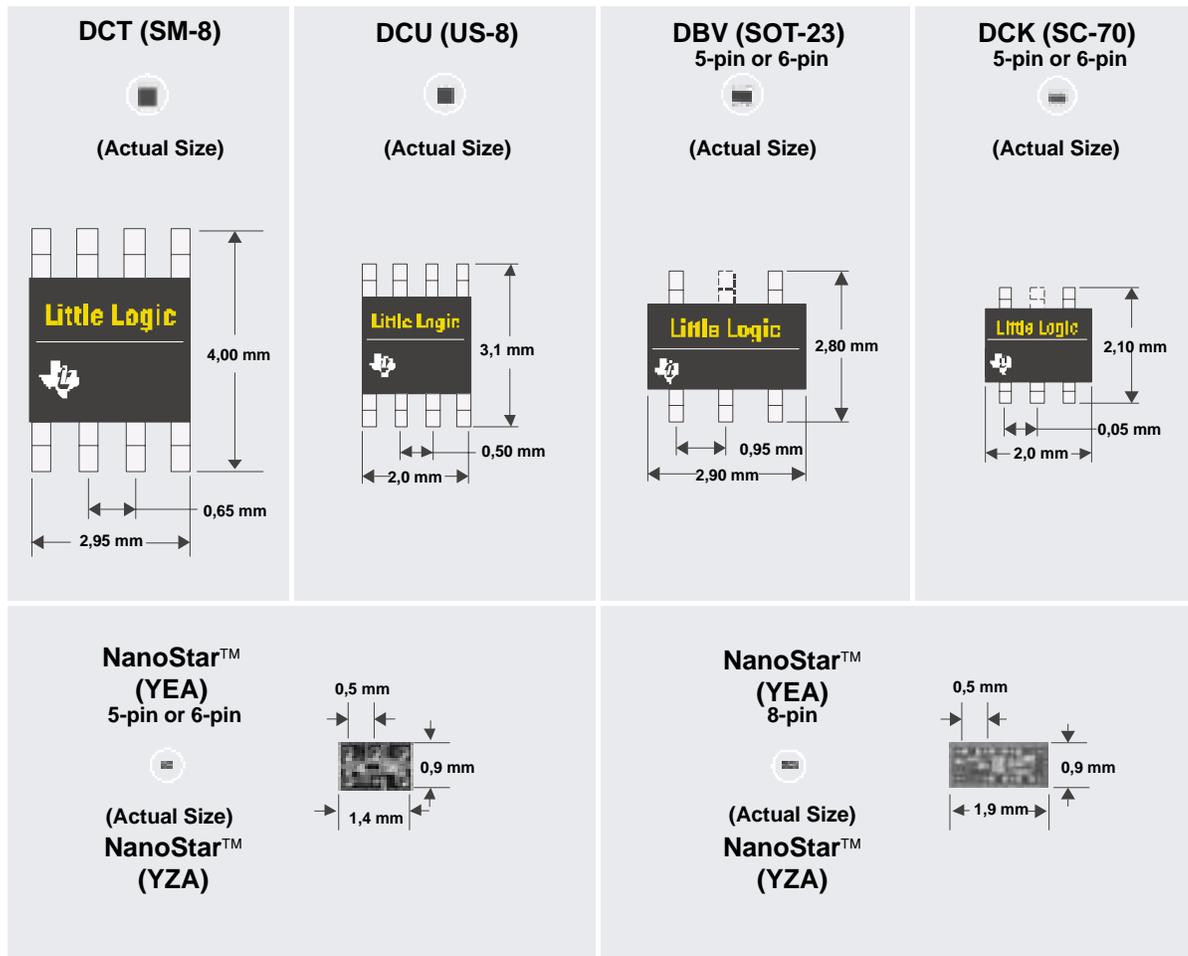


Figure 13. TI Little Logic Package Options

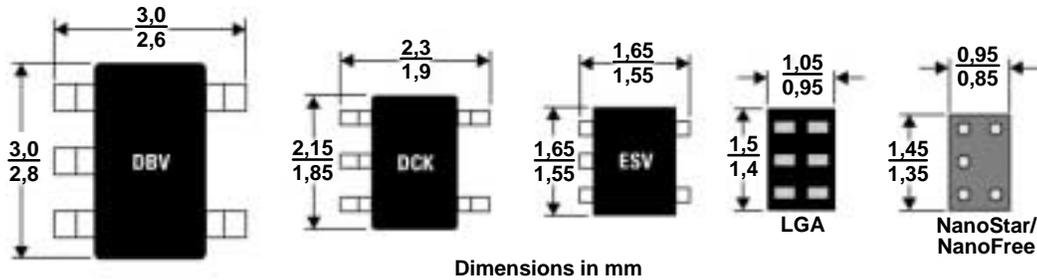
Table 4 gives the physical properties of the TI Little Logic device packages.

Table 4. TI Little Logic Packages Size and Weight

Package Data	SM-8 (DCT)	US-8 (DCU)	SOT-23 (DBV)	SC-70 (DCK)	DSBGA (YEA/YZA)	DSBGA (YEA/YZA)
	8 Pin	8 Pin	5 or 6 Pin	5 or 6 Pin	5 or 6 Pin	8 Pin
Length (mm)	2.95 ±0.20	2.00 ±0.10	2.90 ±0.10	2.00 ±0.15	1.40 ±0.05	1.90 ±0.05
Width (mm)	4.00 ±0.25	3.10 ±0.10	2.80 ±0.20	2.10 ±0.20	0.90 ±0.05	0.90 ±0.05
Height (mm)	1.30	0.90	1.20	0.95	0.50	0.50
Footprint area (mm <sup>2</sup> )	11.80	6.20	8.12	4.20	1.26	1.26
Weight (g)	0.0206	0.0095	0.0135	0.006	0.000995	0.0013

NanoStar and NanoFree share the same package dimensions. The only difference between the two packages is their solder-bump composition. NanoStar is processed with SnPb, while NanoFree provides an environment-friendly Pb-free alternative. Both packages comply with JEDEC MO-211.

Figure 14 shows the comparison between the industry-standard 5-pin DBV and DCK packages, competitors' 5-pin ESV and QFN packages, and TI 5-pin NanoStar or NanoFree package option. TI 5-pin NanoStar (or NanoFree) is 13% smaller than competitor's 6-pin LGA package and 70% smaller than the industry-standard 5-pin DBV package.



**Figure 14. Little Logic Industry Packaging Comparison**

Table 5 compares the physical properties of the TI 5-pin Little Logic NanoStar package with the industry standard 5-pin DBV and DCK packages, and competitors' 5-pin ESV and 6-pin LGA packages.

**Table 5. Little Logic Package Size and Weight Comparison**

Package Data	SOT-23 (DBV) TI	SC-70 (DCK) TI	ESV	LGA	DSBGA (YEA/YZA) TI
Length (mm)	2.90 ±0.10	2.00 ±0.15	1.60 ±0.05	1.45 ±0.05	1.40 ±0.05
Width (mm)	2.80 ±0.20	2.10 ±0.20	1.60 ±0.05	1.00 ±0.05	0.90 ±0.05
Height (mm)	1.20	0.95	0.55	0.55	0.50
Footprint area (mm <sup>2</sup> )	8.12	4.20	2.56	1.45	1.26
Weight (g)	0.0135	0.006	=0.003	0.002	0.000995

## 5 Features and Benefits

Table 6 summarizes the features and benefits of the Little Logic devices.

**Table 6. Features and Benefits of TI Little Logic Devices**

FEATURES	BENEFITS
Low power consumption	Use in portable electronics and battery-operated systems.
Fewer outputs switching. High ground (power) pins to output pins ratio.	Less switching noise
Small, low-profile packages	Saves board space. Simplifies large PCB routing. Use as “quick fix” for design errors.
Cost effective	Inexpensive compared to redesign. Used as “quick fix” for design errors. Reduces time-to-market and maximized design investment in all types of electronic systems.

## 6 Conclusion

The Texas Instruments Little Logic devices provide simple, cost-effective solutions to portable electronics and battery-operated systems and facilitate quick fixes in system design errors. Their small low-profile packages allow for board-space savings and large PCB routing flexibility. Further, the Little Logic devices have a higher ground (power) pins to output pins ratio, which further reduces the already-low switching noise. TI offers Little Logic devices in the AUC, LVC, AHC, AHCT, CBT, CBTLV, and CBTD families. The features, electrical characteristics, and competitive analysis of the TI Little Logic devices are presented in this application report.

## 7 Frequently Asked Questions (FAQs)

**Question 1:** *What are Little Logic devices?*

**Answer:** Little Logic devices are single gates, dual gates, or triple gates that are packaged in extremely small sizes. They enable simple design routing, ASIC design development, and significantly reduce redesign time, effectively extending the life of electronic products. With the miniaturization of portable electronics, these devices are ideal for applications where board space is limited.

**Question 2:** *How do I get copies of the Little Logic data sheets and samples?*

**Answer:** The Little Logic data sheets can be obtained by accessing <http://www.ti.com>. Samples of the Little Logic devices can be obtained by contacting your local TI sales representative.

**Question 3:** *What Little Logic devices does TI offer?*

**Answer:** A complete list of all the Little Logic devices from TI is listed on the Internet. The list can be viewed, by device family, by accessing <http://www.ti.com>.

**Question 4:** *How do I get copies of Little Logic HSPICE and IBIS models?*

**Answer:** The HSPICE models for Little Logic devices can be obtained by contacting your local TI sales representative. The IBIS model can be obtained by accessing <http://www.ti.com>.

**Question 5:** *Do TI Little Logic devices have bus-hold circuits at the input?*

**Answer:** No, TI Little Logic devices do not have bus-hold cells at the input. Bus-hold is a feature commonly used in bus applications. The bus-hold circuit holds the last known state of the input and eliminates the need for external resistors on unused or floating input pins. This feature is found in some TI Widebus™ devices. The “H” in a TI Widebus device name indicates bus-hold. For example, the SN74LVC16245A has no bus-hold, while the SN74LVCH16245A does.

**Question 6:** *What are the advantages of using Little Logic devices?*

**Answer:** The advantages of using the Little Logic devices include:

- Lower power consumption makes them ideal for use in portable electronics and battery-operated systems.
- Fewer outputs switching and higher ground (power) pins to output pins ratio further reduces already low switching noise.
- Board space is saved, and PCB routing is simplified.
- Capability for fixing design errors is flexible, and redesign cost is lower.

## 8 References

1. *Little Logic Data Book* (SCED010), November 2001.
2. *Application of the Texas Instruments AUC Sub-1-V Little Logic Devices* application report, literature number SCEA027.

## 9 Glossary

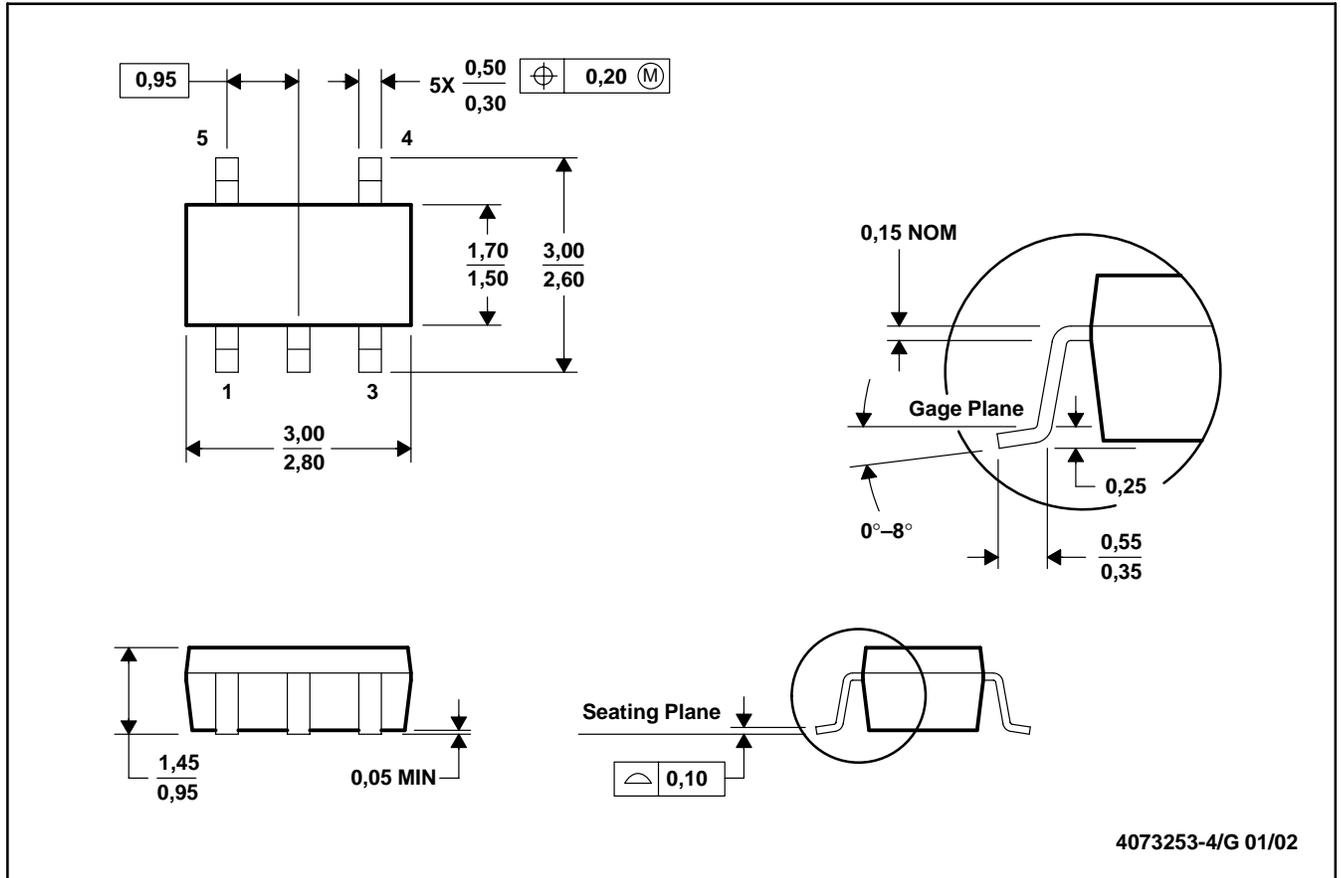
AHC	Advanced high-speed CMOS logic
AHCT	Advanced high-speed CMOS TTL logic
ASIC	Application-specific integrated circuits
AUC	Advanced ultra-low-voltage CMOS logic
CBT	Crossbar technology logic
CBTLV	Low-voltage crossbar technology logic
CMOS	Complementary metal-oxide silicon; a device technology that has balanced drive outputs and low power consumption
$C_{pd}$	Power dissipation capacitance. Used to determine the no-load dynamic power dissipation per logic function. $P_D = C_{pd} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$ .
FET	Field-effect transistor
$f_{max}$	Maximum operating frequency. The highest rate at which the clock input of a bistable circuit can be driven through its required sequence, while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
IBIS	I/O buffer information specification
$I_{OFF}$	Input/output power-off leakage current. The maximum leakage current into/out of the input/output transistors when forcing the input/output to 2.7 V and $V_{CC} = 0$ V
JEDEC	Joint Electron Device Engineering Council
LGA	Land grid array
LVC	Low-voltage CMOS logic
PCB	Printed circuit board
SPICE	Simulation program with integrated-circuit emphasis
$t_f$	Fall time. The time interval between two reference points (20% and 80%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level

TI	Texas Instruments
$t_{pd}$	Propagation delay time. The time between the specified reference points on the input and output voltage waveforms, with the output changing from one defined level (high or low) to the other defined level ( $t_{pd} = t_{PHL}$ or $t_{PLH}$ )
$t_{PHL}$	Propagation delay time, high-to-low level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.
$t_{PLH}$	Propagation delay time, low-to-high level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level
$t_r$	Rise time. The time interval between two reference points (20% and 80%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level
TTL	Transistor-transistor logic
$V_{OH}$	High-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output.
$V_{OL}$	Low-level output voltage. The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output.

## Appendix –Package Mechanical Data

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



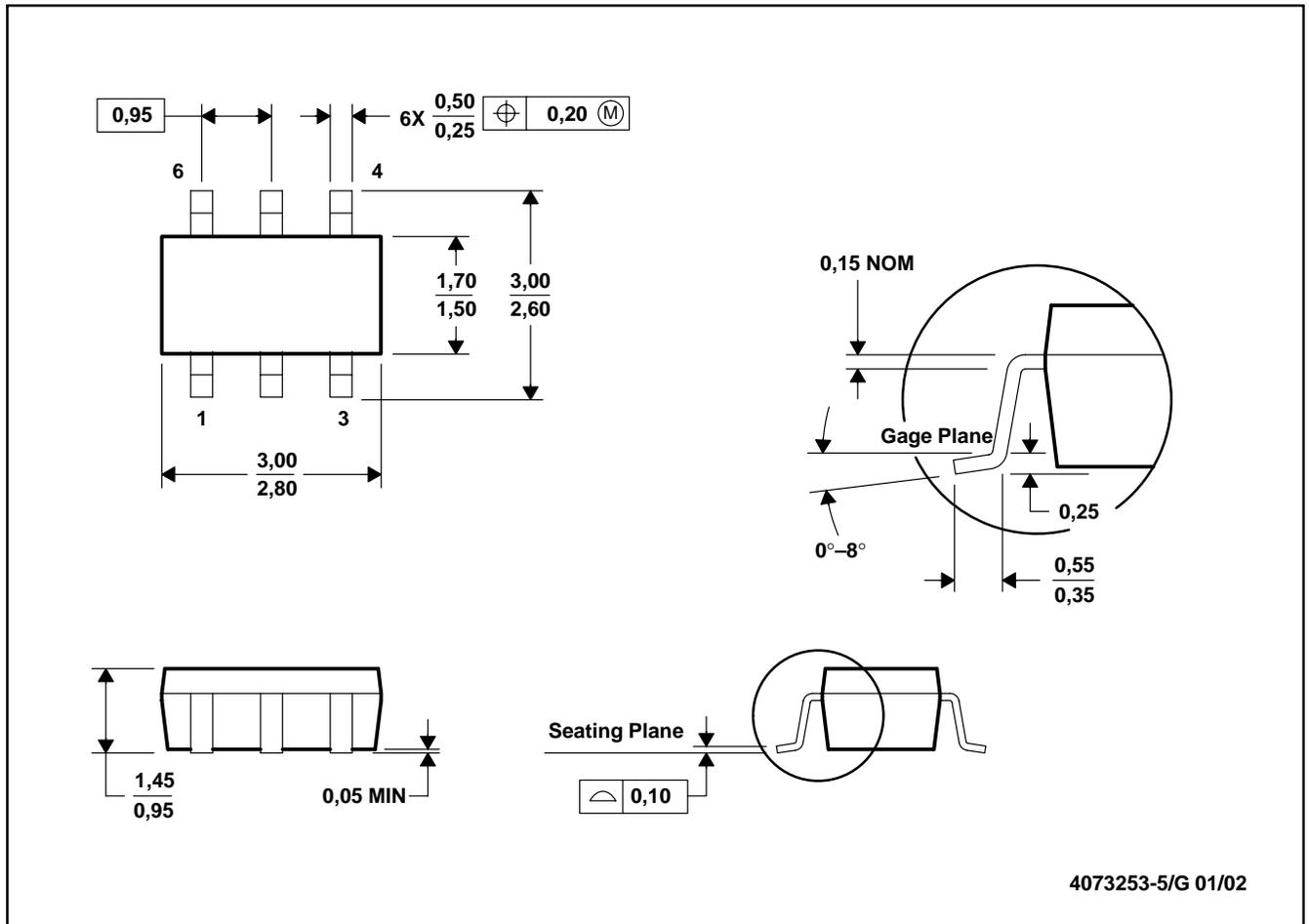
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-178

Figure 15. 5-Pin DBV – Small-Outline Package (SOP)



DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE

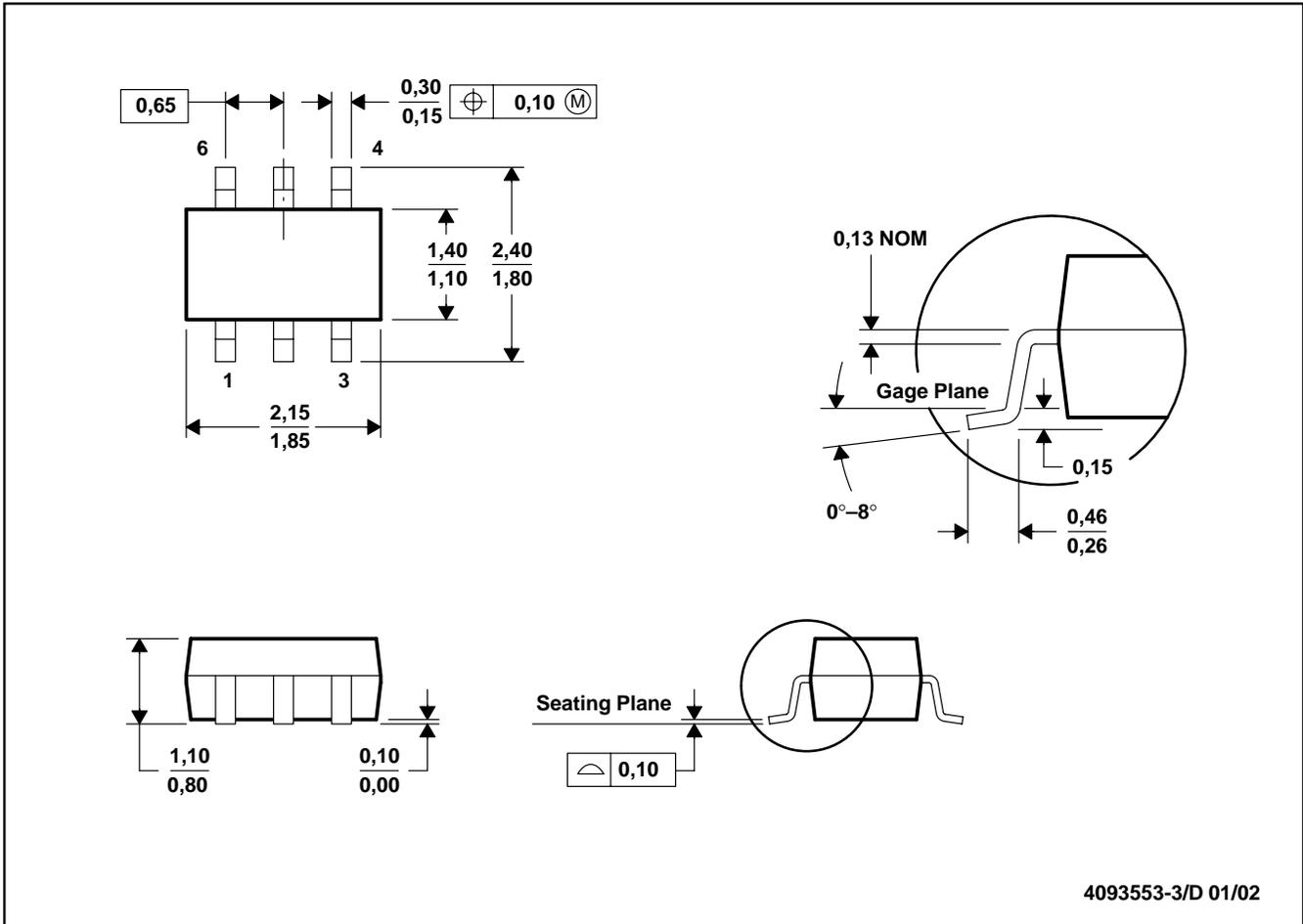


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

Figure 17. 6-Pin DBV – Small-Outline Package (SOP)

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

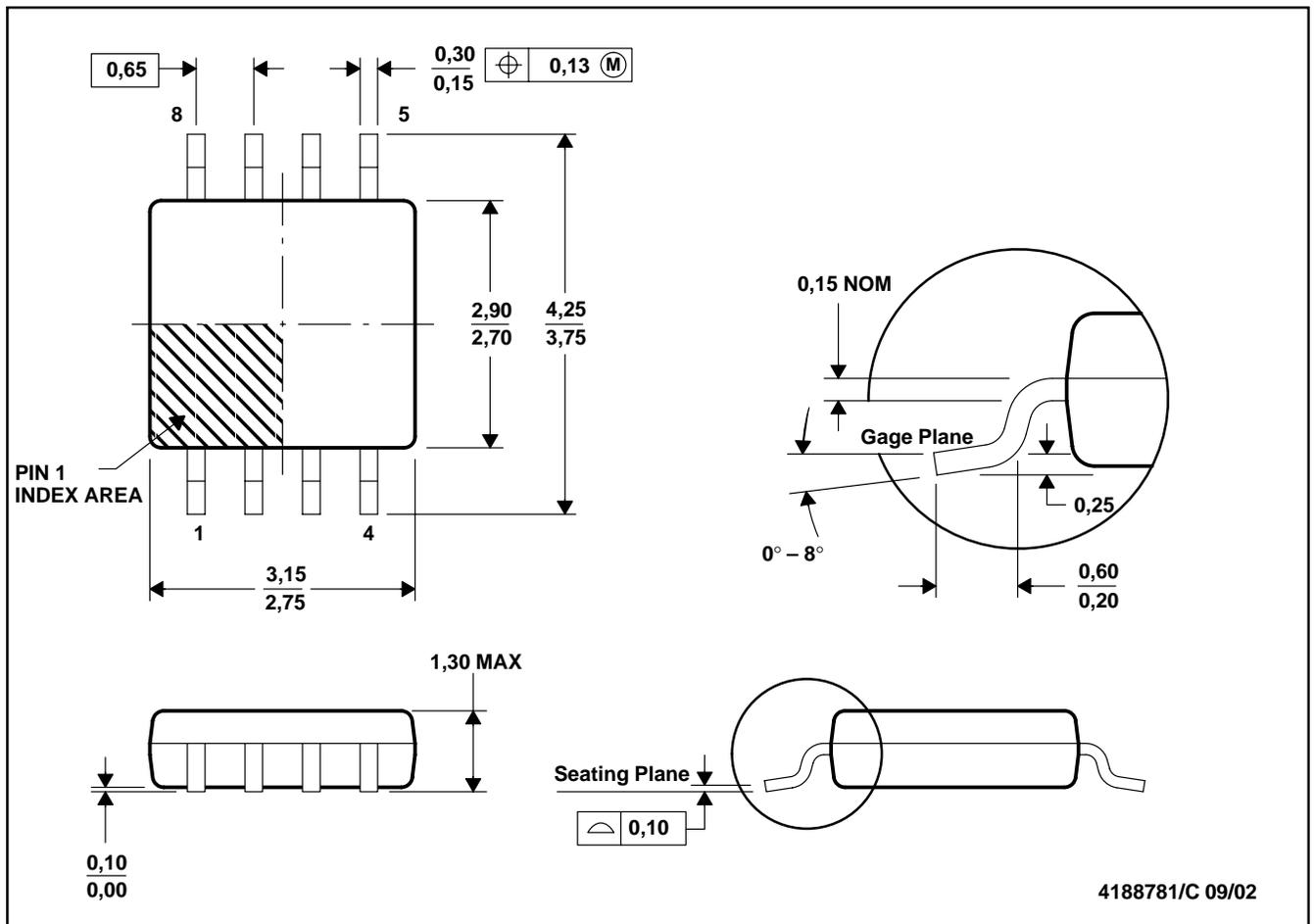


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-203

Figure 18. 6-Pin DCK – Small-Outline Package (SOP)

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

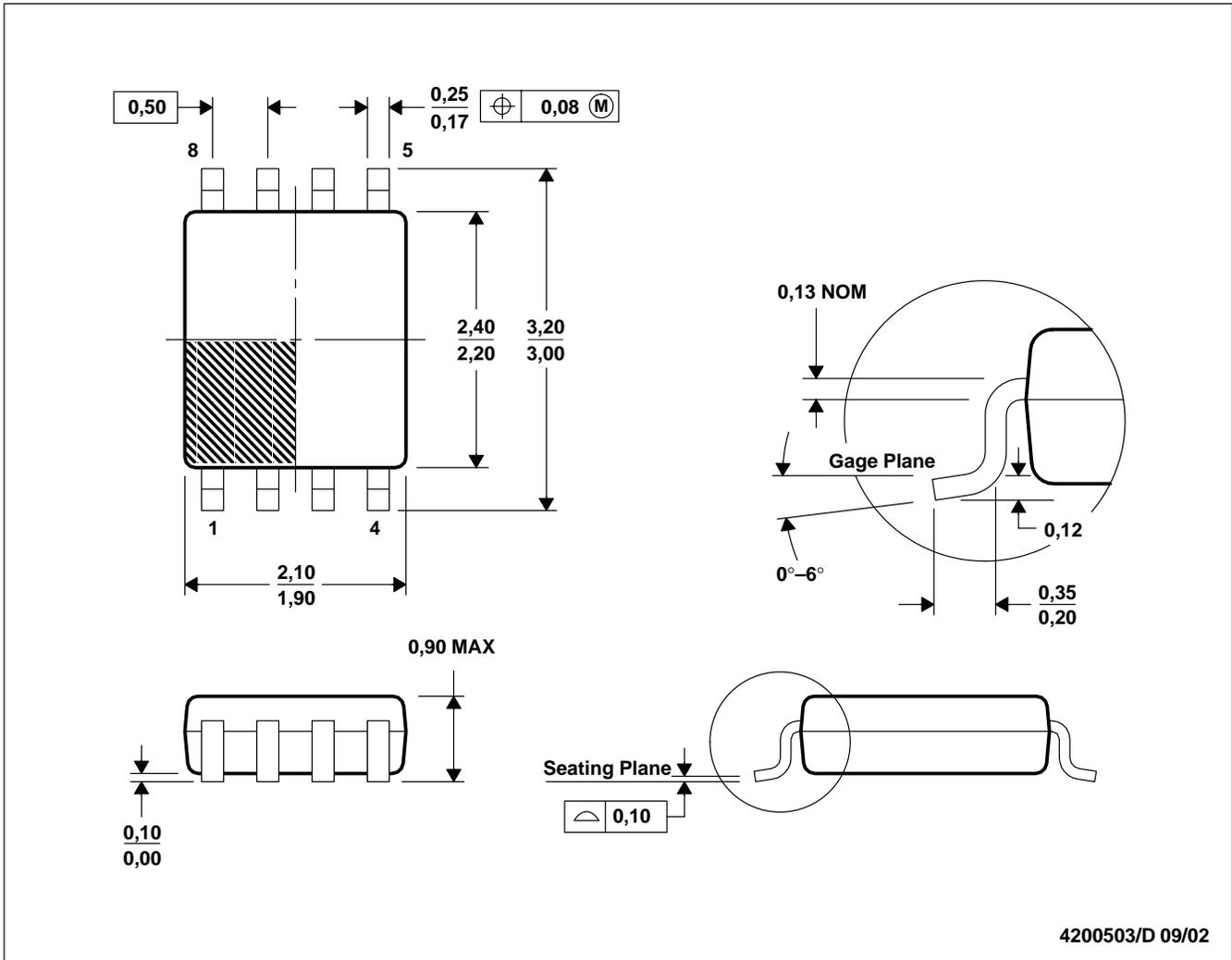


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-187 variation DA.

Figure 19. 8-Pin DCT – Shrink Small-Outline Package (SSOP)

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

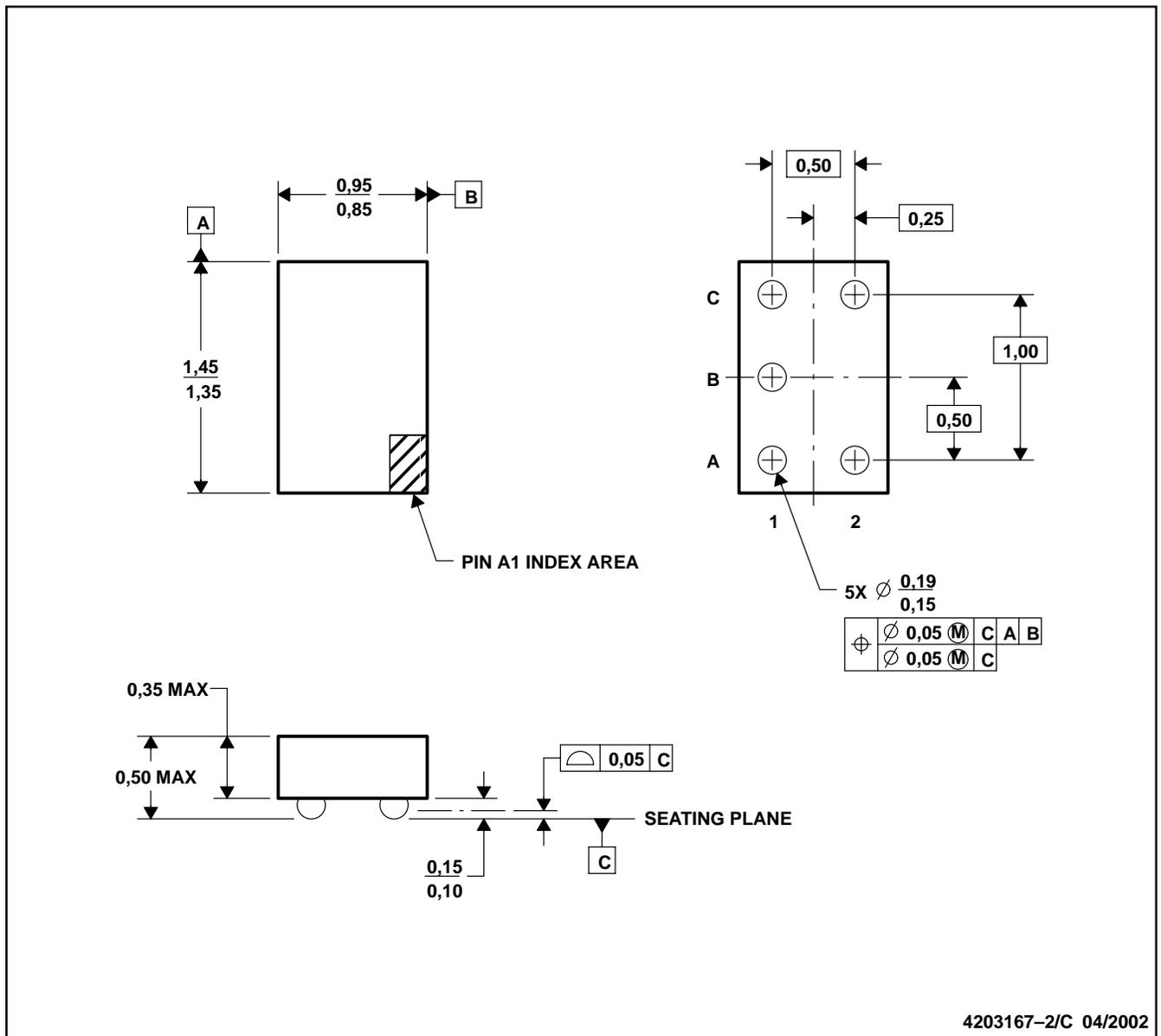


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-187

**Figure 20. 8-Pin DCU – Very Thin Shrink Small-Outline Package (VSSOP)**

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



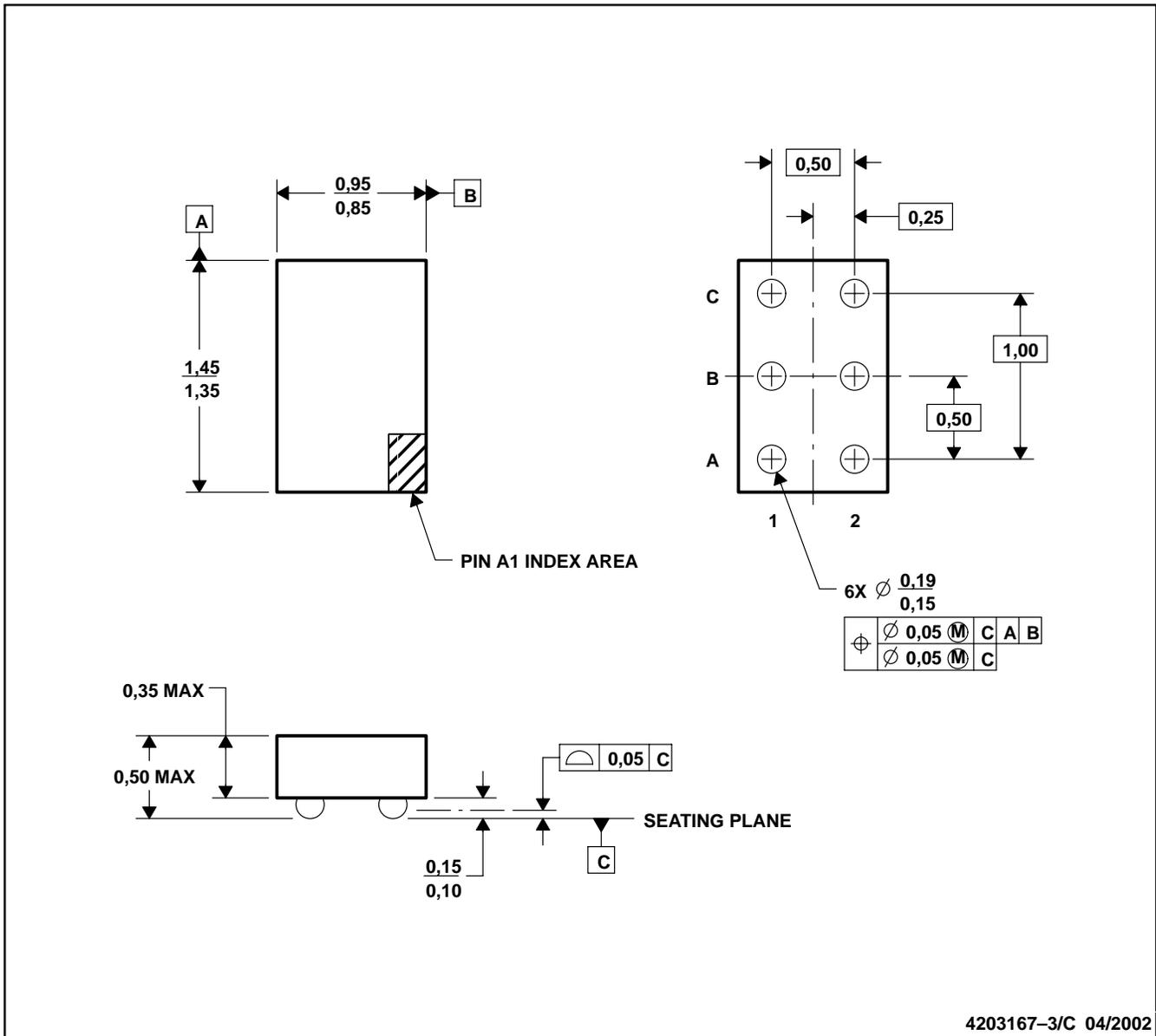
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. NanoStar™ package configuration.  
 D. Package complies to JEDEC MO-211 variation EA.  
 E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

**Figure 21. 5-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†**

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

YEA (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4203167-3/C 04/2002

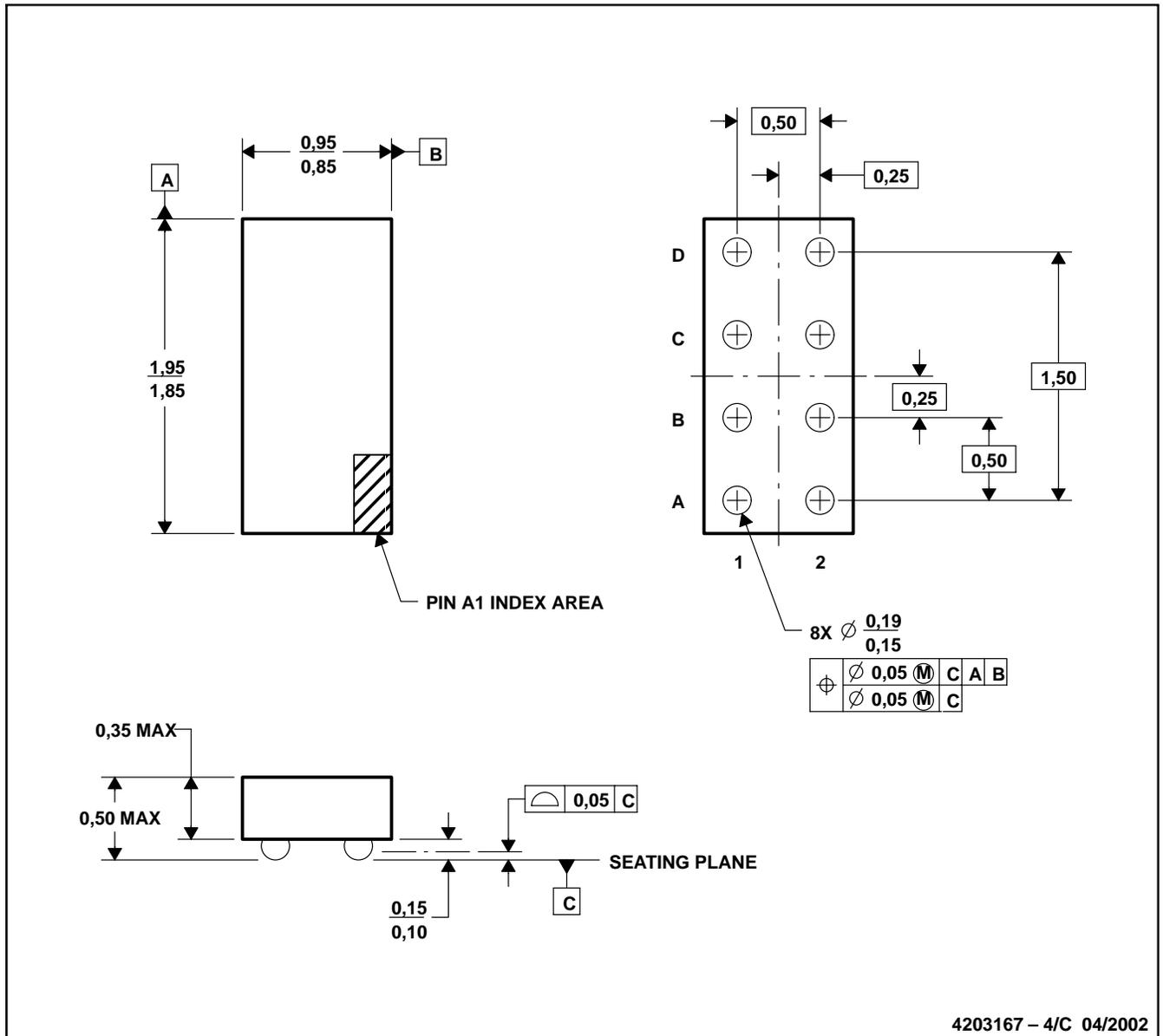
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EA.
  - E. This package is tin-lead (SnPb). Refer to the 6 YZA package (drawing 4204151) for lead-free.

**Figure 22. 6-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†**

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

YEA (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. NanoStar™ package configuration.  
 D. Package complies to JEDEC MO-211 variation EB.  
 E. This package is tin-lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead-free.

**Figure 23. 8-Pin YEA (NanoStar™) – Die-Size Ball Grid Array (DSBGA)†**

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265