

***Dynamic Output Control (DOC™)
Circuitry
Technology and Applications***

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Abstract

Texas Instruments (TI™) next-generation logic is called the Advanced Very-low-voltage CMOS (AVC) family. The AVC family features TI's Dynamic Output Control (DOC™) circuit (patent pending). DOC circuitry automatically lowers the output impedance of the circuit at the beginning of a signal transition, providing enough current to achieve high signaling speeds, then subsequently raises the impedance to limit the overshoot and undershoot noise inherent in high-speed, high-current devices. This allows a single device to have characteristics similar to both series-damping-resistor outputs during static conditions and to high-current outputs during dynamic conditions, eliminating the need for series damping resistors. Due to the characteristics of the DOC output, the dc drive-current specifications for DOC devices are not useable as a relative indicator of the dynamic performance. A thorough understanding of static and dynamic drive-current conditions is required to design with the DOC feature of AVC logic.

Introduction

Performance

Trends in advanced digital electronics design continue to include lower power consumption, lower supply voltages, faster operating speeds, smaller timing budgets, and heavier loads. Many designs are making the transition from 3.3 V to 2.5 V, and bus speeds are increasing beyond 100 MHz. Trying to meet all of these goals makes the requirement of signal integrity harder to achieve. For designs that require very-low-voltage logic and bus-interface functions, TI announces the AVC family featuring TI's DOC circuit. The DOC circuit limits overshoot and undershoot noise inherent in high-speed, high-current devices, while still providing propagation delays of less than 2 ns, maximum, at 2.5 V.

Impedance Matching

The design engineer must carefully consider a logic component's output characteristics to ensure signal integrity and meet timing requirements. The output must have an impedance that minimizes overshoots and undershoots for signal integrity. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. In the past, the selection of a component with integrated 26-Ω series damping resistors on the output ports or the use of external resistors was sometimes necessary. These resistors improve the impedance match of the driver output with the impedance of the transmission-line load and limit overshoot and undershoot noise. Damping resistors reduce the noise, but decrease slew rate and increase propagation delay due to the decreased drive current.

TI's DOC circuitry provides enough drive current to achieve fast slew rates and meet timing requirements, but quickly changes the output impedance level during the output transition to reduce the overshoot and undershoot noise that often is found in high-speed logic. This feature of AVC logic eliminates the need for series damping resistors in the output circuit, thereby improving the output slew rate and propagation-delay characteristics.

The dynamic drive current varies through the transition due to the dynamically changing output impedance. The static on-resistance (R_{ON}) of the output can be calculated from the V_{OH} vs I_{OH} and V_{OL} vs I_{OL} curves (see Figure 1 and Figure 2). At any specific point on the V_{OH} vs I_{OH} curves, $R_{ON} = (V_{OH} - V_{CC})/I_{OH}$. At any specific point on the V_{OL} vs I_{OL} curves, $R_{ON} = V_{OL}/I_{OL}$. The impedance during dynamic conditions is characterized by the slope of the V_O vs I_O line at any specific point on the graph.

The V_{OL} vs I_{OL} curves (see Figure 1) illustrate the impedance characteristics of the output in the low state. The curves represent the amount of sink current available (at a given V_{CC}) to drive the load, as the output voltage decreases from V_{CC} to 0 V when the output is sinking current (i.e., driving low). The V_{OL} vs I_{OL} curve for 2.5-V V_{CC} has two distinct regions of sink current availability. At the beginning of the transition from high to low, the portion of the output from 2.5-V to 1.5-V has a high amount of sink current available. In that region, the curve has characteristics that are similar to a circuit with an output resistance of approximately $20\ \Omega$. Then, during the transition through 1.5 V, there is a steep drop in the drive current available. In the region from 1.5 V to ground, the curve has characteristics that are similar to a circuit with an output resistance of approximately $50\ \Omega$. The V_{OL} vs I_{OL} curves for 1.8-V and 3.3-V V_{CC} have similar characteristics.

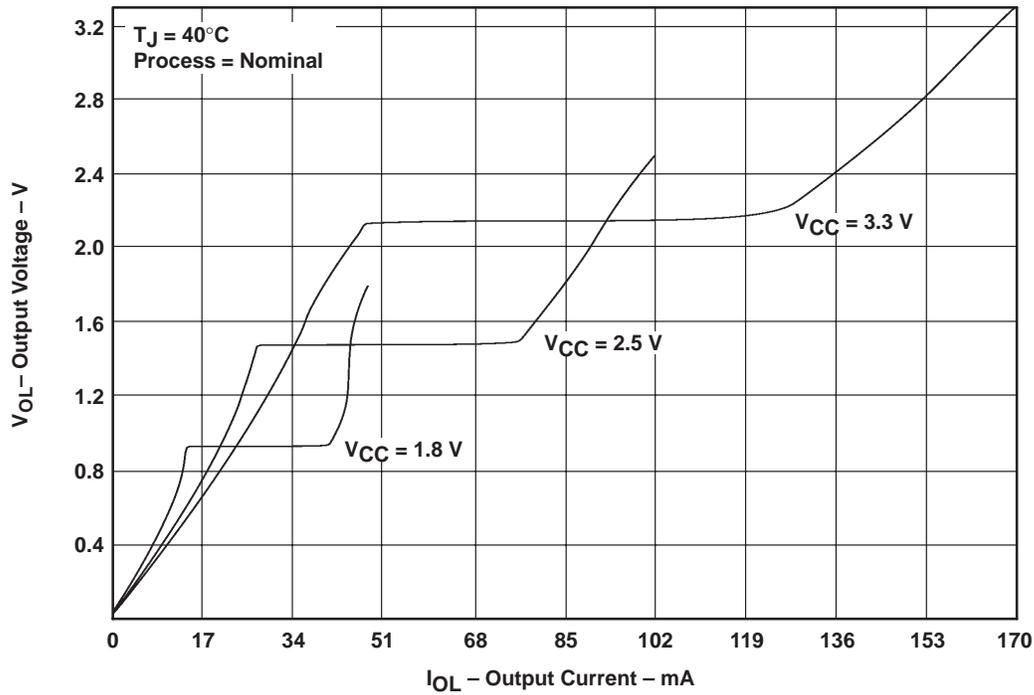


Figure 1. V_{OL} vs I_{OL}

The V_{OH} vs I_{OH} curves (see Figure 2) illustrate the impedance characteristics of the output in the high state. The curves represent the amount of source current available (at a given V_{CC}) to drive the load, as the output voltage increases from 0 V to V_{CC} when the output is sourcing current (i.e., driving high). The operation of the output in the high state is similar to the operation in the low state. There are two distinct regions of source current availability, each with an output resistance (at 2.5-V V_{CC}) of approximately $30\ \Omega$ and $50\ \Omega$, respectively. The V_{OH} vs I_{OH} curves for 1.8-V and 3.3-V V_{CC} have similar characteristics.

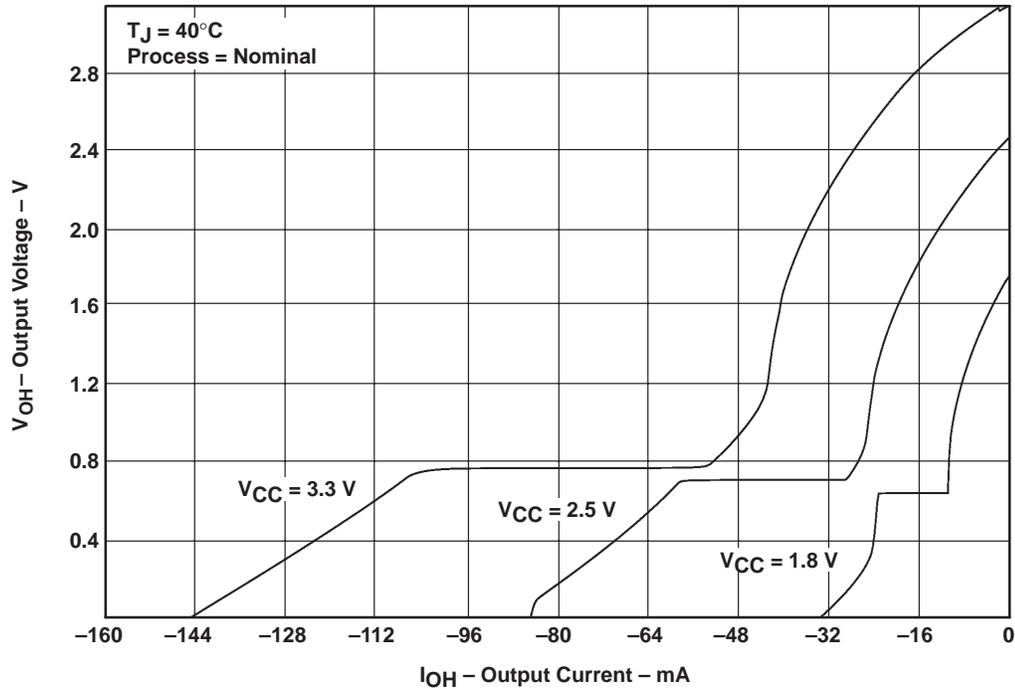


Figure 2. V_{OH} vs I_{OH}

The dual-impedance regions of the DOC output allow a single device to have characteristics similar to a ± 24 -mA high-drive device, providing fast edge rates and propagation-delay times. During the latter portion of the transition and during static conditions, the device has the characteristics of a series-damping-resistor part, with reduced ringing. Figure 3 illustrates the dual-impedance nature of the DOC output as compared to the fixed-impedance outputs of both a high-drive part and a series-damping-resistor part by showing the V_{OL} vs I_{OL} curves of all three.

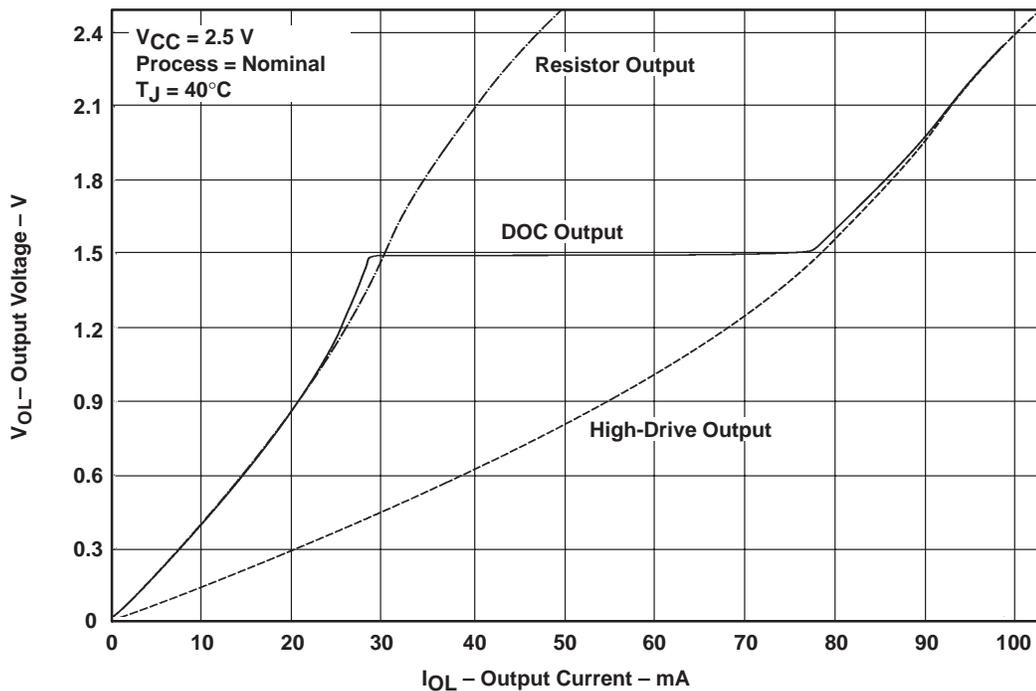


Figure 3. DOC Output Curve Superimposed on Resistor-Output and High-Drive-Output Curves

Output Circuitry

What Happens at the Output in the Transition

A standard device with a fixed low-impedance output delivers high current to the load during the entire transition. At the top of the transition from low to high, high-drive circuits can experience a tremendous overshoot and ringing due to the fast slew rate (see Figure 4). The DOC circuit counteracts this by switching to a higher output impedance, thereby slowing the slew rate as the output approaches the top of the transition.

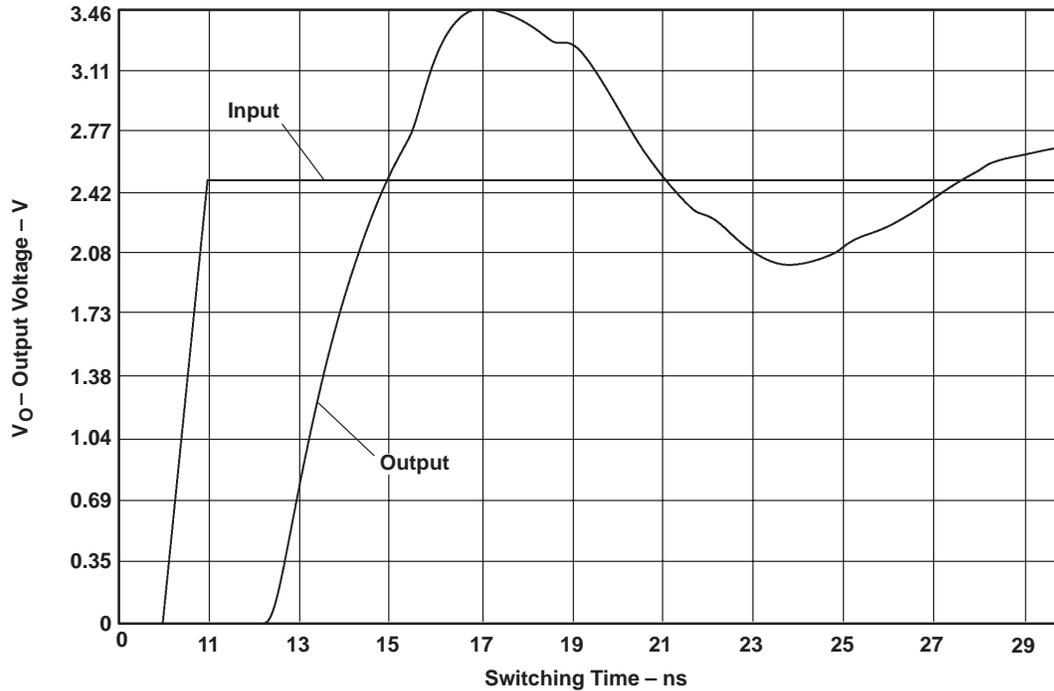


Figure 4. Switching Transition of a Fixed Low-Impedance Driver

Figure 5 illustrates the output of the DOC driver in the transition from low to high. Initially, the output is at a static low level. The 2.5-V V_{OL} vs I_{OL} impedance-characteristic curve (see Figure 1) shows that, with an output at 0 V, the output resistance in the low state is approximately $50\ \Omega$. When the transition from low to high begins, the 2.5-V V_{OH} vs I_{OH} curve (see Figure 2) illustrates the impedance characteristics of the output. Initially, the output resistance is approximately $30\ \Omega$. Under typical conditions, this low-impedance output can deliver nearly 84 mA to the load, providing a very fast slew rate. After the output voltage passes through the threshold (1.5 V) in the transition from low to high, the output resistance is switched from approximately $30\ \Omega$ to approximately $50\ \Omega$. This increase in output resistance reduces the amount of drive current available. This decreases the slew rate and rolls off the transition, producing a smooth knee at the top and reducing overshoot or ringing. When the final output voltage is reached, due to the high output resistance, the amount of drive current available to hold the output voltage at a valid logic level is at a minimum, providing relatively low static-state power levels.

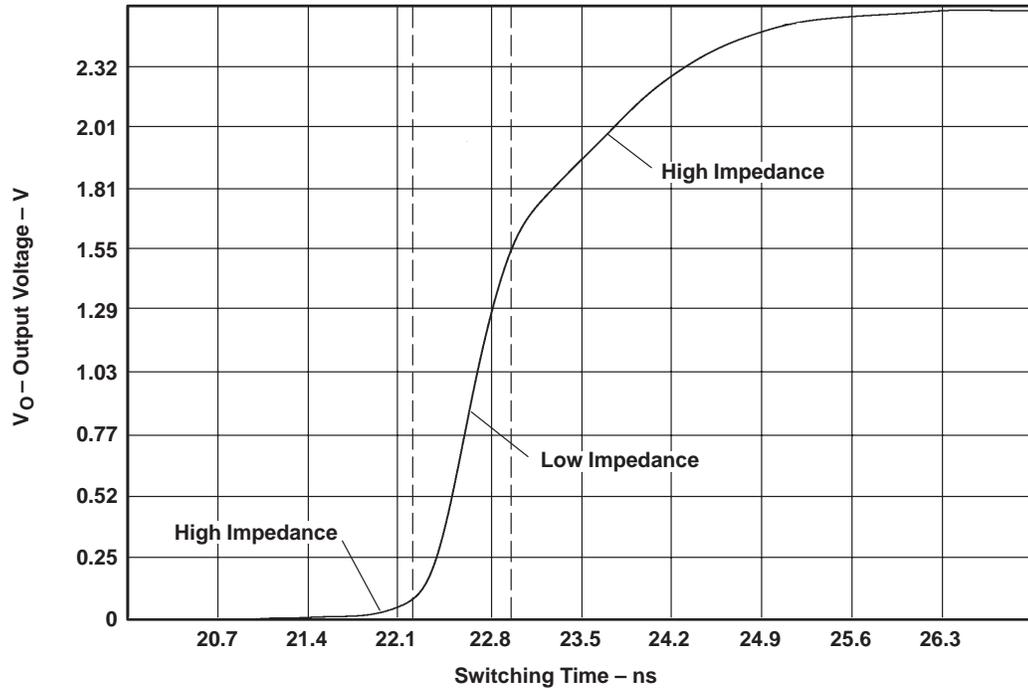


Figure 5. Impedance Through Switching Transitions

A transition from high to low behaves in a similar manner and can be understood by the same principles. When the transition from high to low begins, the 2.5-V V_{OL} vs I_{OL} curve (see Figure 1) illustrates the impedance characteristics of the output. Initially, the output resistance is approximately $20\ \Omega$. Under typical conditions, this low output impedance can deliver nearly 105-mA to the load. Then, as the output voltage passes through the threshold (1.5 V), the output resistance is switched from approximately $20\ \Omega$ to approximately $50\ \Omega$. This results in minimal, or no undershoot.

DOC Circuit Description

Figure 6 shows a simplified output stage of a typical logic circuit. When the input is low, the n-channel transistor (Q_n) turns off and the p-channel transistor (Q_p) turns on and begins to conduct, and the output voltage V_O is pulled high. Conversely, when the input is high, Q_p turns off, Q_n begins to conduct, and V_O is pulled low. This action is similar to an inverter, and several of these inverting stages typically are cascaded in series to form a buffer/driver.

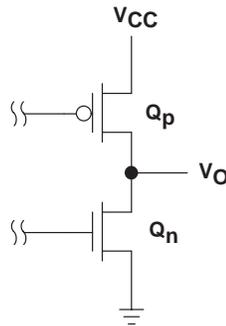


Figure 6. Simplified Totem-Pole Output Stage

The sizes of the output transistors Q_p and Q_n determine the output impedance. The transistors are designed with the sizes of the n-channel FET and p-channel FET selected to provide an output impedance of a specific design value. The sizes can be selected so that the on-resistance of the output is, for example, characteristically approximately $25\ \Omega$, which is the typical output impedance of a conventional low-voltage CMOS logic device. Figure 7 illustrates a driver with the output transistors sized to provide a $25\text{-}\Omega$ output. The driver is shown driving a transmission-line load consisting of a length of transmission line that is terminated into a capacitor. The waveform showing the signal incident at the capacitor depicts the fast slew rates and small propagation delays that are characteristic of low-impedance drivers. The fast edge rates create large overshoots and unacceptable ringing.

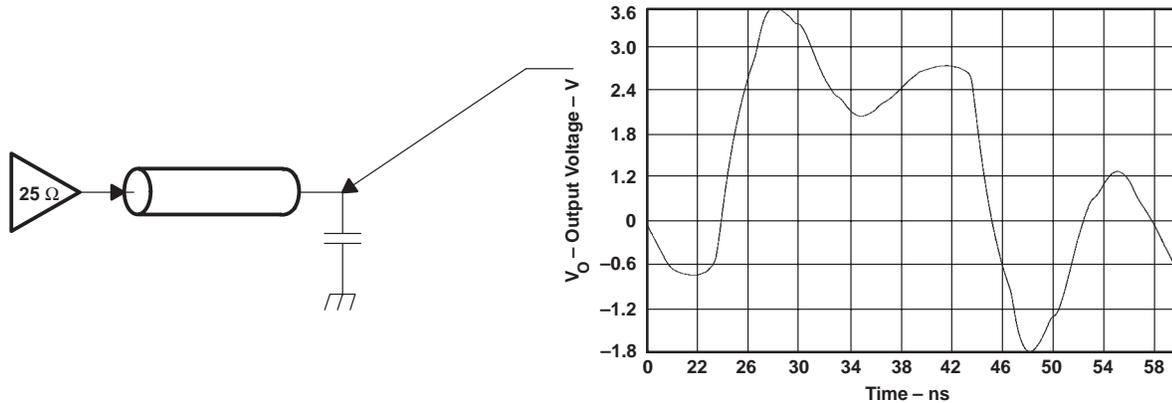


Figure 7. $25\text{-}\Omega$ Driver Driving Transmission-Line Load and Waveform at the Load

One method of reducing the ringing and electrical noise is to slow down the edge rates. This can be accomplished by the addition of a damping resistor in series with the output. This creates a high-impedance low-drive output. Figure 8 illustrates a driver with a $25\text{-}\Omega$ output and a series $26\text{-}\Omega$ damping resistor driving the transmission-line load. The resultant signal is much cleaner, but the slower edge rate increases the propagation delay time. Depending on the total timing budget available, this could be an unacceptable solution. Series resistors also can raise the dc low-voltage level of a signal. This reduces noise immunity of the receiving logic. Finally, series damping resistors should be used only on point-to-point nets, and never with distributed loads, because of the half voltage that propagates down the transmission line due to incident wave switching.

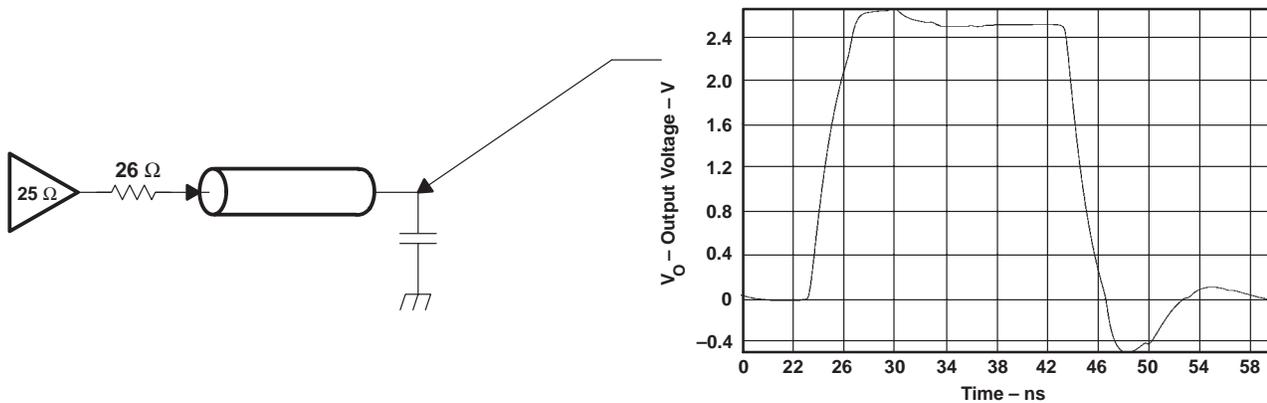


Figure 8. $25\text{-}\Omega$ Driver and $26\text{-}\Omega$ Series Resistor Driving Transmission-Line Load and Waveform at the Load

Another method that can be used to improve the impedance match of the output with the load is to reduce the size of the output transistors. If their sizes are decreased, the output impedance increases. This provides a low-drive output. Figure 9 illustrates a driver with the output transistor sizes selected to provide a $50\text{-}\Omega$ output. The driver is shown driving the same transmission-line load and the resultant waveform at the load exhibits similar characteristics to the series-damping-resistor version.

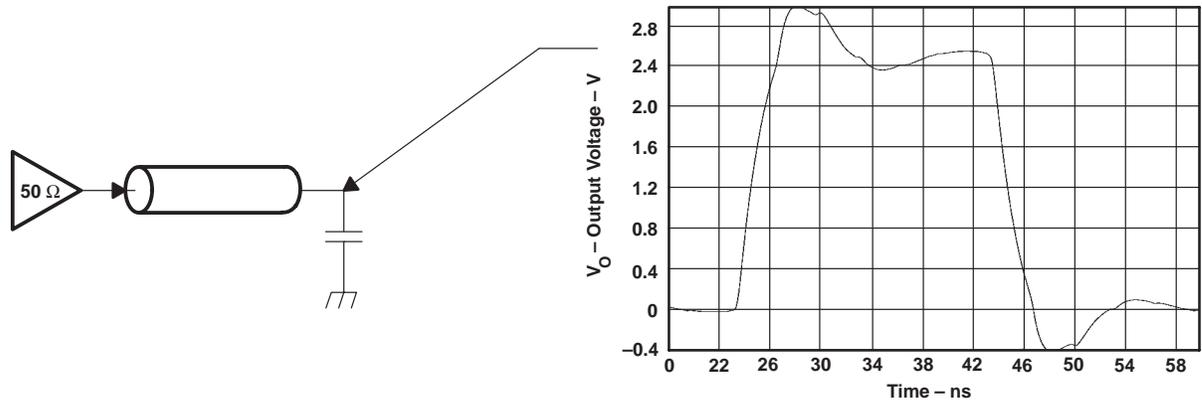


Figure 9. 50-Ω Driver Driving Transmission-Line Load and Waveform at the Load

It is also interesting to explore the attributes of two drivers in parallel. Figure 10 represents two 50-Ω drivers in parallel. The resultant waveform at the load exhibits characteristics similar to the single 25-Ω driver. In fact, the parallel combination of the two has the same output impedance as a single 25-Ω impedance driver. This effectively creates a low-impedance high-drive output.

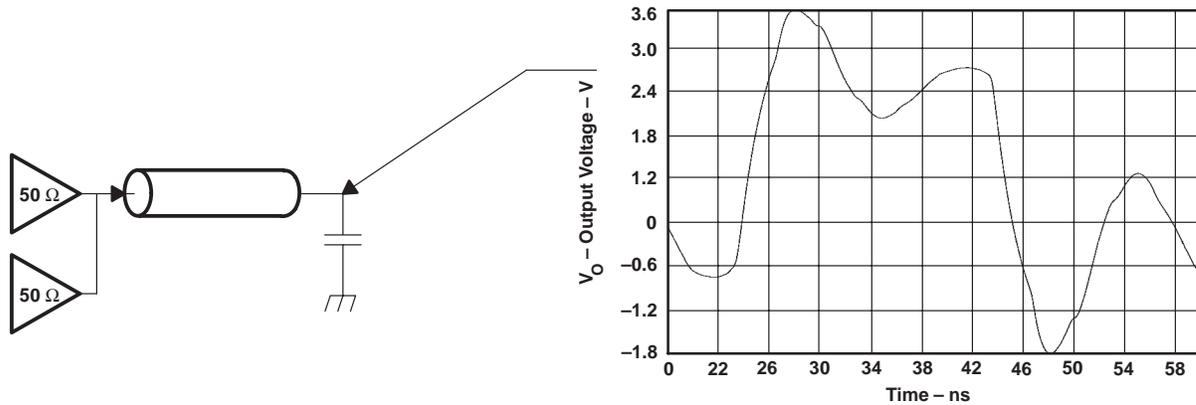


Figure 10. Two 50-Ω Drivers In Parallel, Driving Transmission-Line Load and Waveform at the Load

Increasing the output impedance reduces overshoots and undershoots, but at the cost of increased propagation delays. Decreasing the output impedance decreases propagation delays, but at the cost of increased overshoots and undershoots. A desirable circuit would have a low output impedance for the beginning portion of the output transition and a high output impedance for the latter portion of the output transition. This would provide fast propagation delays, with minimal, or no overshoot or undershoot.

Figure 11 is a block diagram of the DOC circuit, which consists of a fixed driver with a nominal 50-Ω on-resistance. The 50-Ω driver functions like a typical high-impedance low-drive output, with good electrical and noise characteristics. In parallel with the 50-Ω driver is a controllable 50-Ω nominal on-resistance driver, with an output that can be enabled or disabled similar to the output of a 3-state device. When a device is disabled, its output is in a very high-impedance state and contributes nothing to the drive or to the loading of the output. When it is enabled, the parallel combination of the 50-Ω drivers has the same output characteristics as a single 25-Ω impedance driver. This effectively creates a low-impedance high-drive output. The impedance control circuit (ZCC) enables and disables the controllable driver by controlling its ON signal. The ZCC monitors the output and controls the controllable driver at the appropriate times during the signal transition to achieve a high-drive, fast slew-rate transition.

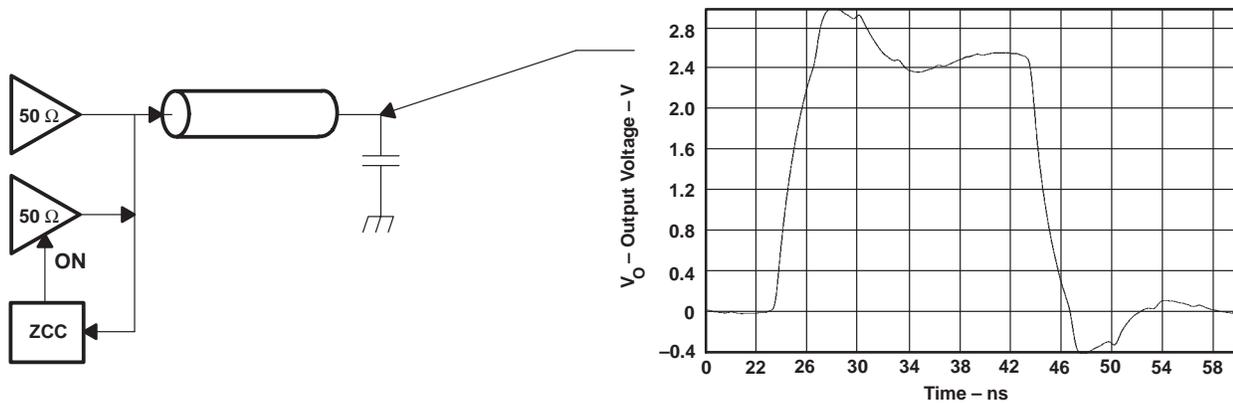


Figure 11. DOC Circuit Driving Transmission-Line Load and Waveform at the Load

The operation of the DOC begins with the output in a static state, for example, at a logic low state. In the static low state, the ZCC has the controllable 50- Ω driver disabled and the n channel of the fixed 50- Ω driver sinks current to ground from the output. When the input transitions from low to high, the n-channel transistor in the fixed 50- Ω driver turns off, and the p channel turns on, sourcing current to the output and beginning the output transition from low to high. Simultaneously, the ZCC enables the p channel in the controllable 50- Ω driver. The parallel p channels of the drivers have a combined on-resistance of approximately 25 Ω . This low impedance provides a high drive current to cause a fast slew-rate signal transition. The ZCC senses the output voltage, and as the voltage passes through threshold in the transition from low to high, the ZCC disables the output p channel of the controllable 50- Ω driver. The increase in output impedance decreases the slope and rolls off the output signal, reducing the overshoot.

The operation of the high-to-low transition is similar.

AC Dynamic Drive vs DC Static Drive

The dc drive-current ratings in the recommended operating-conditions table of a device data sheet typically are selected to show the static-drive capability of a device when the output voltage is at a worst-case valid logic level, such as $V_{OH(MIN)}$ or $V_{OL(MAX)}$. Historically, these dc drive-current ratings were used as a relative measure of a component's ac dynamic-drive performance. For a device with a fixed output on-resistance, this was an acceptable method, because the dc current at a given logic level could be extrapolated to determine the amount of ac drive current available through the transition.

With DOC circuitry, the output impedance characteristics change dynamically during a transition. *The dc drive-current specification is not a useable indicator of the devices' dynamic performance capability.* The dc output ratings of DOC devices (see Table 1) can be used loosely as a relative comparison to the dc output ratings of devices with integral series damping resistors (see Table 2), and this is a good indication of the DOC circuit's excellent low-noise and low-power characteristics. However, unlike a part with a fixed low-drive output, the DOC circuitry provides good ac performance. The DOC output provides a very strong ac drive during dynamic conditions, capable of driving very heavily capacitive CMOS loads.

Table 1. Recommended Static Output Current for DOC Circuits¹

		MIN	MAX	UNIT
I _{OHS}	Static high-level output current	V _{CC} = 1.65 V to 1.95 V		mA
		V _{CC} = 2.3 V to 2.7 V		
		V _{CC} = 3 V to 3.6 V		
I _{OLS}	Static low-level output current	V _{CC} = 1.65 V to 1.95 V		mA
		V _{CC} = 2.3 V to 2.7 V		
		V _{CC} = 3 V to 3.6 V		

Table 2. Recommended Output Current for ALVC Device With Damping Resistor²

		MIN	MAX	UNIT
I _{OH}	High-level output current	V _{CC} = 2.3 V		mA
		V _{CC} = 2.7 V		
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.3 V		mA
		V _{CC} = 2.7 V		
		V _{CC} = 3 V		

The DOC device performs like a high-drive part during signal transition. *Under typical conditions at 2.5-V V_{CC}, the drive current that is available during the beginning of a transition from low to high is about 84 mA, and from high to low is about 105 mA.* Figure 12 illustrates the output current of the DOC circuit driving a standard load through the low-to-high and high-to-low transitions. Note the large peak currents during the transition.

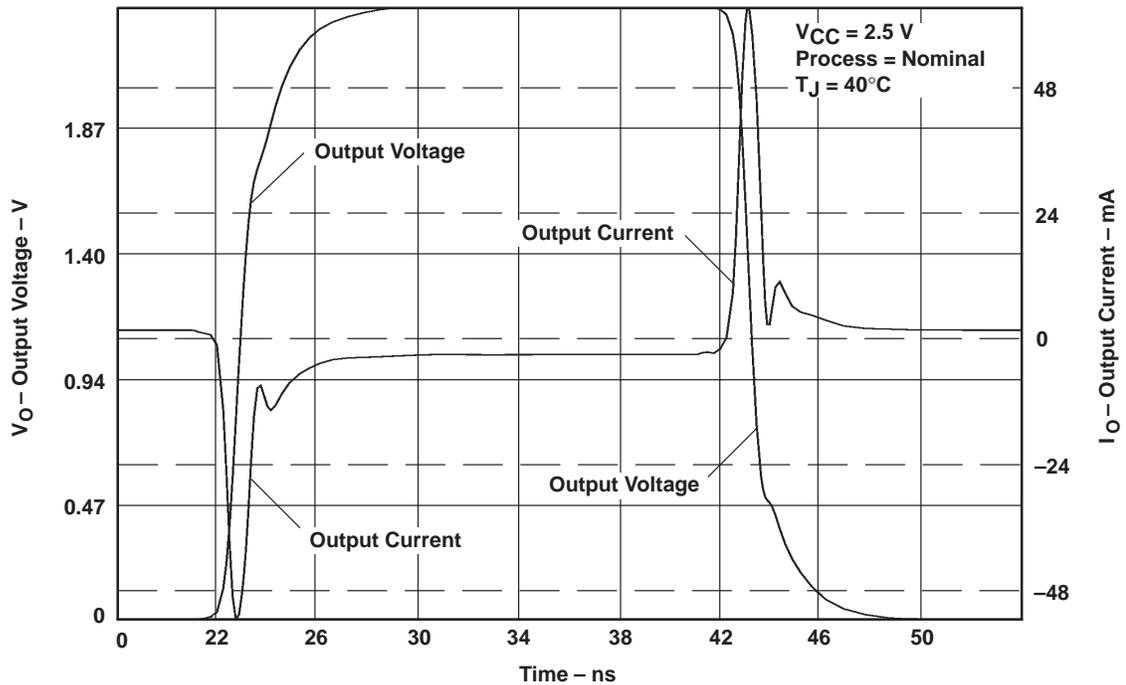


Figure 12. DOC Device Output Current Through the Transition

The dynamic drive current is not specified on the data sheet for devices with DOC outputs because of its transient nature, but it is similar to the dynamic drive current that is available from a ± 24 -mA (at 2.5-V V_{CC}) high-drive standard-output device (see Figure 13).

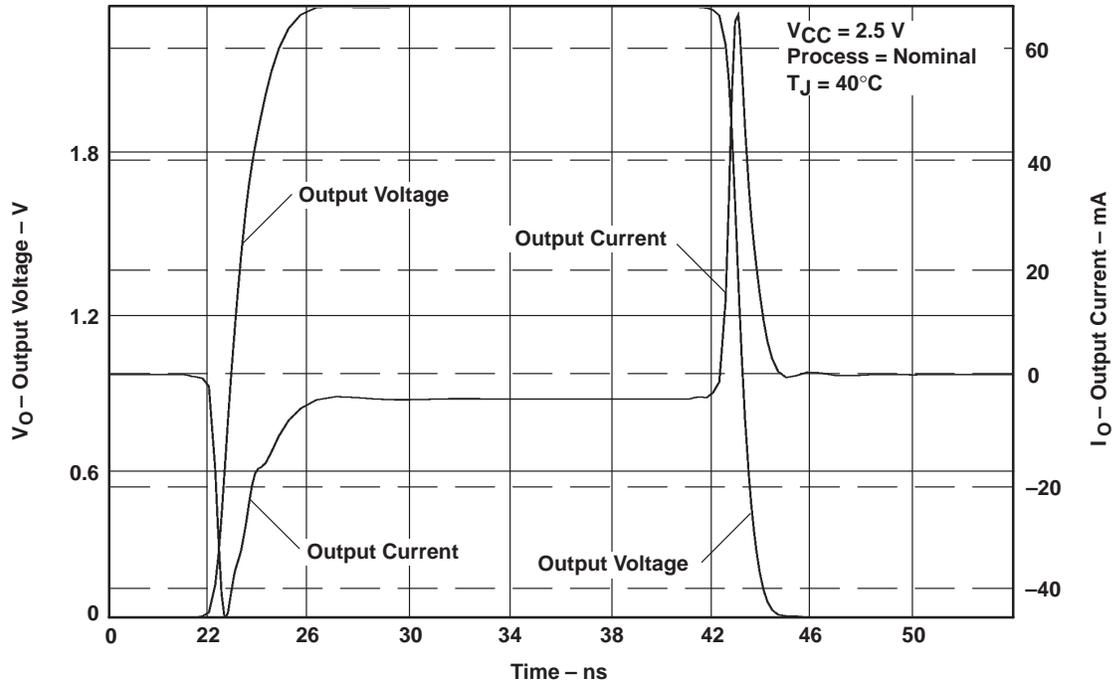


Figure 13. Output Current Through the Transition, ±24-mA High-Drive Standard-Output Device

Because a typical CMOS load is purely capacitive, with very little bias (leakage) current necessary to hold a valid static logic level, the amount of dc drive required of most drivers is small. The dc drive is specified on the data sheet of DOC output devices. The output parameters are static and testable values that are enumerated in terms of minimum and maximum output voltages at specific output currents (see Table 3).

Table 3. Output Voltage Characteristics Over Recommended Operating Free-Air Temperature Range¹

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -4 mA, V _{IH} = 1.07 V	1.65 V	1.2			
	I _{OH} = -8 mA, V _{IH} = 1.7 V	2.3 V	1.75			
	I _{OH} = -12 mA, V _{IH} = 2 V	3 V	2.3			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA, V _{IL} = 0.57 V	1.65 V	0.45			
	I _{OL} = 8 mA, V _{IL} = 0.7 V	2.3 V	0.55			
	I _{OL} = 12 mA, V _{IL} = 0.8 V	3 V	0.7			

Termination (AC vs DC)

Because of the excellent signal-integrity characteristics of the DOC output, transmission-line termination typically is unnecessary. Due to the high-impedance characteristics of the output in the static state, *the use of dc termination is specifically discouraged*. The output current that is required to bias a dc termination network could exceed the static-state output-drive capabilities of the device. AVC family devices with DOC circuitry are suited ideally for any high-speed, point-to-point application or unterminated distributed load, such as high-speed memory interfaces.

Waveforms – Comparison of ALVCH Standard and Resistor Outputs

Figures 14 and 15 show the SPICE results comparing SN74AVC16827 with SN74ALVCH16827 and SN74ALVCH162827 into a standard lumped load (see Appendix A) for $V_{CC} = 2.5\text{ V}$ and $V_{CC} = 3.3\text{ V}$, respectively. The results show the relative propagation delay and noise performance of the DOC circuit.

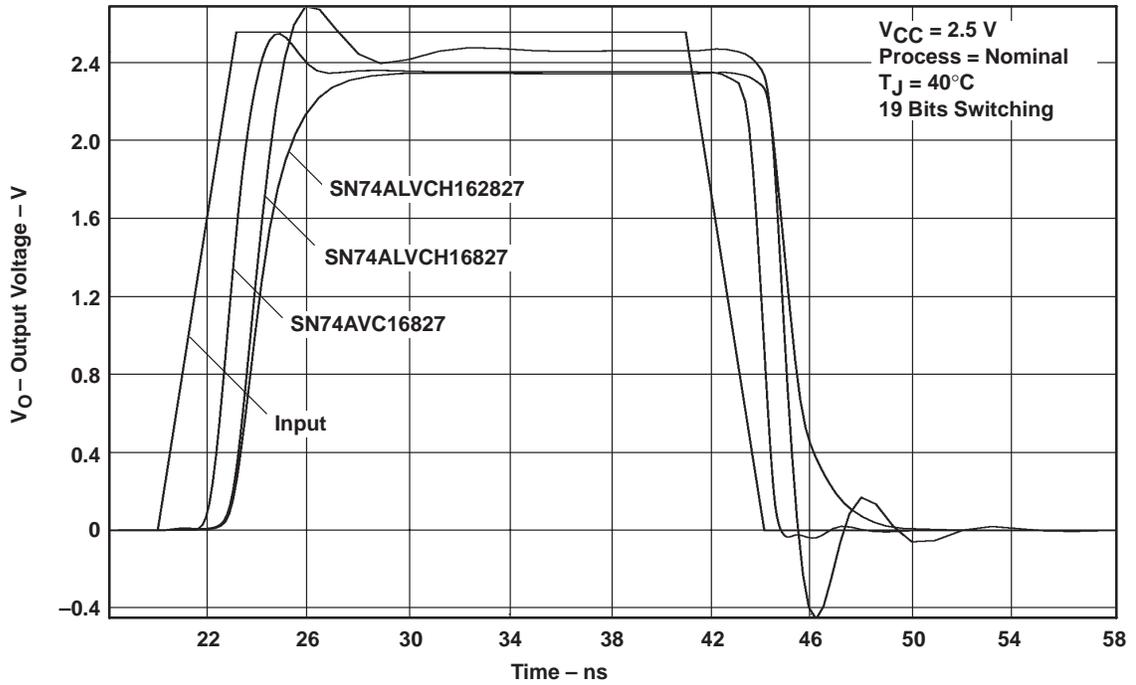


Figure 14. Outputs Driving a Standard Lumped Load, $V_{CC} = 2.5\text{ V}$

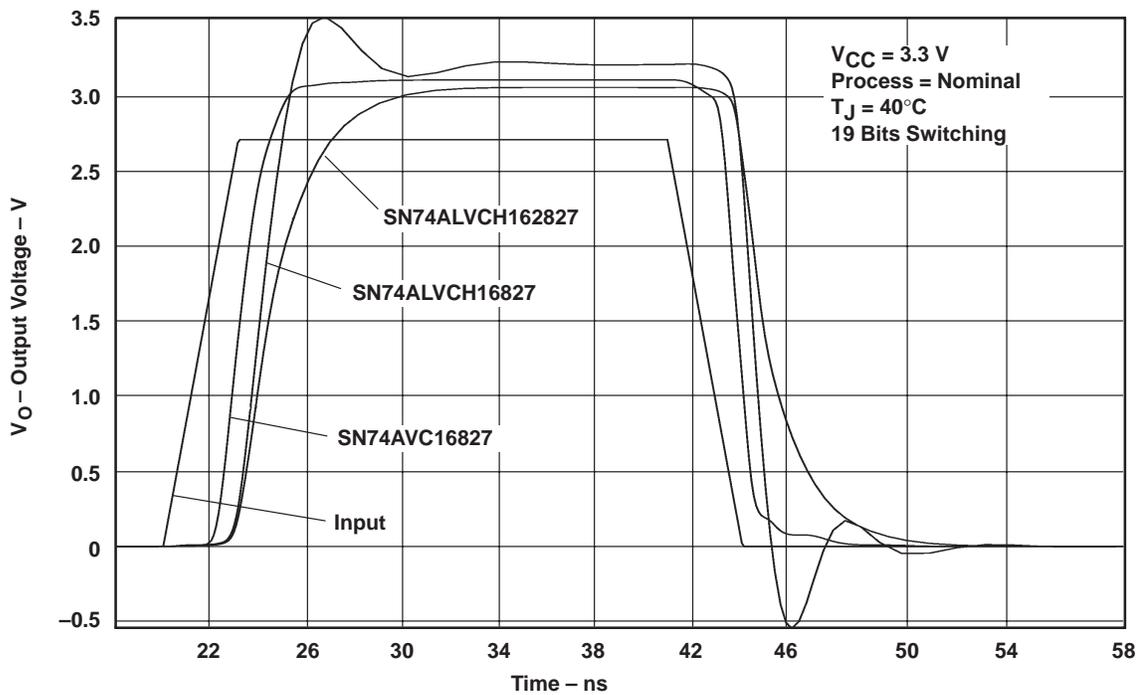


Figure 15. Outputs Driving a Standard Lumped Load, $V_{CC} = 3.3\text{ V}$

Figures 16 and 17 show the SPICE modeling of the SN74AVC16827 with the DOC circuit, an SN74ALVCH16827 with low-impedance output circuit, and an SN74ALVCH162827 with series damping resistors driving a PC100 DQM load for $V_{CC} = 2.5\text{ V}$ and $V_{CC} = 3.3\text{ V}$, respectively. The DQM load is defined in the Intel™ *PC SDRAM Registered DIMM Specification*, Revision 1.0, February 1998³. For this example, the 256-Mbyte load was used. The transmission lines have a characteristic impedance of $70\ \Omega$. The lengths of the transmission lines are specified in the PC100 specification; series resistor R1 was specified as zero. This resistor is not necessary when using the DOC circuit. The six SDRAM loads were modeled by the circuit shown in Figure 18.

The waveforms shown in Figures 16 and 17 were measured at the input to the memory devices. The low-impedance driver exhibits excessive overshoots and undershoots, while the DOC circuit and the driver with series damping resistors does not. The DOC circuit is faster than the series-damping-resistor circuit. This improvement in speed is more pronounced when the simulations are run under worst-case weak conditions.

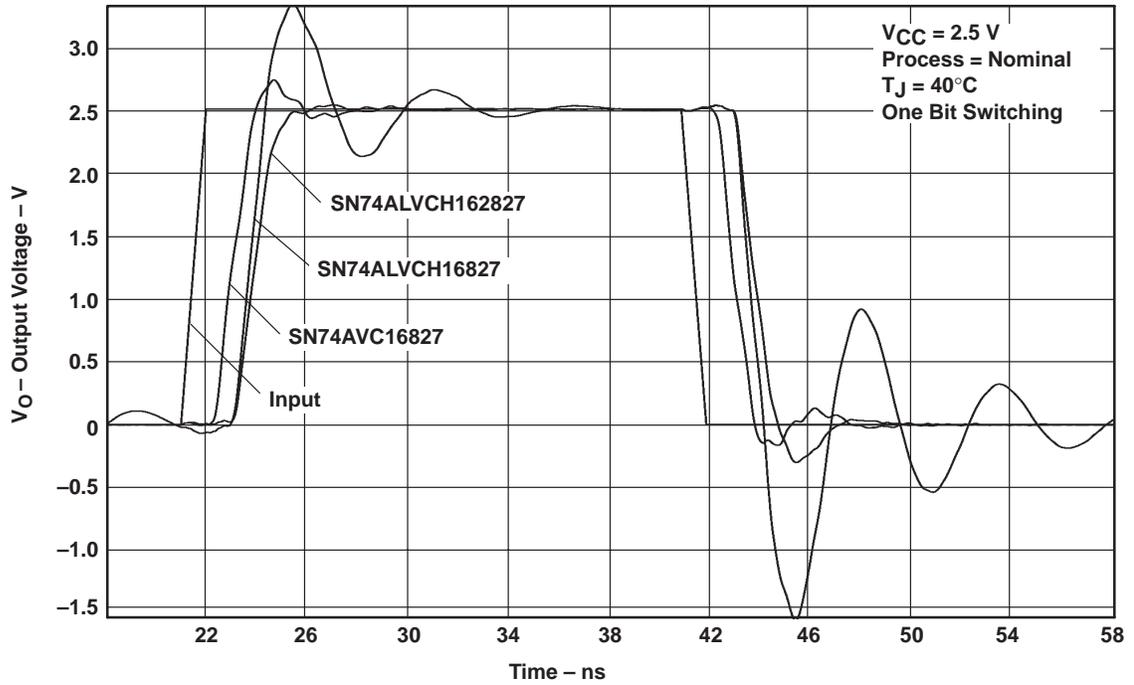


Figure 16. Outputs Driving a PC100 Load Network, $V_{CC} = 2.5\text{ V}$

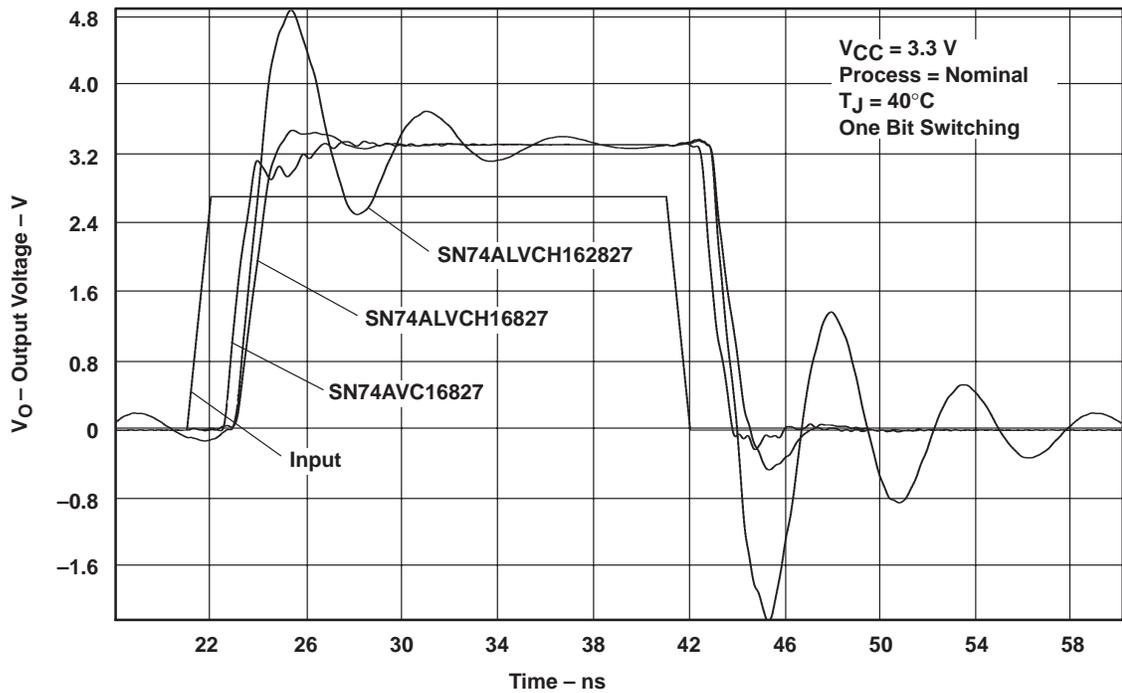


Figure 17. Outputs Driving a PC100 Load Network, $V_{CC} = 3.3\text{ V}$

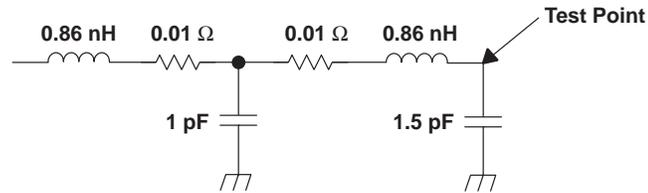


Figure 18. SDRAM Load Model

Features and Benefits

Table 4 summarizes DOC circuit features and some of the benefits of those features.

Table 4. Features and Benefits of DOC Circuitry

FEATURES	BENEFITS
Optimized for 2.5-V V_{CC} . No damping resistors	Enables low-power designs
Low-impedance, high-drive output during the beginning of a signal transition	Fast edge-rates and small propagation delays
High output impedance for the later portion of the output transition	Minimal, or no overshoot or undershoot
High-impedance, low-drive steady-state output after signal transition	Enables low-power designs
DOC outputs do not require series damping resistors internally or externally	Reduced ringing without series output resistors; increased performance; cost savings
I _{OFF} – reverse-current paths to V_{CC} blocked	Outputs disabled during power off for use in partial power-down designs

Conclusion

The DOC circuitry provides a low-impedance, high-drive output during the beginning of a signal transition, to provide fast edge rates and small propagation delays. Then, as the output passes through the threshold, the DOC switches to a high-impedance, low-drive output to roll off the signal and reduce ringing. The amount of static dc drive current specified in the data sheets of devices with DOC features does not reflect the large amount of dynamic current that is available to drive a typical large capacitive CMOS load.

Frequently Asked Questions

1. Q: What is DOC?

A: DOC is the Dynamic Output Control circuit (patent pending). It is the output circuit of TI's AVC family of devices that changes the output impedance during the signal transition.

2. Q: Why use DOC output?

A: During the beginning of the signal transition, DOC output provides the desirable characteristics of high drive to supply fast edge-rates and small propagation delays. As the signal passes through the threshold, the DOC output decreases the drive to roll off the signal and reduce ringing without the use of damping resistors.

3. Q: How does DOC work?

A: The DOC output has an impedance-control circuit that monitors the output signal. When a transition begins, the impedance-control circuit enables the outputs of two parallel drivers to provide a low-impedance, high-drive output. As the output passes through the threshold, the impedance-control circuit disables the output of one of the drivers, providing a high-impedance, low-drive output.

4. Q: Should I use series damping resistors on the output of DOC devices?

A: It is not necessary to use series damping resistors to reduce ringing because the DOC output provides a high-impedance, low-drive output at the end of the signal transition. Using series damping resistors would defeat the high-drive benefit of the DOC output.

5. Q: Can I use dc termination on the output of DOC devices?

A: *Do not use dc termination.* The use of dc termination could exceed the static-drive capability of the DOC output. Due to the excellent signal-integrity characteristics of the DOC output, termination should be unnecessary.

6. Q: What is the maximum drive-current capability of the DOC output?

A: The DOC output has ± 8 -mA dc static-drive current capability at 2.5-V V_{CC} . Under typical conditions at 2.5-V V_{CC} , the amount of ac dynamic-drive current that the DOC output can supply varies from a maximum of about 84 mA at the beginning of the transition from low to high. At the beginning of the transition from high to low, it varies from a maximum of about 105 mA.

7. Q: What is the output impedance of a DOC circuit?

A: The impedance during dynamic conditions is characterized by the slope of the V_O vs I_O line, at any specific point on the graph. The output R_{ON} can be calculated from the V_{OH} vs I_{OH} and V_{OL} vs I_{OL} curves (see Figure 1 and Figure 2). At any specific point on the V_{OH} vs I_{OH} curves, $R_{ON} = (V_{OH} - V_{CC})/I_{OH}$. At any specific point on the V_{OL} vs I_{OL} curves, $R_{ON} = V_{OL}/I_{OL}$. In the high state, the output R_{ON} varies from approximately 50 Ω in the high-impedance mode to approximately 30 Ω in the low-impedance mode. In the low state, the output R_{ON} varies from approximately 50 Ω in the high-impedance mode to approximately 20 Ω in the low-impedance mode.

8. Q: Are devices with DOC output circuitry fast?

A: Yes, the DOC output provides a very fast edge-rate to decrease the propagation delay times, while maintaining the excellent signal-integrity characteristics associated with the slower series-damping-resistor parts.

9. Q: Why aren't ac dynamic-drive specifications included in the data sheet?
- A: The dynamic-drive current is not specified on the data sheet for devices with DOC outputs because of its transient nature, but it is similar to the drive current available from a standard-output device with an I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC} .
10. Q: In data sheets for devices with DOC outputs, is the dc static-drive specification an indicator of the devices' dynamic performance?
- A: No. The devices perform like high-drive devices during signal transition. This is not reflected in the dc static-drive specification on the data sheet.
11. Q: Since the DOC output provides high-drive, does it suffer from poor simultaneous switching performance? How does its simultaneous switching performance compare to standard and resistor devices?
- A: At 2.5-V V_{CC} with output into a standard load, SPICE analysis shows that the SN74AVC16245 DOC outputs have a maximum $V_{OLV} = -165$ mV, standard outputs have a maximum $V_{OLV} = -574$ mV, and resistor outputs have a maximum $V_{OLV} = -36$ mV (15 outputs switching, one steady-state low).
12. Q: Do DOC outputs contribute to a device's low-power performance?
- A: Compared to a damping-resistor output where a portion of the output drive is dissipated in the resistor and not delivered to the load, the DOC output offers better low-power performance. The devices in the AVC family that feature DOC outputs are designed for 2.5-V V_{CC} operation, enabling low-power designs.

Acknowledgment

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References

1. TI *SN74AVC16245 16-Bit Bus Transceiver With 3-State Outputs*, literature number SCES142.
2. TI *SN74ALVC162245 16-Bit Bus Transceiver With 3-State Outputs*, literature number SCES064.
3. *Intel PC SDRAM Registered DIMM Specification*, Revision 1.0, February 1998.

Glossary

A

A	Amperes
ac	Alternating current
ALVC	Advanced Low-Voltage CMOS
AVC	Advanced Very-low-voltage CMOS

B

B	Byte
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C

C	Celsius
CMOS	Complementary metal-oxide semiconductor

D

dc	Direct current
DIMM	Dual-inline memory module
DOC	Dynamic output control (patent pending)
DQM	Data mask
DRAM	Dynamic random-access memory

F

F	Farad
FET	Field-effect transistor

H

H	Henry
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I

IBIS	I/O buffer information specification
I_I	Input current
I_{OFF}	Current into a pin when $V_{CC} = 0$ V
I_{OH}	High-level output current
I_{OHS}	Static high-level output current
I_{OL}	Low-level output current
I_{OLS}	Static low-level output current
IV	Current vs voltage

M

Max	Maximum
Min	Minimum

P

PC	Personal computer
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R

R_{ON}	On-state output resistance
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S

s	Seconds
SDRAM	Synchronous DRAM
SPICE	Simulation program with integrated-circuit emphasis

T

TI	Texas Instruments
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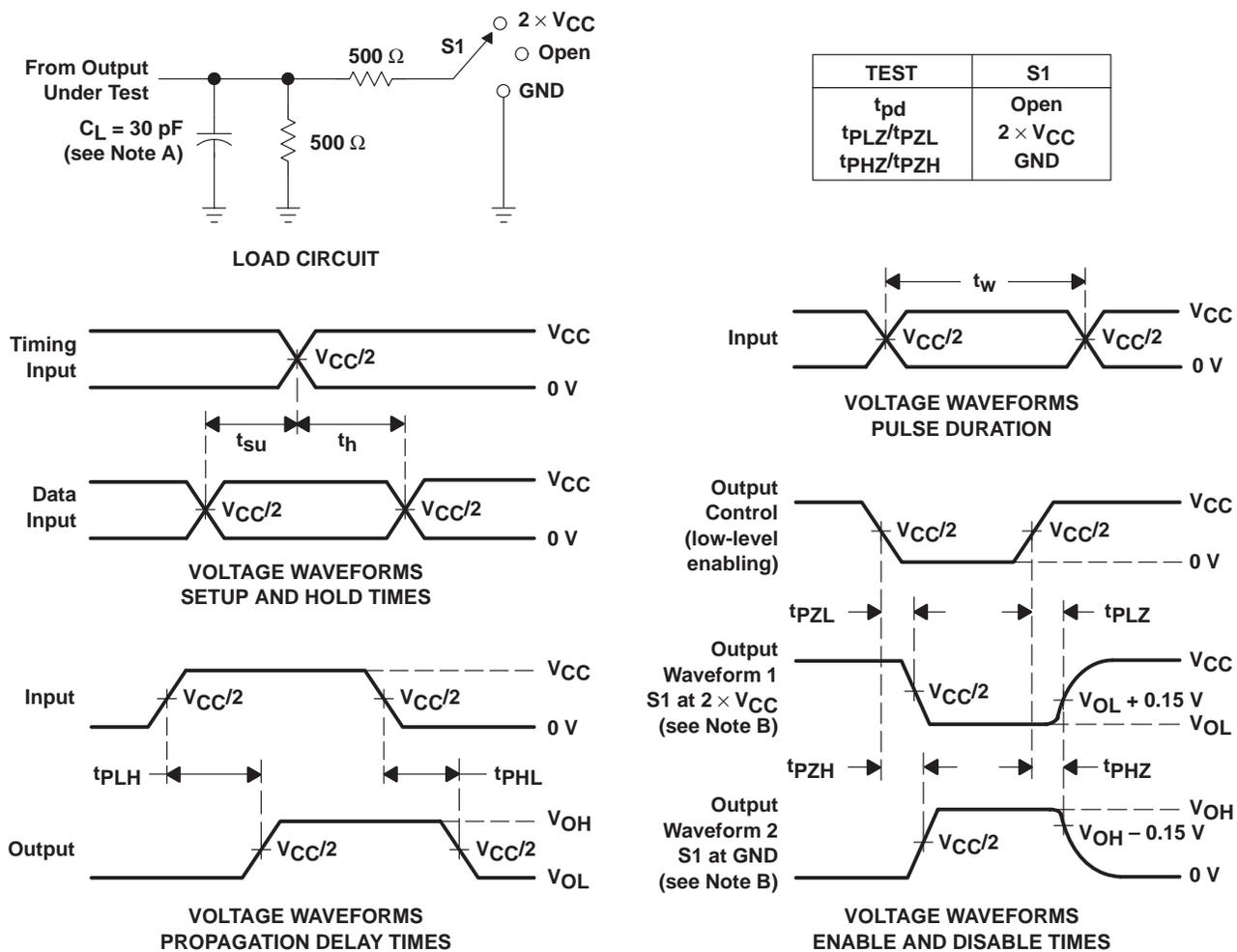
V

V	Volts
V_{CC}	Supply voltage
V_O	Output voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OHP}	High-level output voltage peak
V_{OHV}	High-level output voltage valley
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley

Z

ZCC	Impedance control circuit
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Appendix A – Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure A-1. AVCC Load Circuit and Voltage Waveforms ($V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$)

