TI SN74ALVC16835 Component Specification Analysis for PC100

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Introduction

The PC100 standard establishes design parameters for the PC SDRAM DIMM that is designed to operate at 100 MHz. The 168-pin, 8-byte, registered SDRAM DIMM (see Figure 1) is a JEDEC-defined device (JC-42.5-96-146A). Some of the defined signal paths include data signals, address signals, and control signals (see Table 1). This application report discusses the SN74ALVC16835 18-bit universal bus driver that is available from Texas Instruments (TI™) and analyzes its specifications with respect to the requirements of the registered PC100 DIMM.

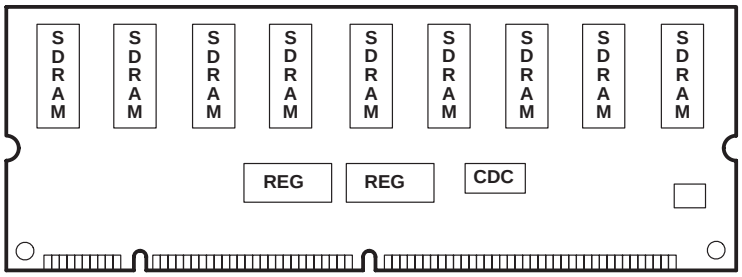

Figure 1. Registered SDRAM DIMM

Table 1. 168-Pin DIMM Pin Assignments

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	V_{SS}	29	DQMB1	57	DQ18	85	V_{SS}	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	V_{CC}	87	DQ33	115	$\overline{RAS}$	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	Vref NC	90	V_{CC}	118	A3	146	Vref NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	V_{CC}	101	DQ45	129	$\overline{S3}$	157	V_{CC}
18	V_{CC}	46	DQMB2	74	DQ28	102	V_{CC}	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	A13	160	DQ62
21	CB0	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	V_{CC}	112	DQMB4	140	DQ49	168	V_{CC}

Device Information

The SN74ALVC16835 is an 18-bit universal bus driver with 3-state outputs designed for 2.3-V to 3.6-V V_{CC} operation (see Table 2 and Figure 2). When the latch-enable (LE) input is high, the device operates in the transparent mode and the Y outputs follow the A inputs. If the clock (CLK) input is held in a high or low state, the device operates like a D-type latch and the Y output data is latched when LE is taken low. If CLK is clocked, when LE is low the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by the active-low output-enable ($\overline{OE}$) input. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled.

Table 2. SN74ALVC16835 Function Table

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y_0†

† Output level before the indicated steady-state input conditions were established if CLK is high before LE goes low

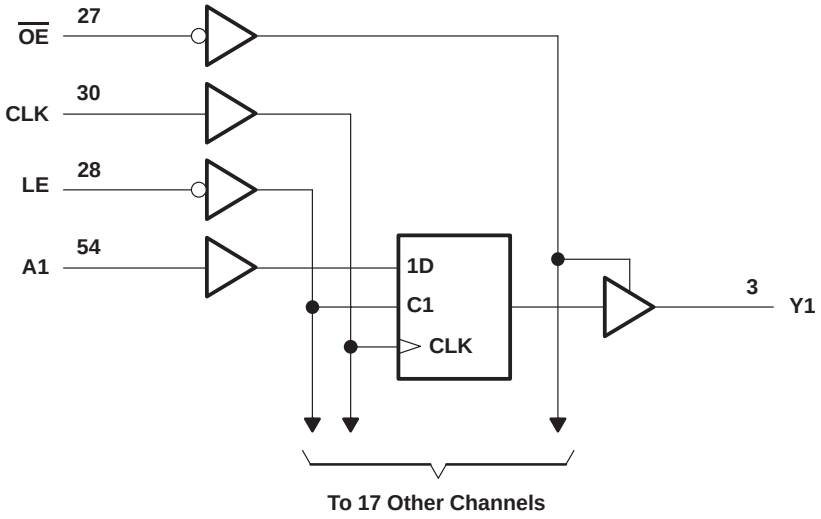

Figure 2. SN74ALVC16835 Logic Diagram

SN74ALVC16835 in the PC100 Application

An analysis of the logic functionality of the device should focus on the polarity of the LE input. The SN74ALVC16835 function uses an active-high LE control input. LE is controlled in the DIMM application by the register enable (REGE) signal from the motherboard. When REGE is low, the DIMM operates in the buffered mode. When REGE is high, the DIMM operates in the registered mode. The REGE signal performs the logical inverse function of the LE signal. To utilize an SN74ALVC16835-type device, an inverter is necessary between the DIMM REGE pin and the SN74ALVC16835 LE pin (see Figure 3). The SN74AHC1G04 Microgate Logic in the plastic small-outline transistor (SOT) package is an ideal single-gate inverter.

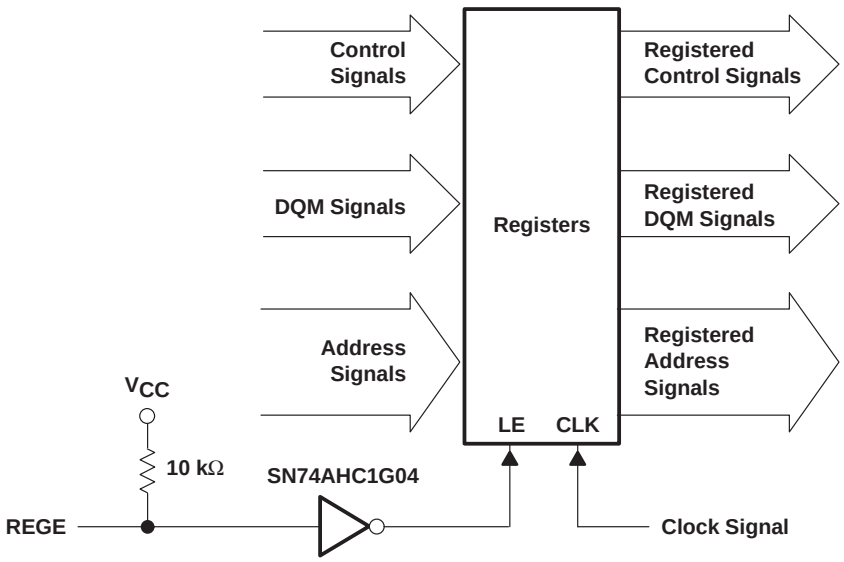

Figure 3. Inverted REGE Wiring for SN74ALVC16835

The bit density of the buffer/register should be considered when selecting a device for a DIMM design. For example, 29 signals must pass through the 128-Mbyte DIMM buffer/register. Using two 18-bit devices, such as the SN74ALVC16835 on the 128-Mbyte DIMM, results in seven unused bits (see Figure 4). Due to contention with the weak pullups in the output circuit of the memory controller, the buffer/register device *cannot* utilize bus hold on the inputs. Because unused CMOS inputs *must* be held at a valid logic high or low voltage, pullup or pulldown resistors are required on any unused buffer/register inputs.

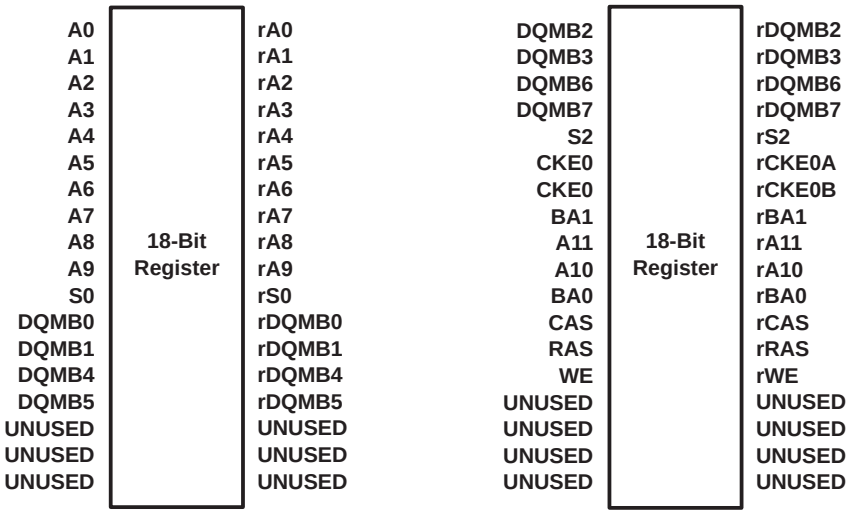

Figure 4. 128-Mbyte DIMM Register Wiring

Examination of the electrical characteristics of the outputs is a critical portion of a successful DIMM design. The following component specification analysis (See Table 3) and IV Characteristics (see Figure 5) are presented for comparison of the SN74ALVC16835 characteristics with the requirements published by Intel™ in the PC SDRAM Registered DIMM Specification Revision 1.0.

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Table 3. SN74ALVC16835 Component Specifications

PARAMETER	CONDITIONS	Intel REQUIREMENTS		TI SN74ALVC16835		UNIT
		V_{CC} = 3.3 V ± 0.15 V T_A = 0°C to 65°C		V_{CC} = 3.3 V ± 0.15 V T_A = 0°C to 65°C		
		MIN	MAX	MIN	MAX	
t_{pd}	From (input) clock To (output) Y	1.7	4.5	1.7	4.5	ns
I_I	$V_I = V_{CC}$ or GND		±10		±5	µA

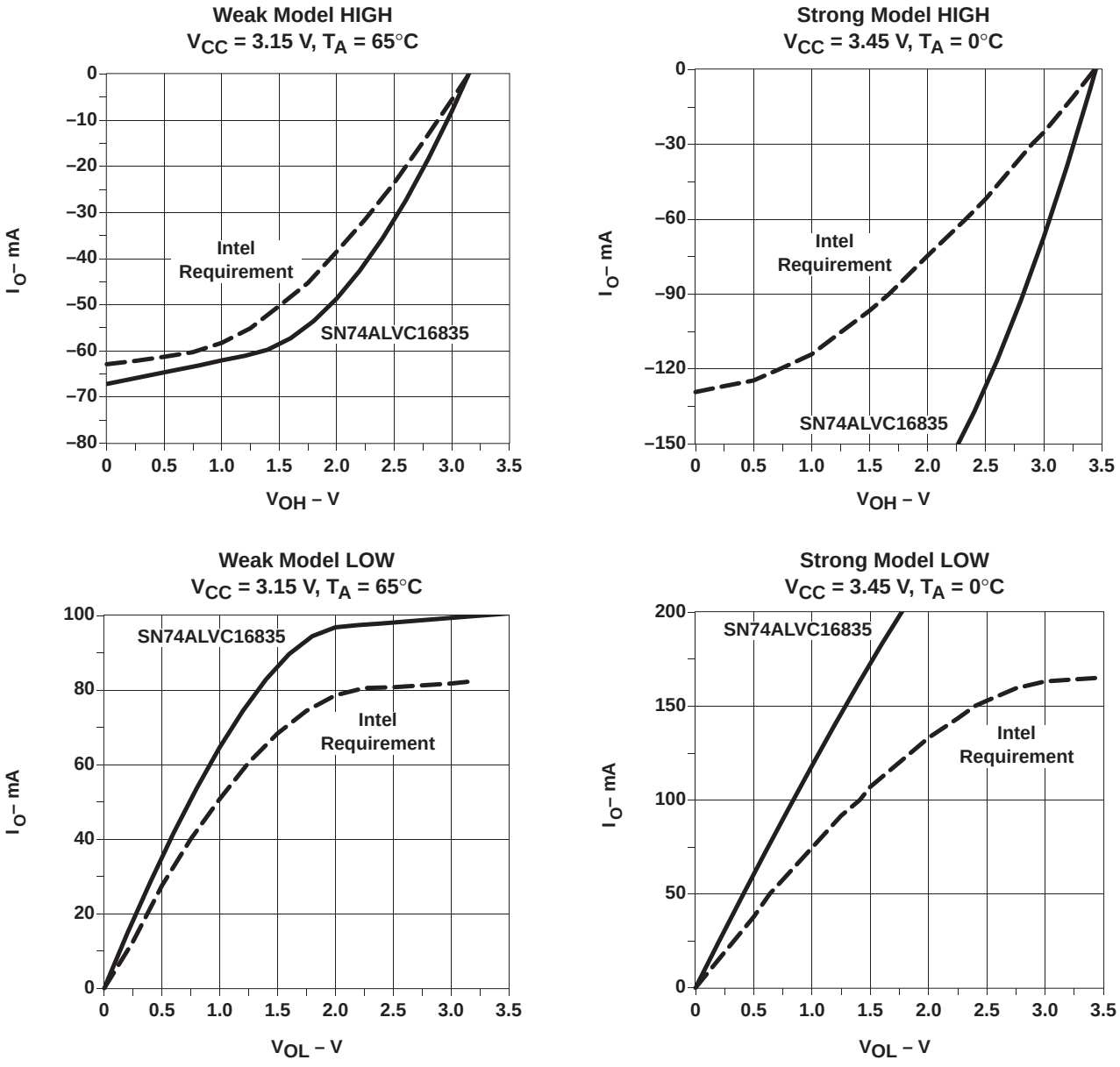

Figure 5. IV Characteristics for SN74ALVC16835 Register Output

Conclusion

The TI SN74ALVC16835 meets or exceeds the requirments defined by Intel in the PC SDRAM Registered DIMM Specification Revision 1.0. To aid design engineers in analyzing electrical characteristics, IBIS models are available from TI's website at http://www.ti.com.

Acknowledgment

Contributors to this report include Stephen M. Nolan, Ji Park, and David Yaeger.