Application Note

Modeling, Analysis, and Tips of Properly Using Demultiplexer

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ABSTRACT

Analog multiplexers are usually bidirectional. Each channel has very similar characteristics in both directions so that the multiplexer can be used as multiplexer or demultiplexer. Multiplexing are commonly used in various applications such as asynchronous data acquisition of multi-channel signals, status read or monitoring of polling system. For multiplexing application, the unselected (OFF) channels are not connected to the common terminal, which is naturally isolated from the signal conditioning circuit after the mux. However, for demultiplexing application, output channels are always connected to the signal conditioning circuit after the mux. For the OFF channels, unwanted voltage can be detected if the output channels are not properly handled.

This application note firstly provides a demultiplexing application example in solar system based on *CD405xB CMOS Single 8-Channel Analog Multiplexer or Demultiplexer With Logic-Level Conversion*, data sheet to show the issue of unwanted voltage at OFF channels. Then, equivalent models for the OFF channel are built to help analysis the root cause. Finally, design and measurement tips are discussed to help engineers use demultiplexer properly.

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Trademarks

1 Introduction

Texas Instruments offers a wide portfolio of analog switches and multiplexers. The general-purpose analog multiplexers *CD405xB* are digitally-controlled analog switches. Since this is bidirectional and each channel has very similar characteristics in both directions, this can also be used as a demultiplexer.

When these devices are used as multiplexers, the CHANNEL IN/OUT terminals are the inputs and the COMMON OUT/IN terminals are the outputs, and vice versa when used as demultiplexers. As shown in Figure 1-1, for multiplexing application, the unselected (OFF) channels are not connected to the common terminal, which is naturally isolated from the signal conditioning circuits after the multiplexer. However, for demultiplexing application, output channels are always connected to the signal conditioning circuit after the mux. For the OFF channels, this can get unwanted voltage if the output channels are not properly handled.

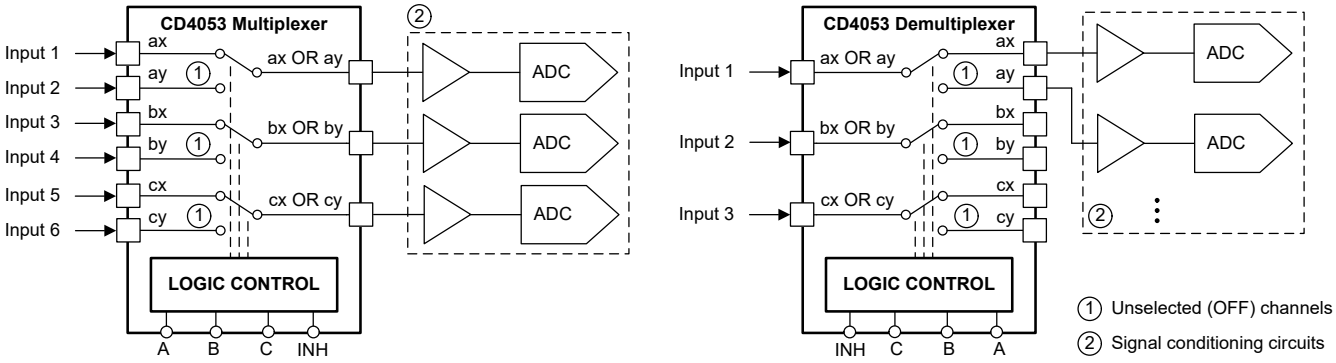

Figure 1-1. Typical Multiplexer and Demultiplexer Application

1.1 Demultiplexing Application Example in Solar System

One demultiplexer application example is to use this in conjunction with amplifiers having different gain for signal segmentation processing. Figure 1-2 shows the application scenario of Smart Combiner Box (also called PV Stream Box) in solar utility power station. Smart Combiner Box is used together with central inverter in middle/large-scale PV grid-connected power generation systems. The Smart Container Box is added between the PV strings and inverter for the purpose of reduction of connection lines between PV strings and inverters, easier maintenance and higher reliability. One of the function is to monitor multi-channel string currents which usually come from current transducer (CT) or hall current sensor.

The current sensor typically has 0 to approximately 5V output or even higher up to 12V, while the recommended ADC full scale range (FSR) of the microcontroller (MCU) is usually 0 approximately 3V. So, amplifier with gain < 1 is needed to attenuate the sampling signal before going to ADC. In addition, the fact is that current sensor usually has much lower accuracy for low current measurement than that of high current measurement. And system errors and noise (such as Vos and drift of the amplifier) of the signal conditioning circuits cannot be totally avoided. To still acquire relatively high accuracy of low current measurement, attenuation of low current signal is not preferred. On the contrary, buffer or amplification is preferred. That means for different amplitude current signal from the same front-end sensor, different back-end signal conditioning circuits are needed. That leads to the signal segmentation processing example using demultiplexers, shown in Figure 1-3.

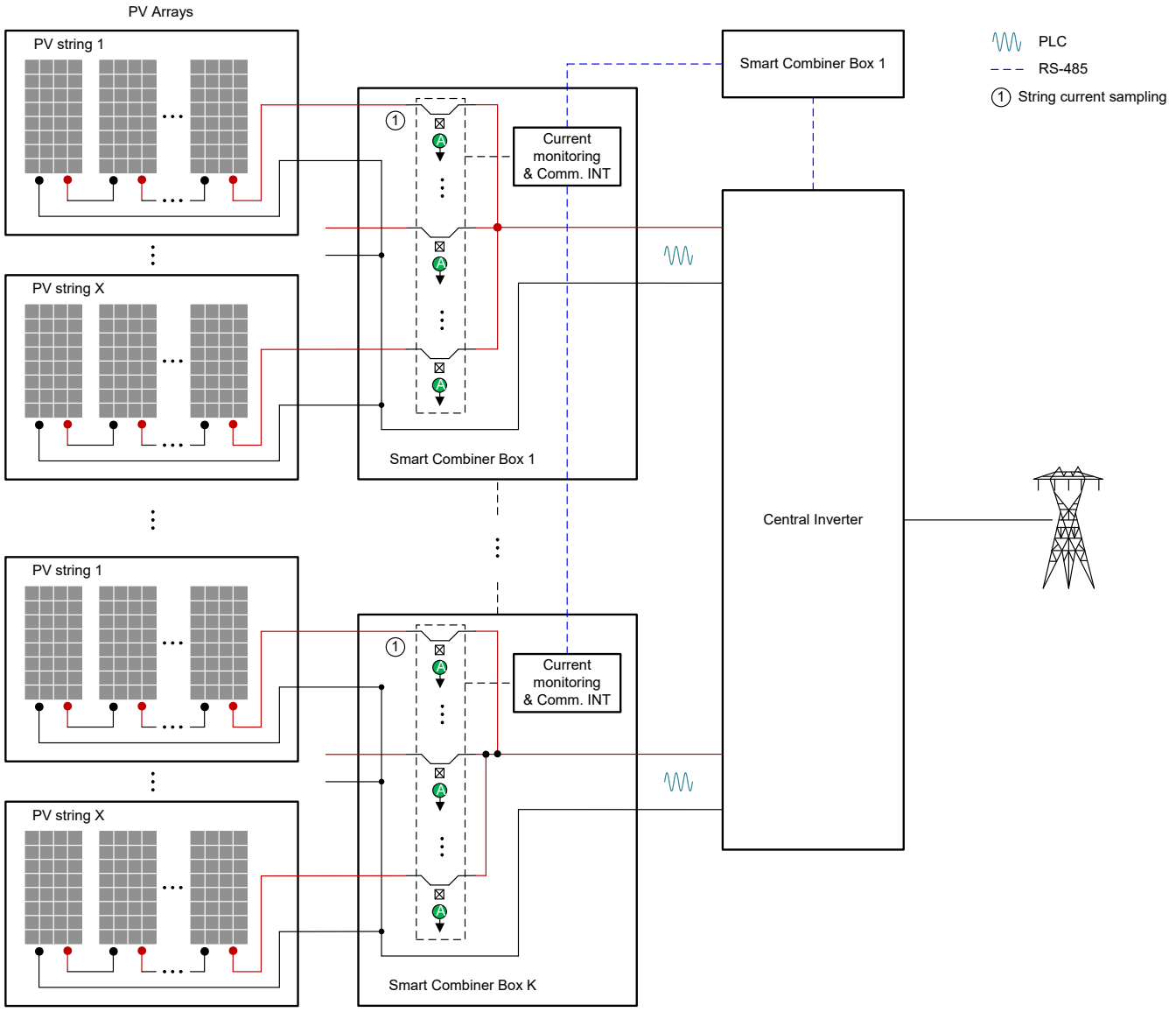

Figure 1-2. Application Scenario of Smart Combiner Box in Solar Utility Power Station

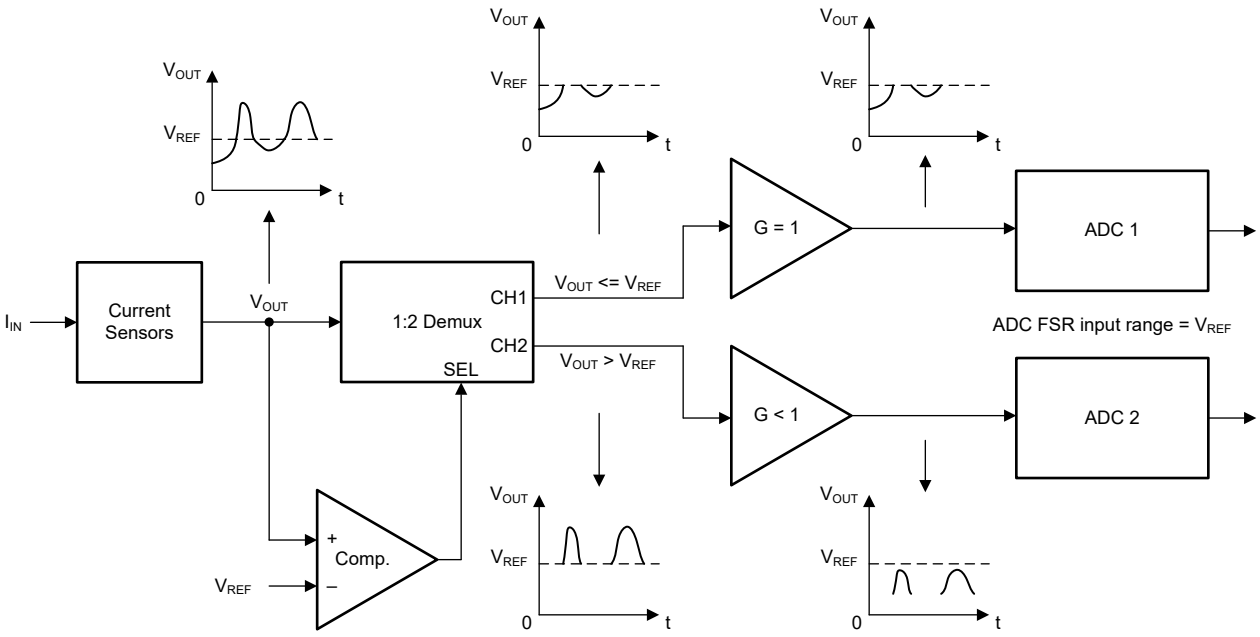

Figure 1-3. Signal Segmentation Processing Example Using Demultiplexers

1.2 Application Issue of Unwanted Voltage at OFF Channels

Figure 1-4 shows a typical application circuit of demultiplexers like CD4053B: both ON and OFF channel outputs are connected directly to inputs of unity gain buffers. For the ON channel, the voltage at output can be slightly smaller than the input due to the existence of ON-state resistance. For the OFF channel, though voltage is blocked from input, there still exists a leakage path from supply to output, which can be modeled as a large resistor. Section 2.1 and Section 2.2 have a detailed discussion on what is going on inside the demultiplexer when the channel is OFF.

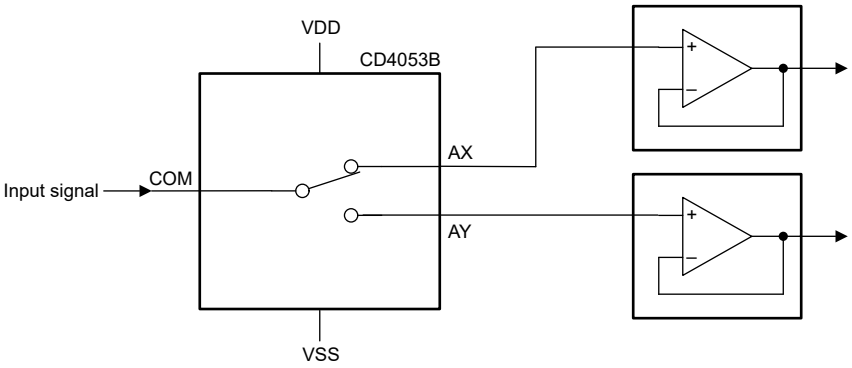

Figure 1-4. Application Circuit of CD4053B as Demux

Meanwhile, the input resistance of unity gain buffer (op amp) is fairly large. If the buffer's input is connected directly to the channel's output, the resistor of channel leakage path and the input resistor of the buffer can form a voltage dividing network. Hence, non-zero voltage can be detected at the OFF-channel output, and the current flowing out of the channel towards the op amp is called OFF channel leakage current. The detected voltage is unwanted because this can also be passed to the following signal conditioning circuit and be recognized by MCU.

Besides, test equipment can fail to measure such voltage if not set up correctly. Figure 1-5 shows a common voltage reading issue. In this case, both multimeter and oscilloscope are used to measure the OFF-channel output voltage. The reading of the multimeter is around 1V, while that of the oscilloscope is almost 0V. This is confusing to know which measurement is correct. Actually, the cause of different readings lies in the different input resistance of these two instruments. Detailed measurement considerations is given in Section 4.1.

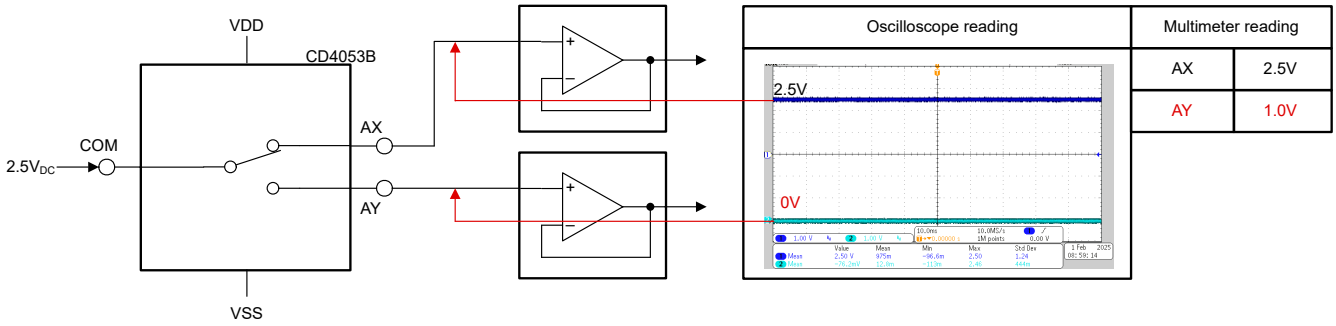

Figure 1-5. Voltage Reading Issue at Demux OFF-channel Output

2 OFF Channel Model Analysis

Analog multiplexers or demultiplexers are essentially combination of switches. The design of CD4053B is based on transmission gate switch. As shown in Figure 2-1, an N-channel transistor and a P-channel transistor are connected in parallel and are controlled by reverse logic so that the transistor can be turned ON or OFF at the same time. Such structure is used because the paralleled ON-state resistance is much flatter across voltage than that of individual transistors, as shown in Figure 2-2. Refer to *Selecting the Correct Texas Instruments Signal Switch*, application note for more information.

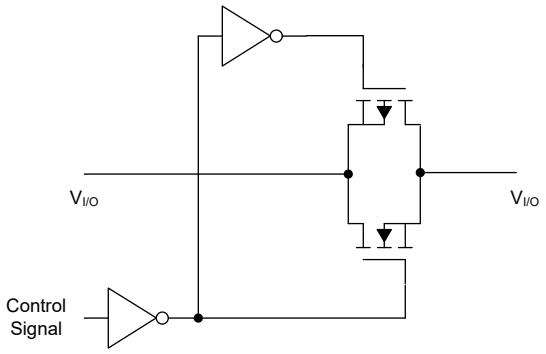

Figure 2-1. Transmission Gate Switch

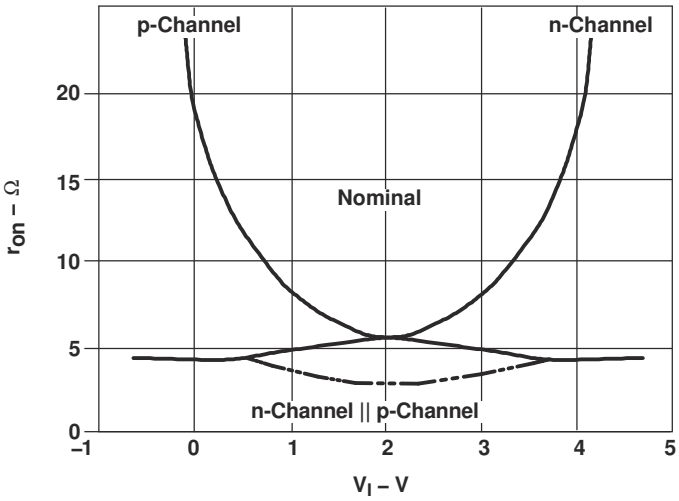

Figure 2-2. On-State Resistance vs Input Voltage for a Parallel n-/p-Channel FET Switch

2.1 Channel Structure

Figure 2-3 shows the typical channel structure such as CD4053B. NMOS path are in parallel with PMOS path as in a transmission gate switch to achieve a flatter ON-state resistance. Two back-to-back NMOS transistors are utilized to compose the NMOS path, and another switch SW is connected between the mid-point of transistor pairs and VSS. When the channel is ON, transistors are ON, SW is OFF, and voltage signal is conveyed from input to output. When the channel is OFF, transistors are OFF, SW is ON, and the voltage of mid-point is pulled down to VSS.

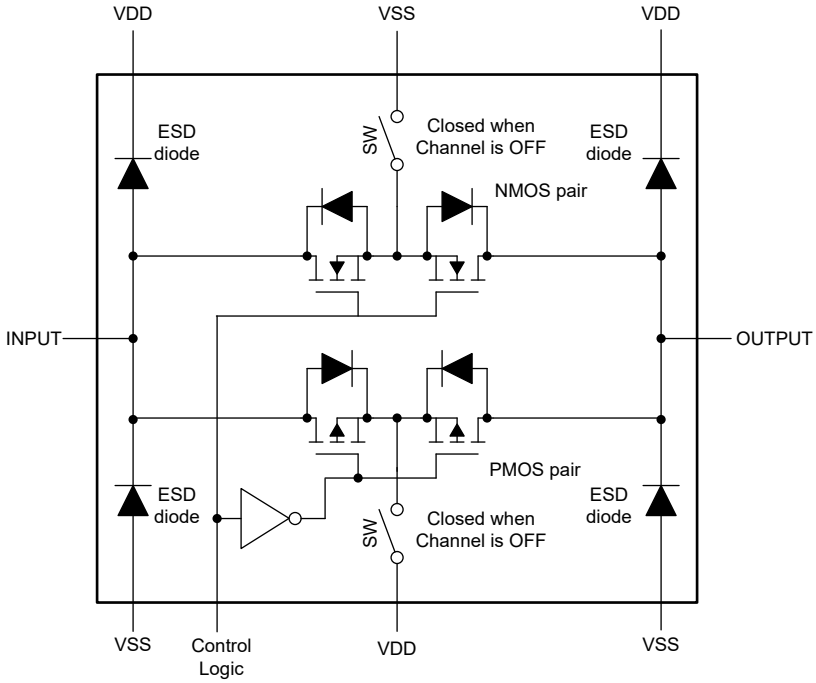

Figure 2-3. Channel Structure of CD4053B

The PMOS path in Figure 2-3 works similarly to the NMOS path. Additionally, ESD diodes are placed at the IO pins to clamp the output voltage range to stay in between VDD and VSS in the case of an overvoltage event.

Assume the input is DC voltage, which is the example in Figure 1-5. Since both OFF-state transistors and ESD diode are not really OFF, there is a small amount of leakage current flowing through transistors and diodes to the output load. The OFF-channel leakage current paths are shown as in Figure 2-4.

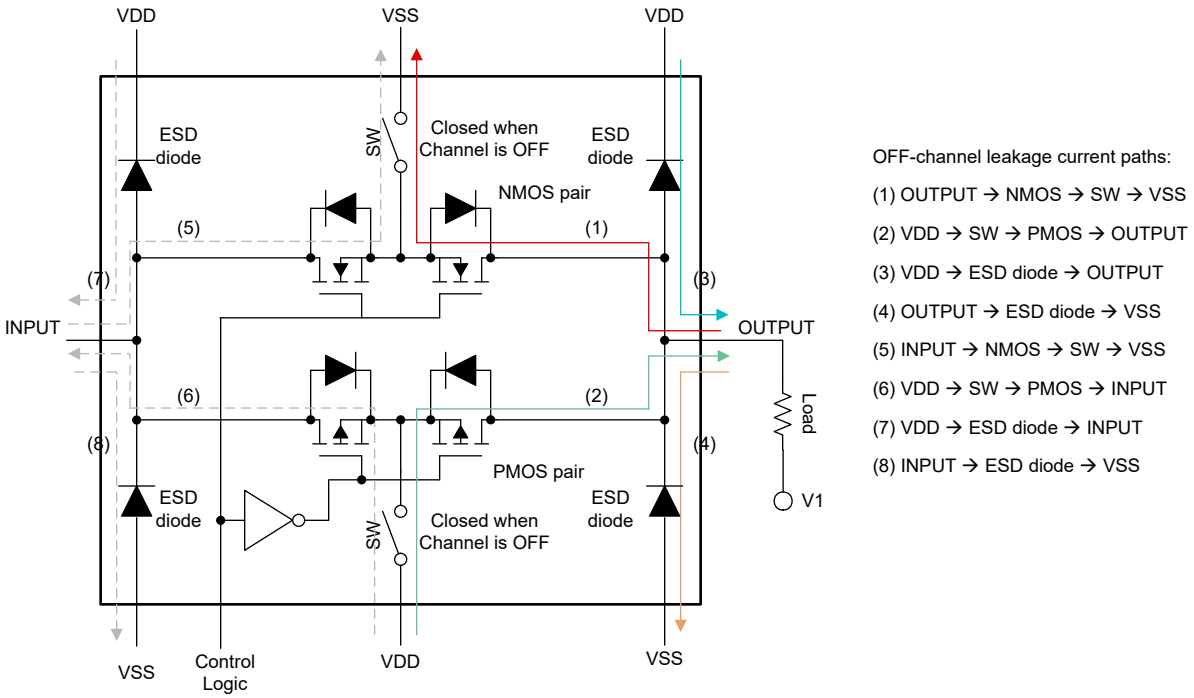

Figure 2-4. OFF-channel Leakage Current Paths

As mentioned above, when the channel is OFF, SW is ON and sinks the leakage current to VSS. Since the ON-state resistance of SW is much smaller than the OFF-state resistance of NMOS transistor, most of the leakage current from input side flows to VSS instead of output. Similarly, for the PMOS path, the leakage current loop forms between input and VDD, rather than between input and output. In other words, the channel structure in Figure 2-3 almost blocks input-to-output leakage paths (5)(6)(7)(8).

For the rest of output leakage paths (1)(2)(3)(4), current is sourced from VDD or is sunk by VSS. The sourcing and sinking current flows in opposite direction, canceling each other out to achieve a fairly low leakage current flowing through the output load.

Additionally, not all mux channel structure has the input-to-output leakage blocking feature. Take the channel structure in Figure 2-5 as an example:

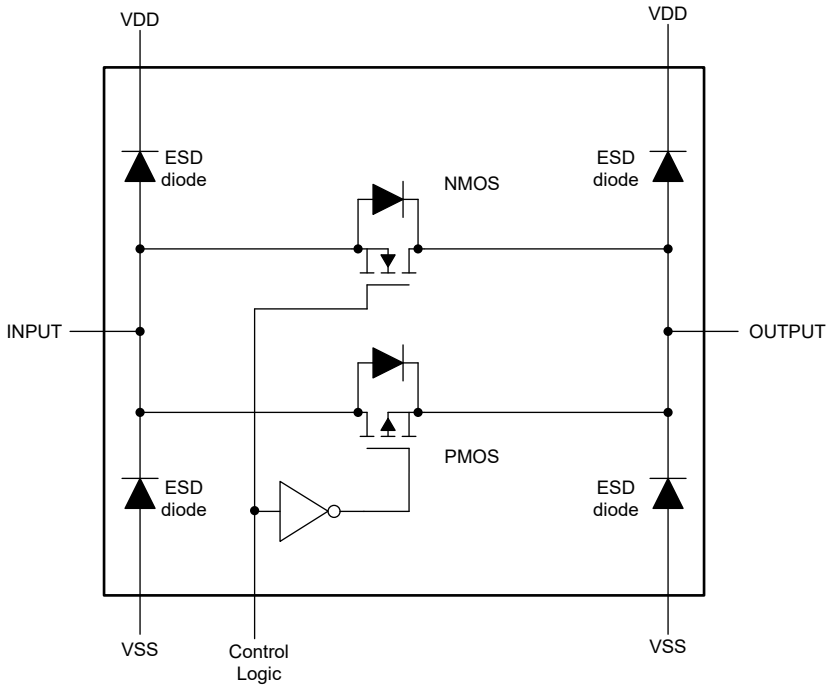

Figure 2-5. Channel Structure Without Input-to-output Leakage Blocking Feature

This structure does not have the additional switch path to guide the input leakage current to VDD/VSS. The OFF-channel leakage current paths are shown in Figure 2-6.

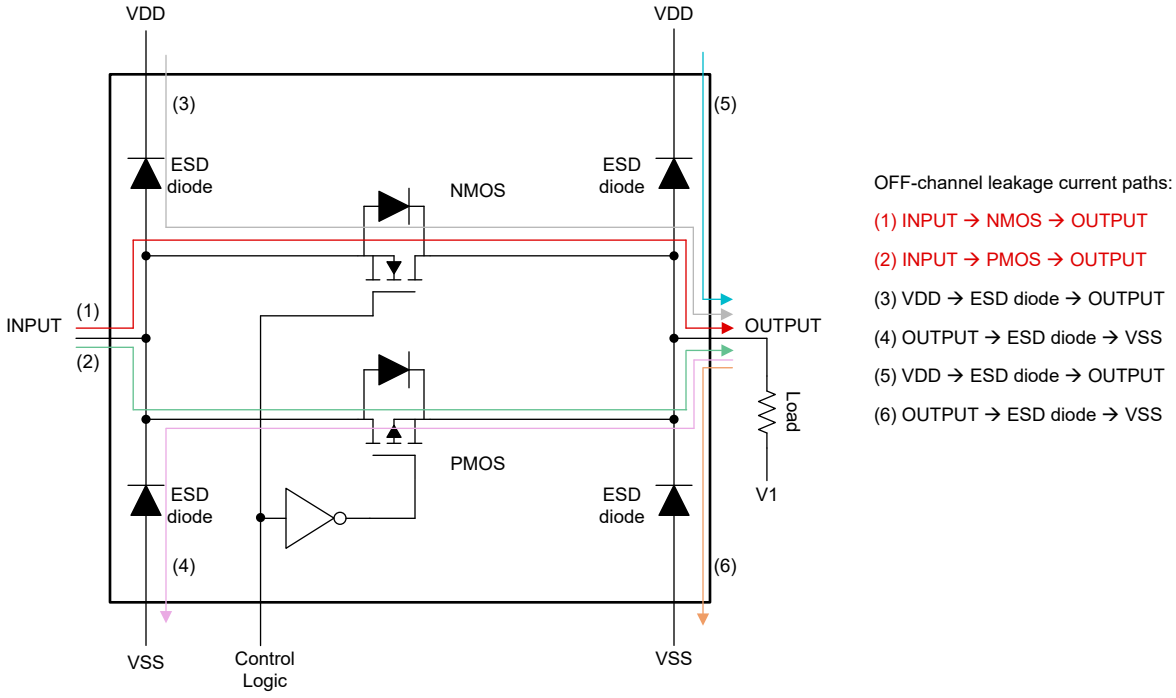

Figure 2-6. OFF-channel Leakage Current Paths With Input-to-to-output Leakage

The OFF-state resistance of NMOS provides paths (1)(2) for leakage current to flow from input to output. Other leakage current in paths (3)(4)(5)(6) cancel each other in opposite direction like in Figure 2-4. The leakage current in paths (1)(2) runs in the same direction and cannot cancel each other. Therefore, the output leakage of this structure can be larger.

2.2 Equivalent Resistor Model

An equivalent model can be built to describe the OFF-state leakage and make this easier for understanding and calculation. Both the OFF-state transistors and reverse-biased diodes can be regarded as large resistors, as shown in Figure 2-7. Other resistance for example, line resistance is neglected for simplification in this case.

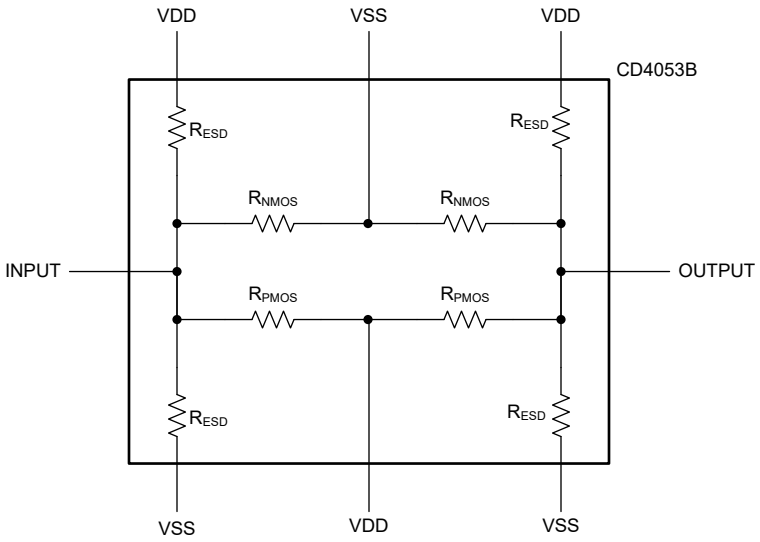

Figure 2-7. Replacing Transistors and Diodes With Resistors

From the output side, most of the leakage from input is sunk by the mid-point of transistors and cannot be seen at the output. Therefore, the paths linked to input can be removed as in Figure 2-8.

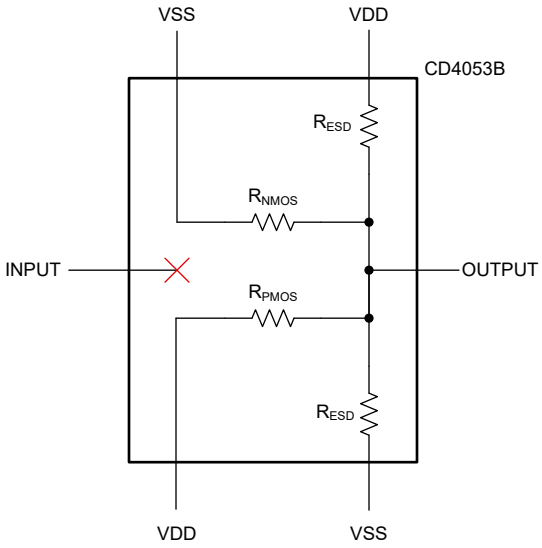

Figure 2-8. Removing Leakage Paths Linked to Input

The paths linked to the same pin (VDD/VSS) can be combined and the final equivalent resistor model is shown in Figure 2-9.

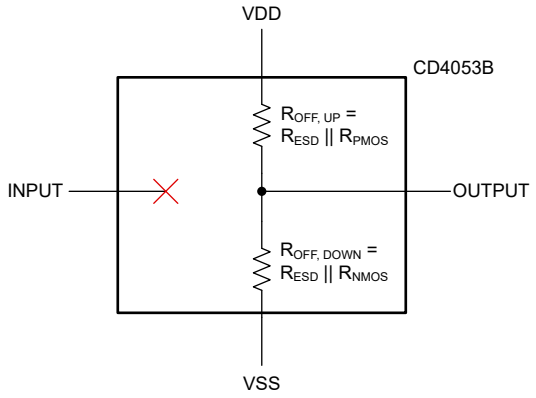

Figure 2-9. Equivalent Resistor Model of OFF Channel

To calculate the value of equivalent resistors $R_{off,up}$ and $R_{off,down}$, connect the output to VDD and VSS respectively, and measure the current flowing out of the output.

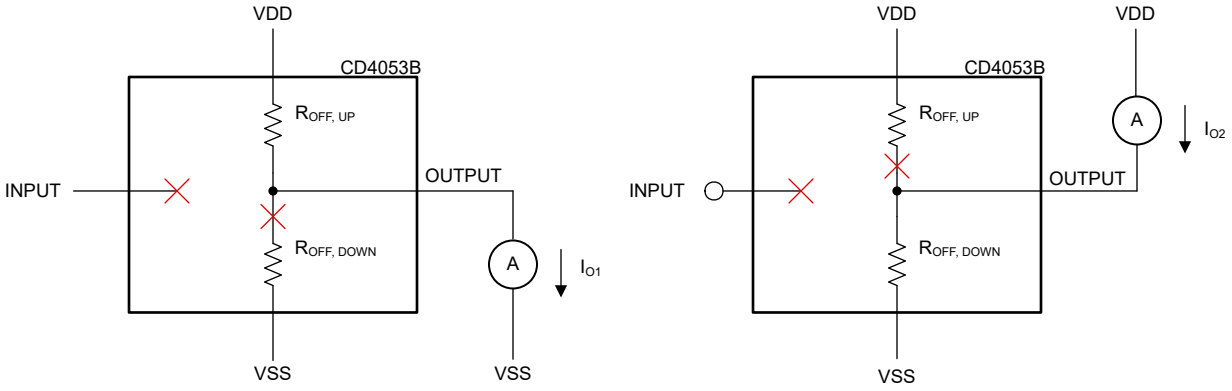

Figure 2-10. Calculating Value of Equivalent Resistors

The $R_{off,up}$ and $R_{off,down}$ can be calculated as the following:

$$R_{off,up} = \frac{VDD - VSS}{|I_{O1}|} \quad (1)$$

$$R_{off,\ down} = \frac{VDD - VSS}{|I_{O2}|} \quad (2)$$

Due to the symmetry of channel structure, a reasonable assumption is that $R_{off,up}$ and $R_{off,down}$ are of the same order of magnitude, for example, if $R_{off,up}$ is tens of MΩ, $R_{off,down}$ can also be assumed to be tens of MΩ.

3 Fix OFF Channel Output Voltage to Ground

As shown in Figure 3-1, the output voltage of OFF channel can be defined by applying any voltage level between VDD and VSS on this (for voltage greater than VDD or less than VSS, the output can be clamped by ESD diodes at VDD or VSS).

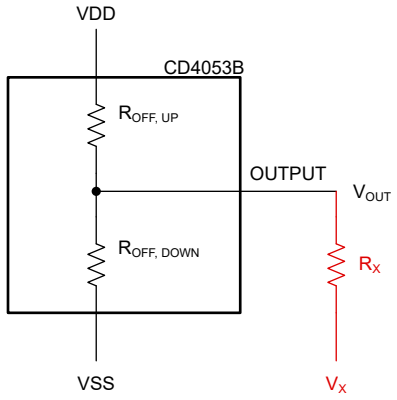

Figure 3-1. Define Output Voltage of OFF Channel

The output voltage can be calculated by solving Kirchhoff's Current Law equation:

$$\frac{V_{DD}-V_{OUT}}{R_{off,up}}+\frac{V_{SS}-V_{OUT}}{R_{off,down}}=\frac{V_{OUT}-V_X}{R_X} \tag{3}$$

Usually, the recommendation is fix the uncertain OFF-channel voltage to ground so that no unwanted voltage can be read by MCU.

The following three designs are proposed to satisfy this need.

3.1 Pull-down Resistor

A pull-down resistor R1 can be connected to the output as shown in Figure 3-2.

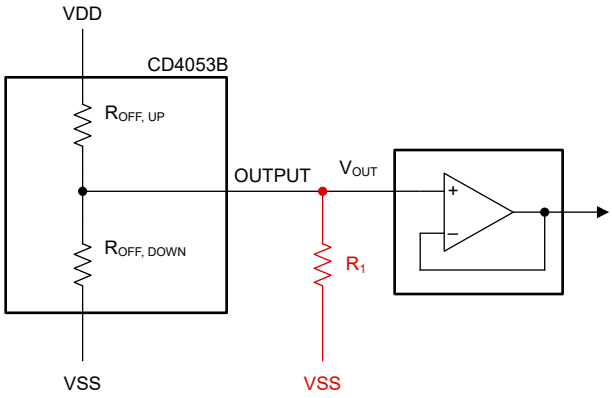

Figure 3-2. Pull-down Resistor

A trade-off exists in the selection of R1.

R1 needs to be chosen far more less than the input resistance of op amp and the OFF resistance of CD4053B to make sure the voltage across is nearly zero.

Equation (3) can be used to prove this. Assuming VSS = 0, in this case, V_X = 0, R_X = R1 ‖ $R_{in,amp}$, where $R_{in,amp}$ is the input resistance of unity gain buffer. Then Equation 3 can be rewritten as:

$$\frac{V_{DD}-V_{OUT}}{R_{off,up}}-\frac{V_{OUT}}{R_{off,down}}=\frac{V_{OUT}}{R1\parallel R_{in,amp}} \tag{4}$$

$$V_{OUT}=V_{DD}\frac{R_{off,down}\parallel R1\parallel R_{in,amp}}{R_{off,down}\parallel R1\parallel R_{in,amp}+R_{off,up}} \tag{5}$$

If R1 ≪ $R_{off,up}$, $R_{off,down}$, $R_{in,amp}$, the item $R_{off,down}$ ‖ R1 ‖ $R_{in,amp}$ ≈ R1, and:

$$V_{OUT} \approx V_{DD}\frac{R_1}{R_1 + R_{off,up}} = V_{DD}\frac{1}{1 + \frac{R_{off,up}}{R_1}} \approx 0 \quad (6)$$

To validate Equation 6, R1 must be at least smaller than $R_{off,up}$, $R_{off,down}$ and $R_{in,amp}$. The following paragraphs use the data sheet of op amp and multiplexer to calculate these values.

$R_{in,amp}$ is usually calculated with common-mode voltage and input bias current:

$$R_{in,amp} = \frac{\Delta V_{CM}}{\Delta I_B} \quad (7)$$

The relationship between common-mode voltage and input bias current is given in the data sheet. Take TLV9004 as an example:

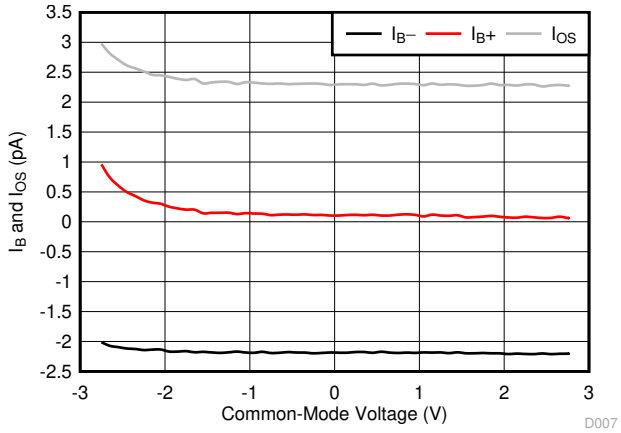

Figure 3-3. I_B and I_{OS} vs Common-Mode Voltage

ΔV_{CM} = 5.5V, $\Delta I_B \approx$ 0.9pA, and $R_{in,amp}$ is calculated to be 6.1TΩ. Therefore, R1 must be less than 610GΩ.

The off resistance $R_{off,up}$ can be calculated by Equation 1.

For CD4053B:

- The typical value of I_{OFF} mentioned in the data sheet is 0.3nA (with VDD = 18V, VEE = VSS = 0, ambient temperature = 25℃). Then $R_{off,up}$ is calculated to be 60GΩ.
- The largest value of is 1000nA (with VDD = 18V, VEE = VSS = 0, ambient temperature = 85 ℃). Then $R_{off,up}$ is calculated to be 18MΩ.

Using the typical value of I_{OFF} to calculate, R1 needs to be less than 6GΩ. Using the largest value of I_{OFF} to calculate, R1 needs to be less than 1.8MΩ.

To choose the appropriate R1 value, three considerations are made here:

- Less than 6GΩ is possibly not applied to every situation, because the typical value of I_{OFF} does not take the temperature variation into account.
- Less than 1.8MΩ can be an overestimation, since the largest value of I_{OFF} also applies to CD4051B, which is a sum of 8 channels' leakage.
- Too large value of R1 in the layout can make the circuit vulnerable to noise and interference.

To be more reliable, R1 is recommended to be no more than 1MΩ.

Also, R1 needs to be large enough so that when the channel is turned ON, the voltage on R1 is almost equal to the input voltage. Figure 3-4 models the effect of R1 on the signal transmission when the channel is ON.

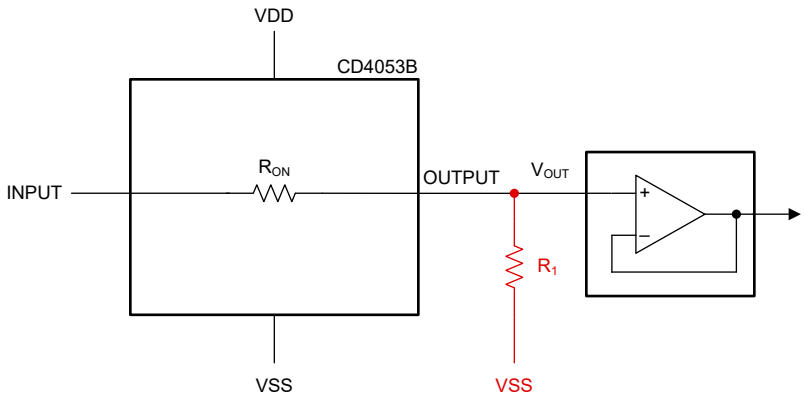

Figure 3-4. Pull-down Resistor's Effect When Channel Is ON

Assuming VSS = 0, V_{OUT} can be written as:

$$V_{OUT} = V_{IN}\frac{R_1 \parallel R_{in,amp}}{R_1 \parallel R_{in,amp} + R_{ON}} \quad (8)$$

Since R1 is usually quite small compared to the input resistance of op amp,

$$V_{OUT} \approx V_{IN}\frac{R_1}{R_1 + R_{ON}} \quad (9)$$

As can be seen from the previous equation, V_{OUT} is smaller than V_{IN}, and this effect needs to not be neglected when R1 is not large enough. The recommendation is that R1 needs to be at least 10 times of R_{ON} to avoid too much degradation of input signal.

For CD4053B, the largest value of R_{ON} mentioned in the data sheet is 1300Ω (with VDD = 5V, VEE = VSS = 0, ambient temperature = 125°C). Hence, at least 10kΩ is required for R1.

To sum up, the recommended value of R1 is 10kΩ to approximately 1MΩ.

3.2 Pull-down Capacitor

Theoretically, a capacitor cannot pull the OFF-channel output node down to ground in DC circumstances since the capacitor is regarded as an infinitely large impedance for DC signal, whatever the value of capacitor is. However, in the real test, a large capacitor does work to pull down the voltage at output.

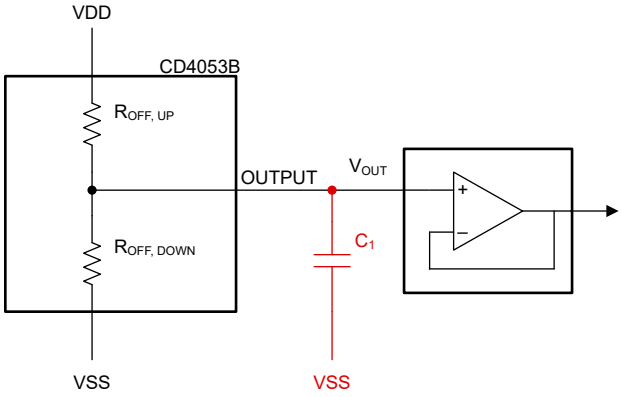

Figure 3-5. Pull-down Capacitor

This is due to the non-designed for performance of capacitor products. The actual capacitor has a finite resistance value because a small amount of current flows between the insulated electrodes. This resistance value is called *insulation resistance*.

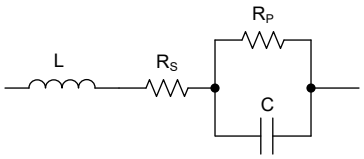

Figure 3-6. Real-world Capacitor Model

The insulation resistance can be calculated by looking up the data sheet of the capacitor. Take TDK's capacitors as an example. According to the TDK Product Center, the insulation resistance is the smaller value of 10GΩ and 100MΩ·uF for capacitors with a rated voltage of 6.3 to approximately 16V. For capacitance of 1uF, the paralleled resistance of this capacitor is 100MΩ, which is small enough compared to the typical value of off-channel equivalent resistance calculated in Section 3.1 Therefore, this can pull down the output voltage to ground.

Plus, the capacitor can also reduce the AC interference coupled in the circuit, such as the 50Hz noise.

This design works well for DC input scenario. For AC input, the reactance of capacitance needs to also be taken into consideration, which is not discussed in this application note.

3.3 Bleeder Resistor With a Switch

To avoid pull-down resistor's value selection trade-off mentioned in Section 3.1, a switch can be added in series with the resistor, as is depicted in Figure 3-7.

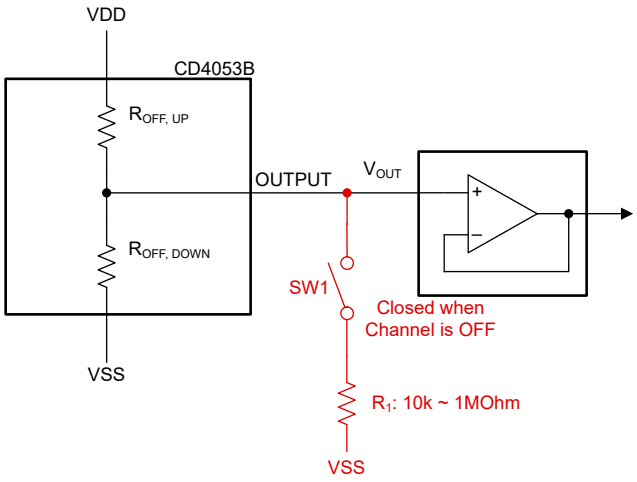

Figure 3-7. Bleeder Resistor With a Switch

The switch SW1 can be controlled with the channel selection signal of demultiplexer:

- When this channel is OFF, SW1 is turned ON to connect the pull-down resistor R1 into the circuit. Then the output voltage can be fixed at ground with R1.
- When this channel is ON, SW1 is turned OFF to block the path so that R1 is not connected to the circuit. Because the input resistance of op amp is very large, the input voltage signal can be conveyed to op amp with little loss.

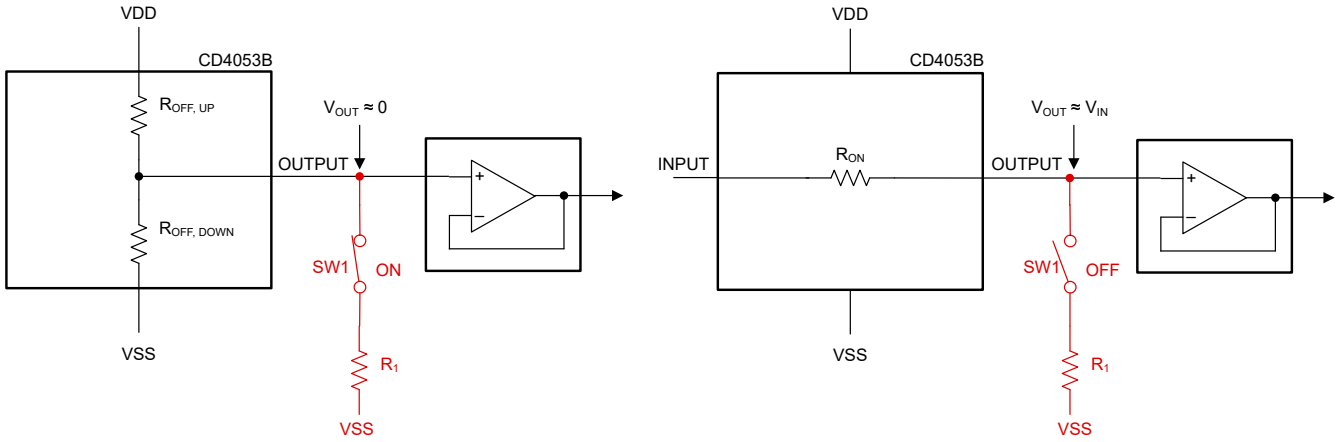

Figure 3-8. Control Scheme of SW1

Refer to application brief *How to Prevent Errors in Voltage Readings When Using Multiplexers with High Input Impedance Op-Amps* for more information.

4 Test and Measurement

4.1 Measurement Considerations

As mentioned in Section 1.2, the voltage readings of the multimeter and oscilloscope are different at the same OFF-channel output node. This is mainly due to the difference in input resistance of two instruments. As shown in Figure 4-1, when the probe is placed at two ends of the device under test (DUT) to detect voltage, the input resistance of multimeter and oscilloscope is actually in parallel with DUT.

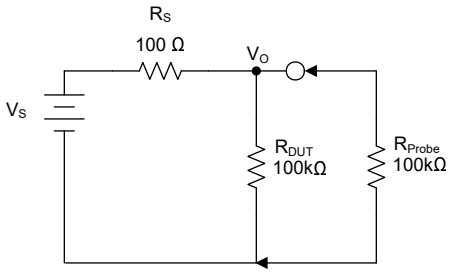

Figure 4-1. Loading Effect of Test Equipment

Usually, the input resistance of test equipment is large enough so that the effect of paralleling can be neglected. However, when the resistance of DUT is comparable to or even larger than the input resistance of test equipment, the effect of paralleling cannot be neglected and error can occur.

Such is the case in CD4053B's application, where the OFF-channel equivalent resistance $R_{off,up}$, $R_{off,down}$, and op amp input resistance $R_{in,amp}$ are enormous. The effect of test equipment on measurement is modeled by R_{test} in Figure 4-2.

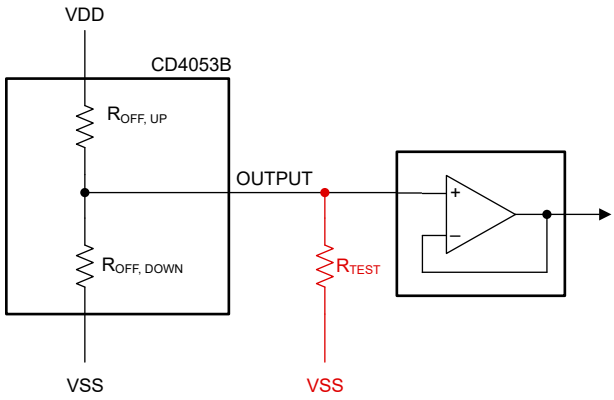

Figure 4-2. Effect of Test Equipment on Measurement

R_{test} is in parallel with $R_{off,down}$ and $R_{in,amp}$. The paralleled resistors $R_{off,down} \parallel R_{test} \parallel R_{in,amp}$ divide the supply voltage with $R_{off,up}$. Therefore, different value of R_{test} can lead to different divided voltage at the OFF-channel output.

Take Tektronix TPP0500B probe for oscilloscope as an example. The nominal probe input resistance R_{test} 10MΩ. Assume $R_{off,up}$ and $R_{off,down}$ to be 60GΩ and $R_{in,amp}$ to be 6.1 TΩ (typical value calculated in Section 3.1). Then R_{test} is far less than $R_{off,up}$, $R_{off,down}$ and $R_{in,amp}$. Therefore, the reading of oscilloscope is nearly 0V according to Equation 6 which is not the correct value.

For multimeter, the input resistance in voltage measurement mode is usually defined by the resistor network inside the network, which is not specified in the data sheet and can vary among different products. Keysight 34401A supports setting of input resistance to >10GΩ level. Testing with this setting can lead to a voltage reading of around 1V . Normally, the multimeter's input resistance is fixed at 10MΩ, and the voltage reading is almost zero, similar to the result with oscilloscope.

To eliminate the effect of input resistance of test equipment, test the output voltage at the output of the unity gain buffer. According to the principle of unity gain buffer, the output voltage equals to the input voltage, and the input

is isolated from the output, which means that the output load of unity gain buffer does not affect input. And no loading error can occur because the output resistance of unity gain buffer is much smaller compared to the input resistance of test equipment (For TLV9004, the open-loop output impedance in the data sheet is 1.2kΩ).

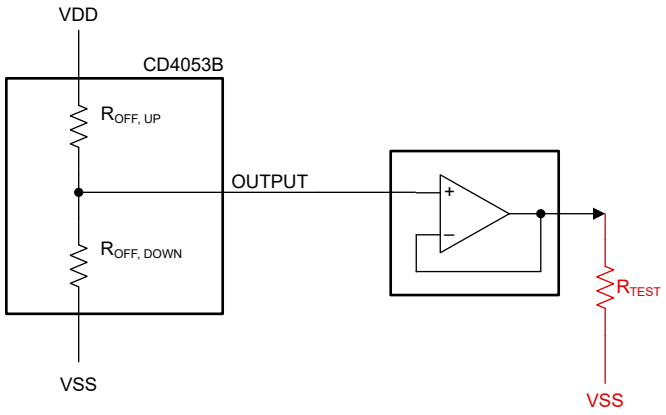

Figure 4-3. Measuring Voltage With Help of Unity Gain Buffer

4.2 Test Result

Figure 4-4 and Figure 4-5 show the voltage readings with oscilloscope and multimeter at OFF-channel output and unity gain buffer output with no pull-down design added. VDD equals to 5V and VSS equals to 0V. The readings are quite different at the OFF-channel output due to the loading effect of test equipment. By changing the measurement point at unity gain buffer output, such effect can be eliminated with around 1V DC voltage read by both instruments. The voltage ripple is due to 50Hz line frequency interference.

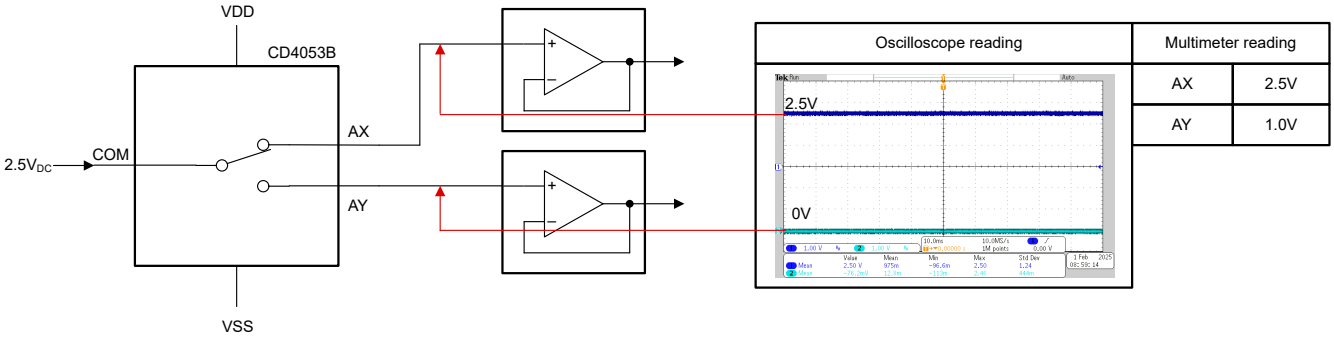

Figure 4-4. Improper Voltage Reading at OFF-channel Output

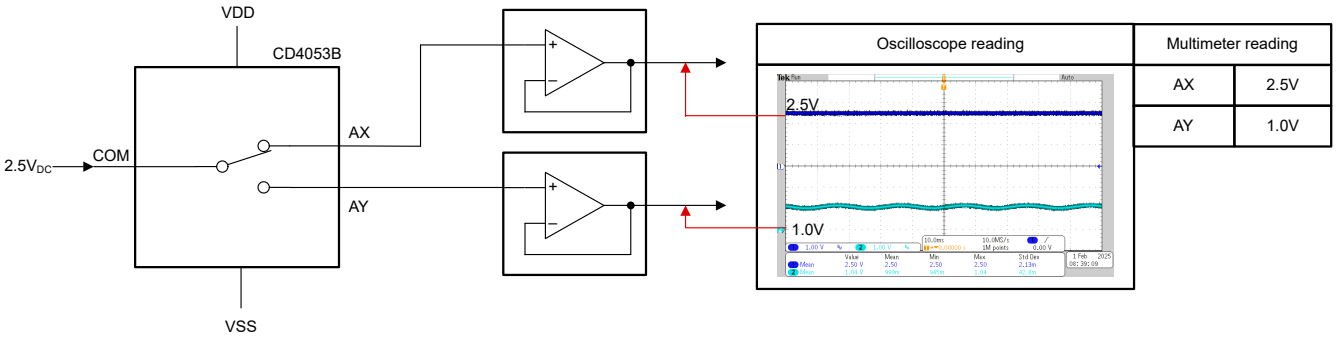

Figure 4-5. Correct Voltage Reading at Unity Gain Buffer Output

Figure 4-6 and Figure 4-7 show the test results with pull-down resistor and capacitor designs deployed. With 2.5V input voltage, the output of unity gain buffer linked to ON channel is 2.5V, and the output of unity gain buffer output linked to OFF channel is nearly 0V.

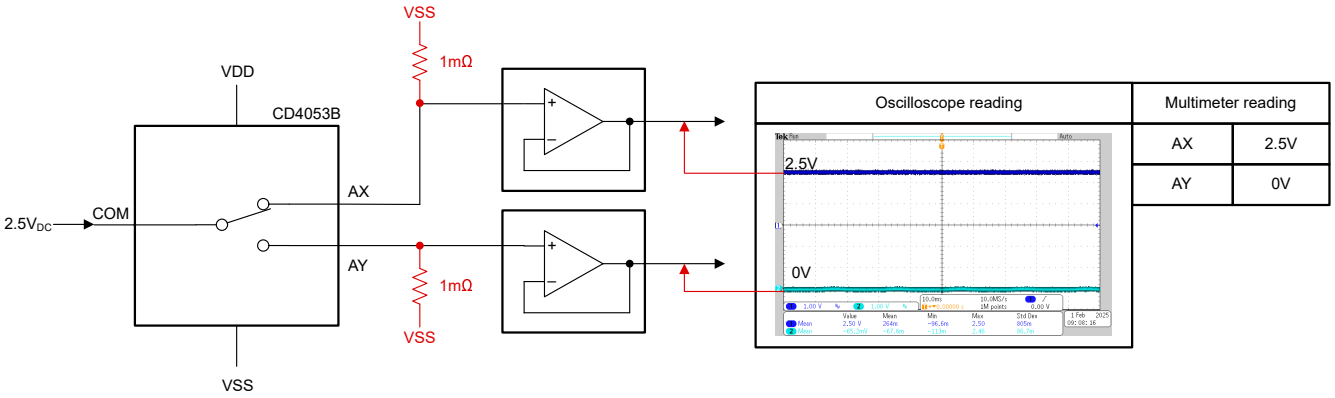

Figure 4-6. Voltage Reading With 1MΩ Pull-down Resistor Design

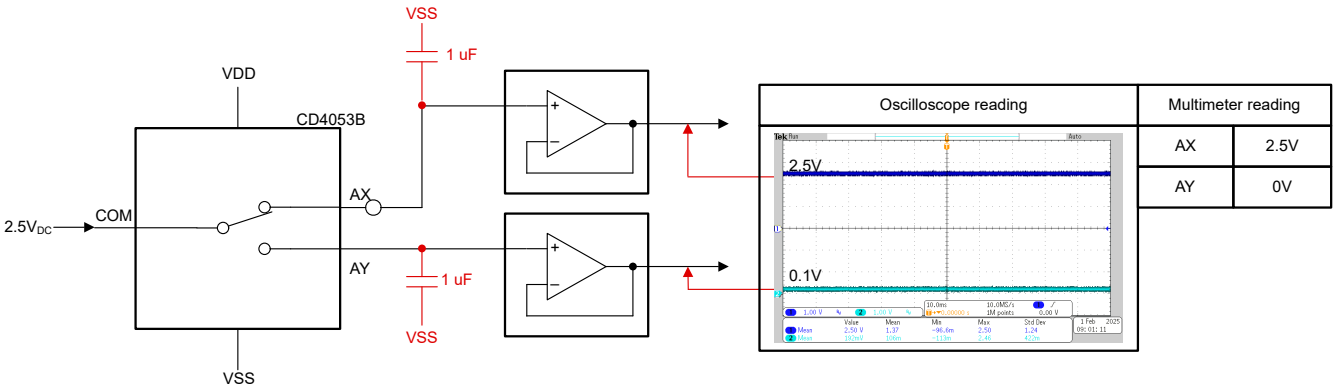

Figure 4-7. Voltage Reading With 1 uF Pull-down Capacitor Design

5 Summary

The bidirectional operation characteristic of signal path enables analog multiplexer to support both multiplexer and demultiplexer usage. In demultiplexer application, when the OFF channel is directly connected to loads with large resistance like op amps, unwanted voltage signal can appear at the OFF-channel output and can be conveyed to the proceeding processor. This application note analyzes the problem by building an equivalent resistor model for OFF channel and proposes three designs to tackle. Since the scenario is sensitive to the input resistance of test equipment, measurement tips are also provided to avoid voltage reading mistakes.

6 References

- Texas Instruments, *CD405xB CMOS Single 8-Channel Analog Multiplexer or Demultiplexer With Logic-Level Conversion*, data sheet.
- Texas Instruments, *Selecting the Correct Texas Instruments Signal Switch*, data sheet.
- Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems*, data sheet.
- Murata, *Insulation resistance and leakage current of ceramic capacitor | Murata Manufacturing Articles*
- Texas Instruments, *How to Prevent Errors in Voltage Readings When Using Multiplexers with High Input Impedance Op-Amps*, application brief.

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