Application Note

Guarding in Multiplexer Applications

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ABSTRACT

TI offers an array of extremely low leakage current multiplexers that can be used for a variety of precision applications. However, to achieve such low leakage in an application that uses a high-performance multiplexer, guarding techniques must be implemented to prohibit PCB parasitics and environmental factors from contributing non-negligible leakages that can affect measurements in a sensitive circuit. This application note outlines the caveats that leakage currents can introduce in precision applications and why guarding techniques can be essential for ensuring the highest multiplexer performance.

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Trademarks

1 What is Guarding?

Guarding is a PCB layout technique that helps shield sensitive nets from parasitic circuit elements or external influences that can cause noise or leakages which can impact the performance of an application. These leakages can be from a multitude of sources, however, applications requiring the most accurate solutions need to consider all potential leakage sources. A model of adjacent trace parasitics and possible environment influences can be seen in Figure 1-1 (top view).

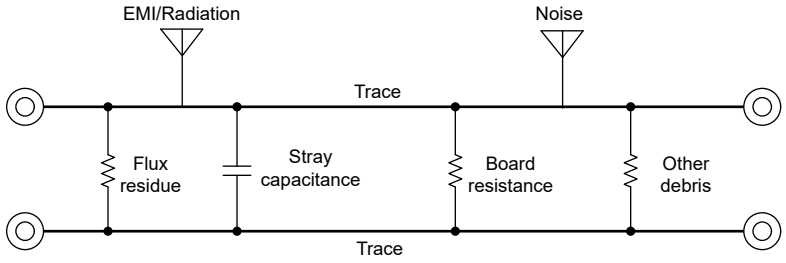

Figure 1-1. PCB Leakage Source Model

As seen above, leakage paths can be formed from several sources including flux on the board, debris (surface leakages), electrical interferences, and of course the inherent board resistance and dielectrics between conductors (traces in this case). Now, while the first two can be removed by having clean manufacturing processes and operational areas or burying the sensitive traces within the PBC, the third and fourth instances can affect any PCB and can cause significant leakages to form if proper guarding is not implemented into the design.

Take the trace to trace resistance as an example. At just a 5 V potential difference between two traces on a PCB and using an estimated trace to trace resistance in the Gigaohm range, this would amount to nA's worth of leakage just from this relatively small delta alone. So one can imagine the increased leakage the net would see from any substantial increase in voltage present on the board. Hence why incorporating a guarding scheme can be so important to keep leakage currents at bay.

Guarding techniques implement active conductors that are at the same potential as the sensitive net and surround said net to create an extremely low leakage environment. With the guard ring and the net at the same potential, this effectively creates an incredibly small voltage delta between the trace and immediate surrounding area which drastically reduces the possibility of stray leakage currents leaking into this area of the PCB. Figure 1-2 outlines a typical guarding scheme.

Figure 1-2. Trace Guarding

2 Guarding Best Practices

To ensure the highest level of leakage performance, there are some best practices for guarding that should be adhered to. As mentioned earlier, the first barrier that needs to be protected again is surface contamination that can often lead to stray leakage currents. In order to counteract this, it is best to bury sensitive nets within the PCB itself to reduce the possibility of any type of debris or contamination from providing leakage paths to the sensitive nets. To go even further, the next recommendation would be to implement a “boxing” ring around the entire net. What this means is that in addition to the traditional guarding which is just on the same layer as the net, the layers above and below also provide shielding by being at the same potential as the guard traces. This type of configuration will mimic the effects of a shielding cable in which it shields the net 360°. Figure 2-1 provides a visual representation.

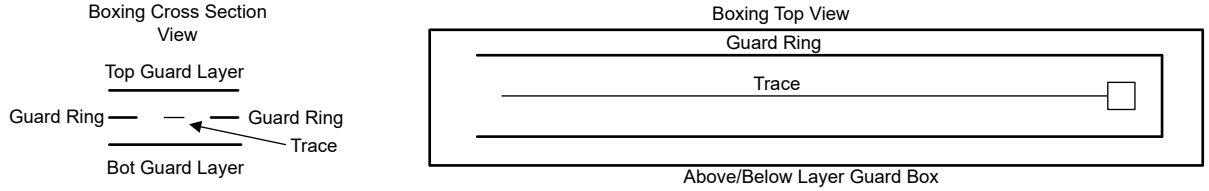

Figure 2-1. PCB Boxing Guard

With package sizes becoming smaller and smaller, this can introduce challenges in incorporating a full guard ring on the trace due to the pitch of some packages. To address this, the designer will need to run the guard ring and traces as close to the pin as possible while still leaving some space between the adjacent guard traces (see Figure 2-2).

Figure 2-2. Small Pitch Guarding

However, if a full guard is required, TI does offer devices that are more guarding friendly in SOIC packages. These are wider pitch devices which will allow for a full guard to be implemented around each pin of the device. One such example can be seen using the MUX36S16DWR, as shown in Figure 2-3.

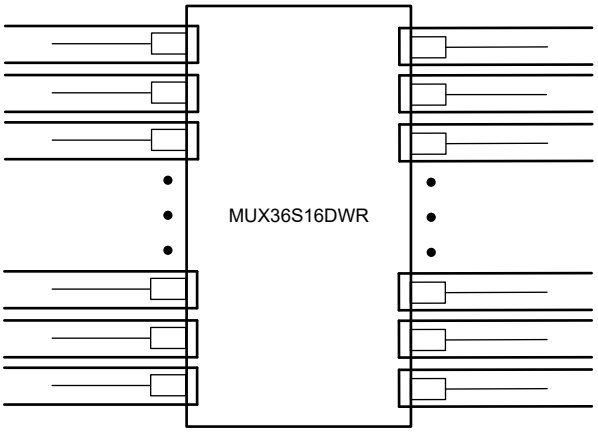

Figure 2-3. Wide Pitch Guarding

Lastly, the design must ensure that the guard is well generated. What this means is that the guard voltage mimics the net voltage as closely as possible to provide the optimal guarding results. To do this, one must just simply incorporate a precision buffer to be able to drive the guard appropriately. Figure 2-4 illustrates a sample topology.

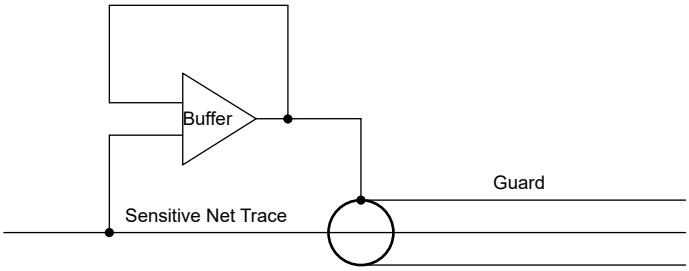

Figure 2-4. Guard Generation Circuit

This topology is recommended to be designed with a precision buffer to reduce any extra leakage currents emanating from the op-amp itself and to ensure the closest guard possible. Table 2-1 shows some recommended op-amps to use for this application.

Table 2-1. Recommended Guard Generation Op-Amps

Device	Voltage Range	Offset Voltage
OPA397	5.5 V	60 uV
OPAx197	36 V	25 µV
OPA593	85 V	10 µV
OPA455	150 V	3.4 mV

3 How Can Leakage Affect the Performance of a Precision Application?

Leakage currents introduced from multiplexers can contribute to undesirable results when implemented into a high precision application. Table 3-1 shows that there are two different multiplexers to choose from.

Table 3-1. Multiplexer Performance Comparison

Multiplexer	Leakage Performance (25C/125C)	On-Resistance (25C/125C)
TMUX1108	3pA/950pA	2.5 Ω/4.9 Ω
TMUX1308	1nA/800nA	75 Ω/270 Ω

These devices will have leakage and resistance components to them that can have an influence on the application and contribute error if proper guarding precautions are not put into place. The error that is introduced from these leakage currents is equivalent to the approximate amount shown in Equation 1.

$$V_{ERROR} = (R_{ON} + R_{SOURCE}) \times I_{LEAK} \quad (1)$$

To further clarify, the model of a multiplexer's ON leakage current is shown in Figure 3-1.

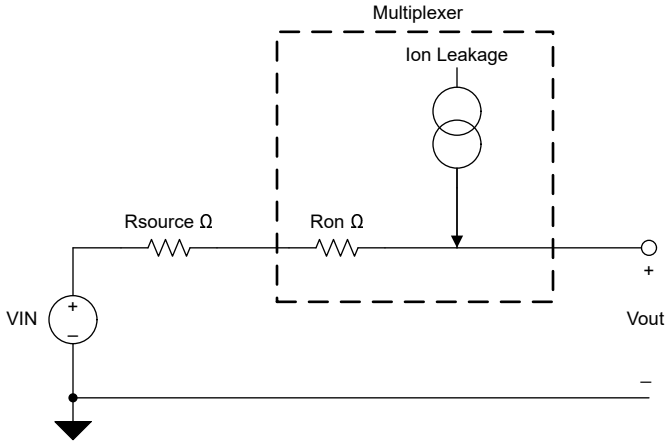

Figure 3-1. ON-Leakage for Multiplexers

When feeding into a high impedance node, the leakage current takes the path of least resistance, which is through the on-resistance and source-resistance path and induce an offset error that affects the measurement at the output. Continuing using the chosen multiplexers above, it is evident that leakage can indeed be significant if proper guarding and device selection is not taken into serious consideration (below is assuming R_{source} is negligible).

Table 3-2. Multiplexer Induced Offset Error

Multiplexer	Leakage Performance (25°C/ 125°C)	On-Resistance (25°C/125°C)	Offset Error (25°C/125°C)
TMUX1108	3 pA/950 pA	2.5 Ω/4.9 Ω	7.5 pV/4.6 nV
TMUX1308	1nA/800 nA	75 Ω/270 Ω	75 nV/216 µV

While this example above showcases how leakage currents can contribute heavily to offset error just based on multiplexer selection, it is important to note that the low leakage performance can only be achieved with a proper layout and guarding implemented.

4 Multiplexer Recommendations for Precision, Low Leakage Applications

While guarding plays a critical role in determining the leakage performance of certain applications, the application needs to start with a very high precision capable device in order to achieve such low levels of leakage. TI offers several different multiplexer families that would be recommended in such applications as shown in Table 4-1.

Table 4-1. Recommended Precision Multiplexer Families

Device	Configuration	Voltage Range	On-Leakage (25°C)	On-Resistance (25°C)
TMUX1108/09	8:1x1/4:1x2	5 V, ±2.5 V	3pA	2.5 Ω
TMUX1111/2/3	1:1x4	5 V	3 pA	2.5 Ω
TMUX1121/2/3	1:1x2	5 V	3 pA	1.9 Ω
TMUX6111/2/3	1:1x4	17 V, ±17 V	10 pA	125 Ω
TMUX6121/2/3	1:1x2	17 V, ±17 V	10 pA	120 Ω
MUX36D08	8:1x2	36 V, ±18 V	10 pA	125 Ω
MUX36S16	16:1x1	36V, ±18 V	10 pA	125 Ω
TMUX7219	2:1x1	44 V, ±22 V	40 pA	2.1 Ω
TMUX7208/09	8:1x1/4:1x2	44 V, ±22 V	40 pA	4 Ω
TMUX7211/2/3	1:1x4	44 V, ±22 V	100 pA	1.7 Ω
TMUX8108/09	8:1x1/4:1x2	100 V, ±50 V	40 pA	38 Ω
TMUX8211/2/3	1:1x4	100 V, ±50 V	10 pA	5 Ω

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