Application Brief

Enabling SPI-Based Flash Memory Expansion by Using Multiplexers

Field programmable gate array (FPGA) based designs need efficient memory storage to have the capacity to run a wide array of applications. Although the FPGA has internal storage, high-performance systems such as servers, Ethernet switches, SSDs, and hardware accelerators may require external memory to meet their minimum memory capacity. This external memory can be volatile or non-volatile, depending on whether the data needs to be stored when power is removed. Non-volatile memory, such as flash memory, is able to preserve data even when it is unpowered, making it ideal to store boot-up code and FPGA configuration data. The FPGA communicates to the external memory via serial peripheral interface (SPI) protocol, routed by a multiplexer (MUX).

Figure 1 shows how a MUX routes the SPI signal to give users multiple ways to access the flash memory, either through the FPGA or an external header. The header allows external access to the flash memory to debug boot-up code and to update other stored firmware.

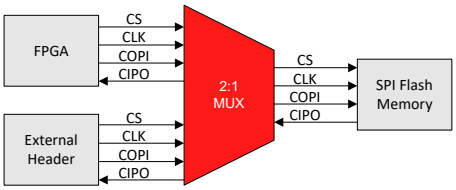

Figure 1. External Access to Flash Memory

Figure 2 shows how the FPGA can access multiple external memories through the use of a MUX for memory expansion. Although SPI protocol allows direct connection from the master to multiple slaves, the MUX is essential in lowering bus capacitance and facilitating connection when there is only one master chip select bit. The bidirectional capability of the multiplexers enables the same MUX to address both use-case scenarios in Figure 1 and Figure 2.

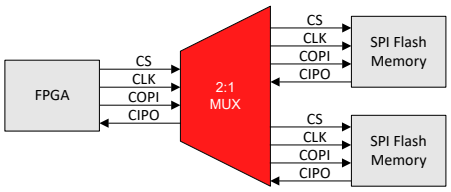

Figure 2. FPGA Access to Multiple Flash Memories

In addition to allowing an alternate path to the flash memory, powered-off protection muxes also provide isolation between the FPGA and external memory, protecting the system from power sequencing issues as shown in Figure 3. To learn more about this application, see Power Sequencing With Powered-off Protection Signal Switches, and for additional information regarding crosstalk and off-isolation, see TI Precision Labs - Switches and Muxes: bandwidth, crosstalk, off-isolation, and THD+Noise.

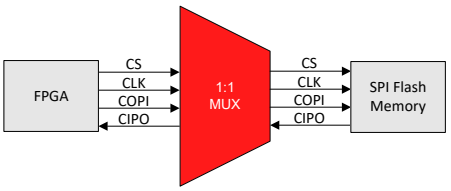

Figure 3. FPGA and External Memory Isolation

SPI Protocol

SPI is a synchronous serial interface used by FPGAs and MCUs to communicate to a variety of peripherals such as flash memories, sensors, ADCs, and SD cards over short distances. The SPI bus uses push-pull drivers which support higher clock frequencies (> 75 MHz) with lower power consumption (< 1 mA) compared to open drain drivers which are used for I2C or SMBus. The SPI protocol typically uses four channels (two data lines, one clock signal, and one chip select bit) compared to I2C, which uses two channels (one data lane, and one clock signal). To achieve higher throughput, quad SPI (four data lanes) and octal SPI (eight data lanes) protocols are becoming more prevalent in high-performance systems using external memories. Common uses of quad SPI and octal SPI are in flash memory systems

that implement multiple parallel data lines in the SPI interface rather than a single COPI line and single CIPO line. Quad SPI frequently uses eight total signal lines: one chip select line (CS), one data strobe line (DQS), two differential clock lines (CLK and nCLK), and four data lines (D0, D1, D2, and D3). Octal SPI includes four additional data lines (D4, D5, D6, and D7), resulting in a total of 12 signal lines. Figure 4 shows an example of access to multiple quad SPI flash memories using two 4-channel 2:1 multiplexers.

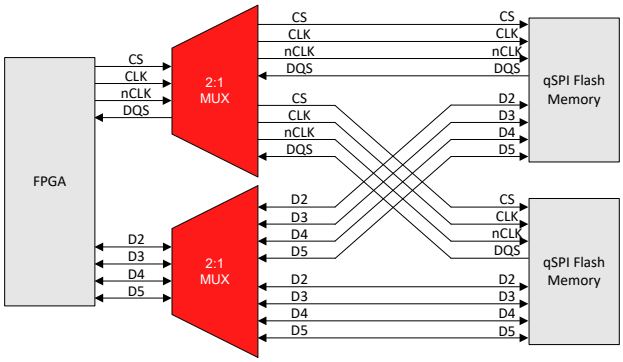

Figure 4. FPGA Access to Multiple Quad SPI Flash Memories

Figure 5 shows an example of access to multiple octal SPI flash memories using two 6-channel 2:1 multiplexers.

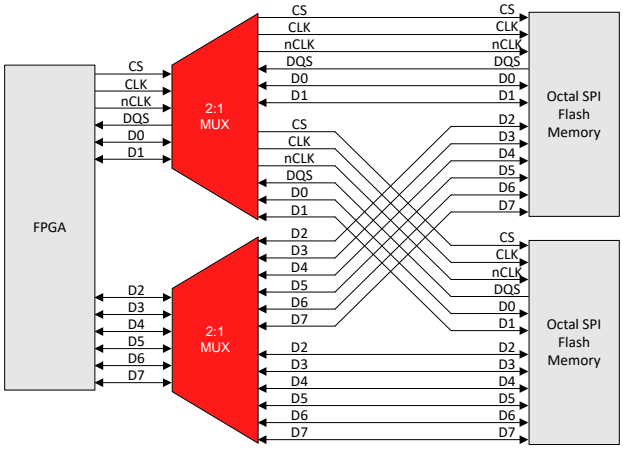

Figure 5. FPGA Access to Multiple Octal SPI Flash Memories

For more information on the SPI bus, see the *SPI bus (Serial Peripheral Interface) hardware overview* section in the *Analog Engineer's Pocket Reference*.

Selecting the Right MUX for SPI Applications

The most critical MUX parameters for SPI digital signaling are voltage, channel count, and bandwidth. To select the proper MUX voltage, simply match the FPGA or MCU I/O voltage with the recommended MUX I/O voltage. The MUX channel count is defined by the SPI protocol: typical SPI protocol requires four channels (two data lines, one clock signal line, and one chip select line), quad SPI requires eight channels, and octal SPI requires twelve channels. The bandwidth is a simple way to account for the MUX parasitic effects on a clock signal due to on-state capacitance (C_{ON}). For most systems, a 50% margin of the maximum fundamental clock frequency is sufficient MUX bandwidth for application. For example, if the maximum SPI clock signal is 100 MHz, a MUX with 1.5 times the bandwidth (150 MHz) is recommended.

Recommended MUX Bandwidth =
Clock Frequency × 1.5

In some cases, designers seeking ideal bandwidth should use a MUX with three times the maximum fundamental clock frequency, though this requirement is generally not needed in application.

For sharp rise and fall times, the TMUX1574 (2 GHz bandwidth) can be used in a SPI application. Figure 6 shows how the TMUX1574 performs passing a 75-MHz SPI clock signal. The top waveform shows the clock signal for reference, and the bottom waveform shows the output clock signal after passing through the MUX. The bottom waveform shows that the MUX has almost no impact on the output SPI clock signal. This is due to the low C_{ON} that allow the 75-MHz clock signal to pass with almost no distortion. Using MUXes with lower C_{ON} results in higher bandwidth which can be critical in systems where board layout or connectors add extra capacitance.

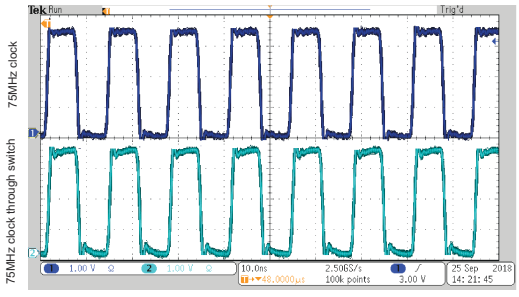

Figure 6. 75-MHz Clock Passing Through TMUX1574

TI Solutions for SPI MUXes

In high-performance systems, FPGAs and MCUs may require external memory for expanded storage. This external memory can be non-volatile, such as flash memory, allowing data to be stored when power is lost. This functionality makes flash memories ideal to store boot-up code, FPGA configuration data, and media files. FPGAs and MCUs communicate to these flash memories via SPI protocol routed by a MUX. This MUX gives users multiple ways to access the flash memory, all while protecting the FPGA and MCU during power sequencing with powered-off protection. Additionally, devices with 1.8 V logic compatibility eliminate the need for external voltage translation when a processor on a 1.8-V rail is controlling a MUX operating on a 3.3-V or 5-V rail. Choosing the right MUX for your application will depend on the SPI protocol, signal voltage, and bandwidth requirements. To help support a wide variety of SPI applications, the TI portfolio of high-bandwidth MUXes supports a wide range of signal voltages for ideal SPI performance.

Table 1. SPI Multiplexer Recommendations

Device	Configuration	Key Features
TMUX1574	2:1, 4-channel	2-GHz Bandwidth, Low C_{ON} (7.5 pF), Low R_{ON} (2 Ω), Powered-off protection, 1.8-V Logic Compatible
TMUX1575	2:1, 4-channel	1.3 mm × 1.3 mm package, 1.2-V compatible control inputs, Powered-off protection, Low C_{ON} (10 pF), Low R_{ON} (1.7 Ω), 1.8-GHz Bandwidth
TMUX1511	1:1, 4-channel	3-GHz Bandwidth, Low C_{ON} (3.3 pF), Low R_{ON} (2 Ω), Powered-off protection, 1.8-V Logic Compatible
TS3A27518E	2:1, 6-channel	240-MHz Bandwidth, Low R_{ON} (4.4 Ω), Powered-off protection, 1.8-V Logic Compatible

References

- Texas Instruments, *Analog Engineer's Pocket Reference Guide*
- Texas Instruments, *Eliminate Power Sequencing With Powered-Off Protection Signal Switches*
- Texas Instruments, *Improve Stability Issues With Low CON Multiplexers*
- Texas Instruments, 1.8 V Logic for Muxes and Signal

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265