Application Report
SCDA012A–June 2009–Revised July 2009

Differential Passive Signal Switch on Computing

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ABSTRACT

This application report describes multiplexing applications for differential bus signals and how to use Texas Instruments high-speed passive-switch products (TS3DV416, TS3DV520, TS3DV520E, TS3DV421, and others on the product roadmap such as TS3DSxxx and TS2DSxxxx) with various bandwidths and data rates. This application report describes the components that make up the system applications, including both the transmitter and receiver sides.

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1 General Description

Differential bus signaling is a new technology that addresses the needs of today's high-performance data transmission applications, and it is therefore becoming an important I/O bus.

Numerous terms and units are used to quantify the ability of data transmission circuit to move data from one place to another. At the physical layer (electrical and mechanical), data signaling rate, data transfer rate, jitter, and skew are most often specified. The following sections provide the basic definition of differential signaling and demonstrate the use of a high-speed passive switch in several differential bus applications.

2 Fundamental of Differential Signal Operation

High-speed data-transfer rates are necessary in video, Ethernet, memory, and data communications equipment. In the past, the processors and controllers used TTL/CMOS I/Os from 8-bit width increasing to 16-bit, 32-bit, and 64-bit width with higher clock frequencies and data-transfer rates. These incremental changes have limitations caused by board space, EMI, noise, and design difficulties.

Differential signal I/O is gaining popularity in computing platforms, because it can offer faster data-transfer rates, lower power consumption, and lower voltage. Digital signal I/O is also a relatively well-established standard specification from standard work groups.

The differential signal uses two wires for each electrical path, providing high immunity to noise and crosstalk. The signals transmitted are a positive signal on one wire and a negative signal on the other. The receiving end derives the signal from the difference between the two wires. The technique can be used for both digital and analog signals, such as the audio and digital signals of RS-422, RS-485, Ethernet, PCI Express (PCIe), USB, DVI, HDMI, LVDS, and DVI.

The two major signaling systems are high-voltage differential signaling and low-voltage differential signaling.

High-voltage differential signaling is a generic term that describes a variety of systems. In computer electronics, "high voltage" is normally considered 5 V or higher.

Low-voltage differential signaling (LVDS) is an electrical signaling system that can run at very high speeds over inexpensive twisted-pair copper cables. It was introduced in 1994 and has since become very popular in computers, where it forms part of very high-speed networks and other computer buses.

3 Low-Voltage Differential Signaling

Differential technology allows products to provide high data rates that range from hundreds of megabits per second to 2 Gbps, 5 Gbps, or even faster. With the various data rates required in different equipment and applications, a number of products and devices are defined by standard work groups.

One of the differential signaling technologies is known as LVDS-EIA/TIA644, and it is a signaling method used for high-speed transmission of binary data over copper wires. The benefits of balanced data transmission begin to outweigh the costs over single-ended techniques when signal transition times approach 10 ns.

The LVDS working group defines driver and receiver electrical characteristics to ensure that LVDS becomes a multipurpose interface standard. It does not define protocol, interconnect, or connector details, because these details are application specific. Therefore, each application that uses LVDS should also reference the appropriate protocol and interconnect standards.

The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with typical offset voltage of 1.2 V relative to ground (see Figure 1).The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.5 V to 2.35 V. The receiver has a sensitivity level of ±100 mV. The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver.

Because the standard does not specify power-supply voltage, and the driver output characteristics are independent of power supply, the supply voltage may be 5 V, 3.3 V, or even lower.

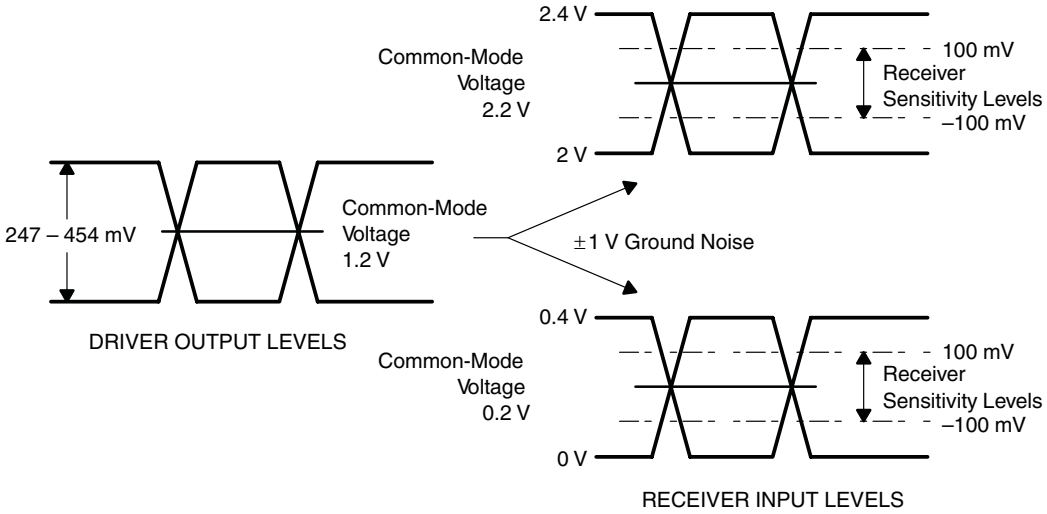


Figure 1. Driver and Receiver Electrical Characteristics

The I/O buses described below use differential signaling technology with defined data rates and required channels. Each new standard bus structure has its own protocols, interconnections, connectors, and voltage swing.

LVDS bus structure can be ac-coupled or dc-coupled. AC coupling adds capacitance on the transmission line and allows both transmitter and receiver to operate at dc voltage levels that are optimal. AC coupling shifts the common voltage ±200 mV. Most ac coupling is done on the transmitter side, and placing the capacitor close to the transmitter side is recommended.

In higher-speed applications, ac coupling is recommended only for dc-balanced signals. AC coupling generates baseline wander in high-speed serial data transmissions that are not dc balanced.

Figure 2 shows an example of V_{OH} and V_{OL} changes after ac coupling.

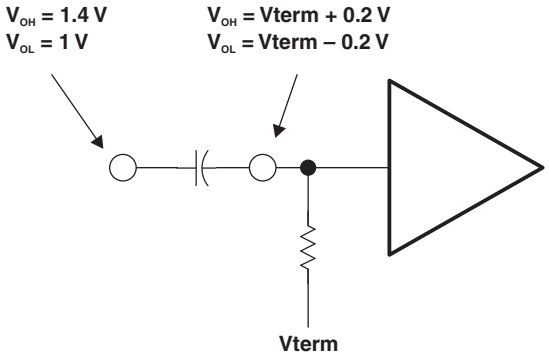


Figure 2. V_{OH} and V_{OL} Changes After AC Coupling

The following are some LVDS protocols that are defined for convenient development of related components and programming at fixed high-speed data transmission rates.

- HyperTransport (since 2001)
- FireWire (IEE1394-1995)
- Serial ATA (since 2004)
- RapidIO (since 2004)
- PCI Express known as PCI-E or PCI-e (2004 by Intel)
- Flat Panel Display Interface (since 1996 by VESA)
- OpenLDI (since 1999 by National)
- Gigabit Ethernet (IEEE 802.3-2005)

3.1 Flat Panel Display Interface

The panel industry is rapidly accelerating to higher resolution and a greater number of color bits per pixel. Breakthroughs in better color resolution are possible only by increasing the overall data rate from the host to the panel.

Digital image processing enhances the overall viewing by using LVDS signaling to transmit and receive the high-speed video data stream.

With the growth of digital displays, many IP cores have been created to support LVDS buses, and they have been embedded in applications such as graphic video controllers, application processors, and display devices for notebooks, motherboards, set top boxes, DVD players, and other audio/video equipment.

VESA (Video Electronics Standards Association) defines the standardization of selected electrical interface requirements for LCD panels intended for notebook computers, LCD display monitors, and other video interfaces, which allows the designers of the IP cores, LVDS transmitters, and receivers to follow the defined electrical specifications.

The LVDS transmitter is a device that converts LVCMOS/LVTTL data into LVDS channels at transmit clock speeds. LVDS transmission data rate can be calculated by number of bits and clock frequency. For example 6 bits $\times$ 65 MHz = 390 Mbps per pair.

The LVDS receiver is a device that converts the LVDS signal to LVCMOS/LVTTL. Both LVDS transmitters and receivers must comply with the same LVDS specification to communicate.

The specified electrical characteristics of LVDS transmitters and receivers are shown in Table 1 and Table 2 with key related parameter of I/O behaviors.

The LVDS transmitter in notebooks, set-top boxes, ultra-mobile PCs, mobile processors, and portable media player processors is used as an internal video output for panel connection. The LVDS receiver in LCD monitors and TV displays is used as a video input for scalar IC and TFT LCD panel display.

Table 1. LVDS Transmitter Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OD}	Normal differential output voltage	R_L = 100 Ω	250		450	mV
	Reduced differential output voltage		100		300	
ΔV_{OD}	Changes in V_{OD} between complimentary output states				35	mV
V_{OS}	Offset voltage		1.125	1.2	1.375	V
ΔV_{OS}	Changes in V_{OS} between complimentary output states				35	mV
I_{OS}	Output short-circuit current				24	mA
I_{OZ}	High-impedance output current				10	µA
V_{ID}	Differential input voltage		0.1		0.5	V

Table 2. LVDS Receiver Electrical Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V		100	mV
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V	–100		mV
I_{IN}	Input current			±10	µA
V_{ID}	Differential input voltage		100		mV
V_{CM}	Common-mode input voltage	V_{DD} = 3.3 V	V_{ID} / 2	2.4 – V_{ID} / 2	V
		V_{DD} = 2.5 V	V_{ID} / 2	V_{DD} – 0.4 – V_{ID} / 2	

LVDS is a standard interface between the host and the LCD panel module, which would be either FPD-Link or LDI interface. The LVDS receiver function is typically integrated into the panel timing controller and three or four data pairs per primary color (red, green, and blue) and clock, depending on depth color supported (6-bit or 8-bit color) .

The Standard Panel Working Group (SPWG) and VESA established a set of panels with dimensions and interface characteristics that allow both notebook and LCD supplier industries to manage design more easily.

Today the main standard buses for LCD panel module connections use 20 pins, 30 pins, 40 pins, or 50 pins, with varying numbers of channels and sideband control signals. Figure 3 shows the detailed interface connection pin assignments.

The 20-pin panel interface is intended for 12.1", 12.1"W, and 13.3"W display interfaces with four main LVDS channels and a pair for the I^2C display data channel (DDC). The 30-pin panel interface is intended for 13.3", 14.1", 14.1"W, 15", 15.4"W, and 17"W panel sizes with eight LVDS channels and a pair for the I^2C DDC.

The 30-pin and 40-pin interfaces are intended to achieve higher resolution and require 10 LVDS channels and a pair for I^2C DDC.

6-bit and 8-bit links are a feature of each LVDS channel (two wires), and the transmitter converts the 6 bits of TTL/CMOS data to each LVDS pair for transmission, and the receiver converts the LVDS signals back into the 6 bits of TTL/CMOS data at the receiver side (see Figure 3).

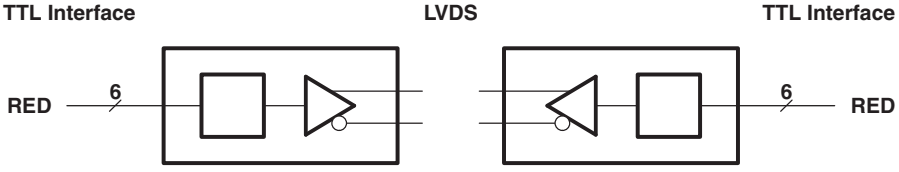


Figure 3. LVDS-TTL Conversion

Table 3. LCD Panel Signal Interface Connector Pinout

Pin No.	6-Bit Single Link	6-Bit Dual Link	8-Bit Link	8-Bit Link
1	GND	GND	GND	GND
2	3.3V	3.3V	GND	GND
3	3.3V	3.3V	3.3V	3.3V
4	3.3V	3.3V	3.3V	3.3V
5	NC	NC	3.3V	3.3V
6	SCL	SCL	SCL	3.3V
7	SDA	SDA	SDA	3.3V
8	RinX0-	RinXO0-	RinXO0-	SCL
9	RinX0+	RinXO0+	RinXO0+	SDA
10	GND	GND	RinXO1-	RinXO0-
11	RinX1-	RinXO1-	RinXO1+	RinXO0+
12	RinX1+	RinXO1+	RinXO2-	GND
13	GND	GND	RinXO2+	RinXO1-
14	RinX2-	RinXO2-	CLKO-	RinXO1+
15	RinX2+	RinXO2+	CLKO+	GND
16	GND	GND	GND	RinXO2-
17	CLK-	CLKO-	RinXO3-	RinXO2+
18	CLK+	CLKO+	RinXO3+	GND
19	GND	GND	RinE0-	CLKO-
20	GND	RinE0-	RinE0+	CLKO+
21		RinE0+	RinE1-	GND
22		GND	RinE1+	RinO3-
23		RinE1-	RinE2-	RinO3+
24		RinE1+	RinE2+	GND
25		GND	CLKE-	RinE0-
26		RinE2-	CLKE+	RinE0+
27		RinE2+	GND	GND
28		GND	RinE3-	RinE1-
29		CLKE-	RinE3+	RinE1+
30		CLKE+	NC	GND
31				RinE2-
32				RinE2+
33				GND
34				CLKE-
35				CLKE+
36				GND
37				RinE3-
38				RinE3+
39				GND
40				NC
Channels	4 Pairs	8 Pairs	10 Pairs	10 Pairs

3.2 Embedded Video Controller With LVDS Output

To allow the system to send the display data to the panel module faster, the LVDS transmitter converts the TTL/CMOS (R, G, B) parallel data to serial LVDS signaling. A phase-locked transmit clock is transmitted in parallel with the data stream over another LVDS link. The RGB data can be 6-, 7-, or 8-bit parallel data input to each LVDS pair depending on the specific LVDS transmitter specification and transmitted clock frequency. Figure 4 shows the connection between the host (LVDS transmitter) and the peripheral (LVDS receiver).

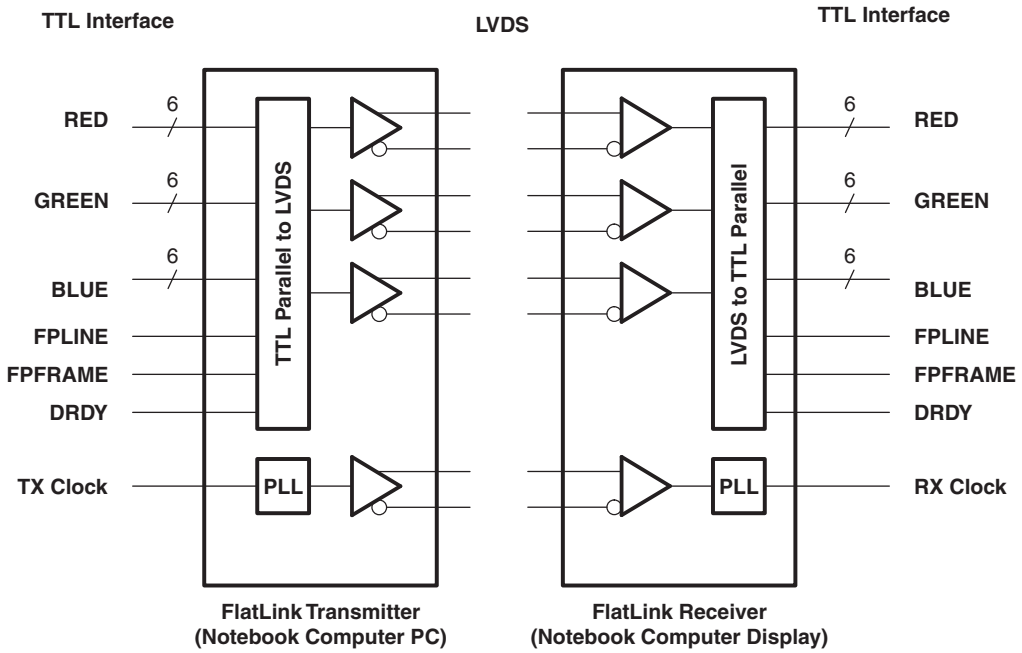


Figure 4. Typical Connection Between LVDS Transmitter and Receiver

3.2.1 Connecting a Single LVDS Source to a Dual LVDS Expansion Multiplexer

The application in Figure 5 shows how to use a passive switch to expand the LVDS transmitter to two LVDS receivers in two different LCD panel modules without a second LVDS transmitter. One example of equipment that might require this system is a PC notebook with two displays—the main display and a second LCD panel located on the front cover for media movie display, checking email, tasks, schedule, weathers, internet, and GPS map viewing without opening the notebook. In this design, the notebook would need a simple high-speed passive switch to expand the LVDS source and select the LCD panel that is currently being used as the display.

The correct differential switch must be selected based on the LCD panel type, the number of LVDS channels, the data rate, and the V_{IO} range.

Figure 5 shows the typical switching route between one LVDS transmitter and two receivers connected to LCD panel modules.

The figure shows how the high-speed passive switch can switch any LVDS signals within its specified data rate and V_{IO} range. Other key characteristics of the switch related to signal integrity and are also important. These high-speed passive switches can be used not only for LCD panel buses and but also for non-LCD panel LVDS bus signaling.

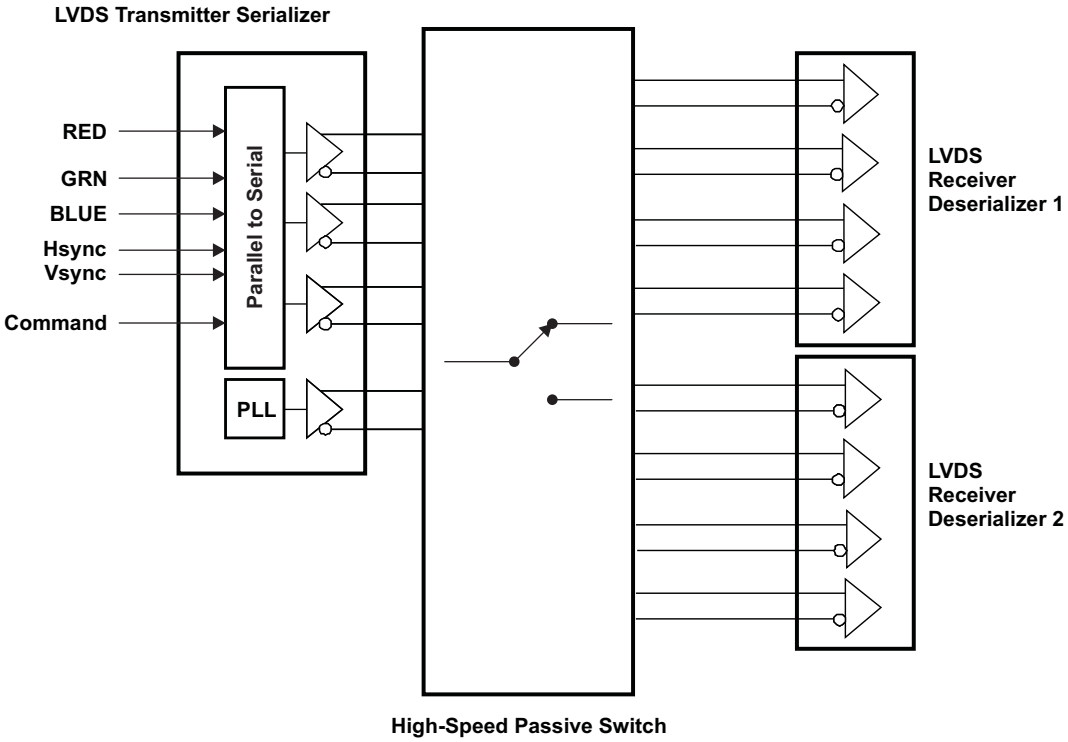


Figure 5. High-Speed Switch as 1:2 Multiplexer to Two LVDS Receivers

3.2.2 Connecting from Two LVDS Sources to a Single Panel Display

Some systems have two video sources (that is, two LVDS transmitters) with a single LCD panel module (the LVDS receiver). Often, the first LVDS transmitter is embedded into the graphic video controller or FPGA, and the second LVDS transmitter is from a second processor or expansion bus (SDVO, PCIe bus) used for high-performance graphics.

The intention of adding two LVDS sources is that the first (embedded) LVDS is a default display for power saving during battery mode, and the second LVDS transmitter is higher performance and, therefore, consumes more power and is used when the notebook is powered by ac.

Figure 6 shows a typical example of switching for two different LVDS transmitters to a single LVDS receiver. All high-speed passive switches allow bidirectional signaling and feature a select control pin that can be set high or low by a system-monitoring circuit to connect the desired LVDS transmitter to the receiver.

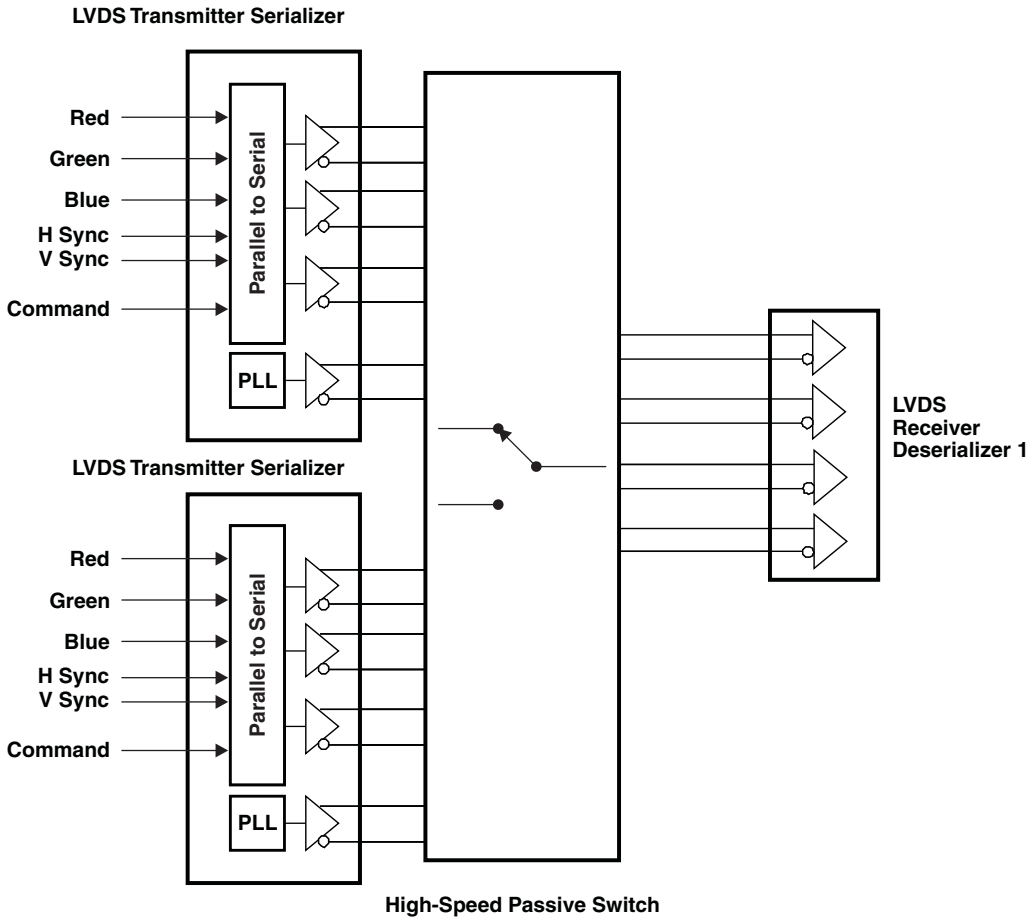


Figure 6. High-Speed Switch as 2:1 Multiplexer to One LVDS Receiver

3.2.3 Multiplexing SDVO and PCI Express (PCIe) Signals

Some integrated video controllers such as Intel GMCH chip support Serial Digital Video Output (SDVO) and multiplex PCIe signals on the same pins for dual functions. SDVO is a proprietary Intel technology introduced with their 9xx-series of motherboard chipsets. SDVO makes it possible to use a 16-lane PCIe slot to add additional video signaling interfaces such as VGA and DVI monitor outputs or SDTV and HDTV television outputs.

Table 4 shows SDVO and PCIe signaling names on the same pin. Figure 7 shows an example of how to use differential switches for 1:2 connection of an SDVO bus and PCIe slot.

The SDVO port is an optional bus for converting to LVDS, DVI, HDMI, or other video type. The PCIe bus is a standard high-speed expansion bus slot that can be used in any peripheral function including video. The passive switch in this application makes two connections from the source for easy implementation of SDVO or PCIe bus.

Table 4. SDVO and PCIe Based Graphic Port Signal Mapping

SDVO Mode	PCIe Mode
SDVOB_RED	PEG_TXP0
SDVOB_RED#	PEG_TXN0
SDVOB_GREEN	PEG_TXP1
SDVOB_GREEN#	PEG_TXN1
SDVOB_BLUE	PEG_TXP2
SDVOB_BLUE#	PEG_TXN2
SDVOB_CLK	PEG_TXP3
SDVOB_CLK#	PEG_TXN3
SDVOC_RED	PEG_TXP4
SDVOC_RED#	PEG_TXN4
SDVOC_GREEN	PEG_TXP5
SDVOC_GREEN#	PEG_TXN5
SDVOC_BLUE	PEG_TXP6
SDVOC_BLUE#	PEG_TXN6
SDVOC_CLK	PEG_TXP7
SDVOC_CLK#	PEG_TXN7
SDVO_TV_CLKIN	PEG_RXP0
SDVO_TV_CLKIN#	PEG_RXN0
SDVO_INT	PEG_RXP1
SDVO_INT#	PEG_RXN1
SDVO_FLD_STALL	PEG_RXP2
SDVO_FLD_STALL#	PEG_RXN2

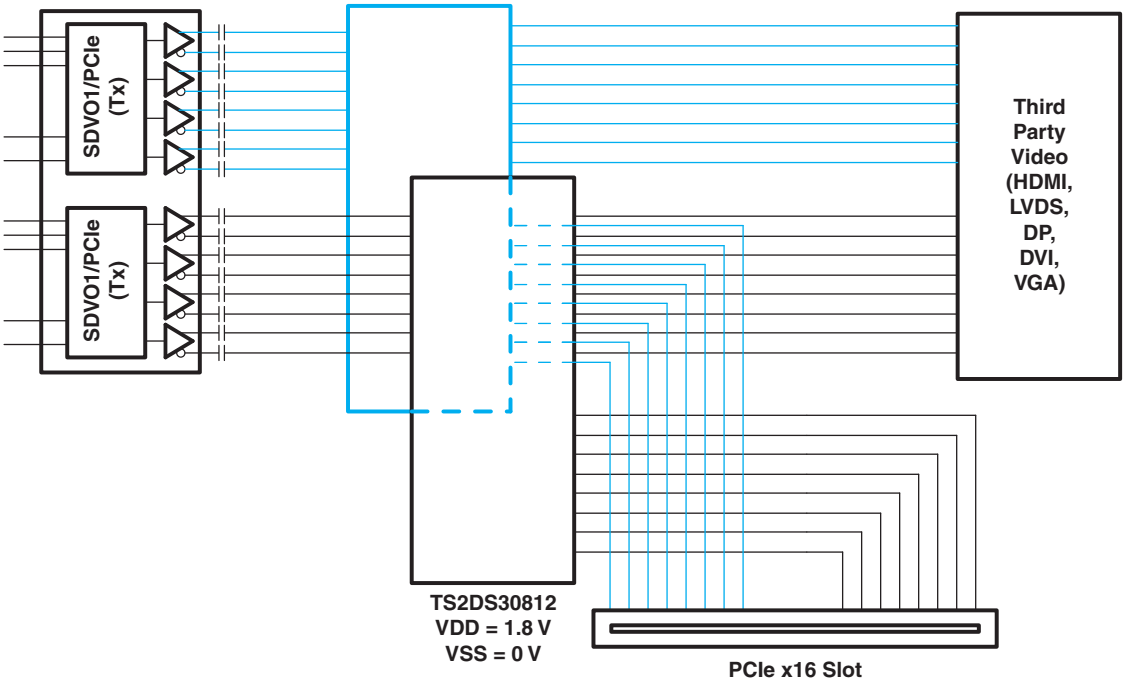


Figure 7. Multiplexing Out to PCIe Slot and HDMI Converter

PCIe Gen I data rate is higher than SDVO at is 2.5 Gbps/pair. TS3DV421 and TS2DS38012 can be used in this application as they support 3.8 Gbps. V_{IO} can be set from 0 V to 1.8 V by connecting the V_{DD} = 1.8 V and V_{SS} = 0 V. Both devices have four channels, and the system may need more devices to multiplex based on the number of PCIe lanes and SDVO channels.

The PCIe Gen II data rate is higher, up to 5 Gbps, and it may require a different high-speed differential switch that is specified for this higher data rate.

3.3 External Video Output Multiplexing

PC monitor applications sometimes use VGA as external video interface, but VGA is limited in its ability to scale to support higher resolutions and color depths. Differential signaling can be used for not only internal LCD panel module interfaces but also for external video interfaces, and can overcome these limitations.

There are many standard digital video output types such as Digital Video Port (DVP) (defined by InfiniteReality), DFP, SGI Open LDI, DVI, HDMI, and DisplayPort, which all use differential signaling with different video encoding and decoding protocols, interconnections, clock or embedded clock, and number of channels, as well as different types of connectors.

A digital display interface is desired by the PC industry and other home audio/video electronics. A digital interface reduces the design complexity when connecting to digital display technologies such as Digital Visual Interface (DVI), High Definition Multimedia Interface (HDMI), and DisplayPort (DP).

The data format used in DVI is based on a panel serial format that uses transition minimized differential signaling (TMDS). Each DVI single link consists of four pairs of differentials (one for each color code of red, blue, and green, and one for a clock signal). DVI Dual Link consists of seven differential pairs to transmit 24 bits per pixel. The clock signal is nearly the same as that of the analog video signal.

HDMI is another interface standard used for audiovisual equipment such as television and home theater as well as LCD PC monitor video interface. HDMI supports standard video formats, enhanced video, and high-definition. It is also backward compatible with DVI. HDMI Type A uses four differential pairs, and Type B uses seven differential pairs.

DisplayPort is an open industrial standard digital display interface under the VESA display system committee. It supports both video and audio digital signaling for the notebook PC video interface. It has five differential pairs—four main link differential pairs carrying the audio/video data and one AUX differential pair that is bidirectional and used for realizing robust plug-n-play for ease of use.

Notebooks, DVD players, portable A/V players, LCD display monitors, and televisions are required to support many types of video interfaces. These systems often require high-speed differential signal multiplexing to switch between video ports, such as from a single video source output to two video output sources using 1:2 multiplexing. The passive switch is an inexpensive solution that can switch the source to two different video output at a high data rate.

DVI and HDMI 1.2a use the same data rate (up to 1.65 Gbps per channel) and compatible TMDS signaling levels. HDMI 1.3 standard increases the link's data rate from 165 MHz to an expected 275 MHz and the data rate up to 3.4 Gbps per channel.

DisplayPort is a royalty-free option that aims to surpass both DVI and HDMI on several fronts. DisplayPort uses the electrical layer of 2.5-Gbps channels, and the bandwidth is up to 10.8 Gbps over four channels. It supports cable lengths of up to 15 m while using lower voltage levels than DVI.

Because HDMI and DP use different signaling levels, an additional component is required for signal translation of DP to TMDS when using both HDMI and DP on the same system.

3.3.1 DVI/HDMI Electrical Characteristic

An illustration of DVI/HDMI using a TMDS differential pair is shown in Figure 8. TMDS technology uses current drive to develop a low-voltage differential signal at the receiver side of the dc-coupled transmission line. The link reference voltage AV_{CC} sets the high voltage level of the differential signals, while the low voltage level is set by the current source of the transmitter and termination resistance at the receiver.

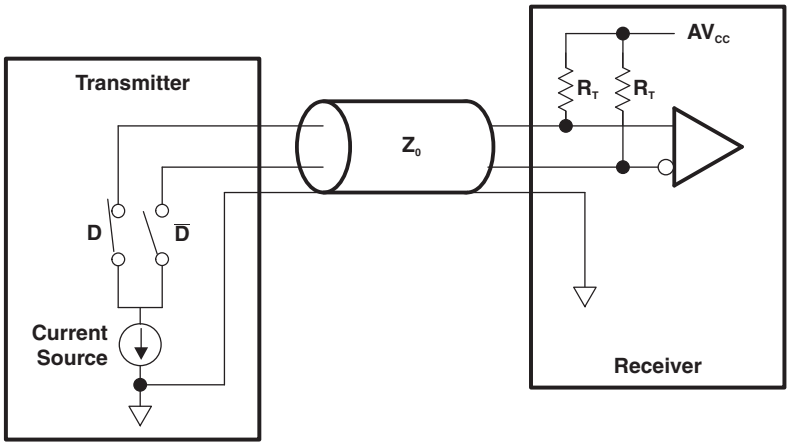


Figure 8. TMDS Differential Pair Transmitter and Receiver

The operating conditions of TMDS interface are specified at 3.3 V ± 5% (see Table 5) and transmitter electrical specifications are dc-coupled TMDS link and single-ended high-level output voltage, V_H is AV_{CC} ±10 mV and low level output voltage, V_L is (AV_{CC} – 600 mV) < V_L < (AV_{CC} – 400 mV) (see Table 5).

Combining the single-ended swing voltage (V_{swing}) specified with the overshoot and undershoots requirements; it is possible to calculate the minimum and maximum high-level voltage (V_H) and low-level voltage (V_L) that allowable on the interface (see Table 6).

As DVI and HDMI TMDS is based on 3.3-V condition, any high-speed passive switch can be used in multiplexing with the feature signal path can pass through within 2.7 V to 3.6 V at defined data rate.

Table 5. Required Operating Conditions

Parameter		Value
AV_{CC}	Termination supply voltage	3.3 V ± 5%
R_T	Termination resistance	50 Ω ± 10%
T_{OP}	Operating temperature	0°C to 70°C

Table 6. Transmitter DC Characteristics

Parameter		Value
V_H	Single-ended high-level output voltage	AV_{CC} ± 10 mV
V_L	Single-ended low-level output voltage	(AV_{CC} – 600 mV) ≤ V_L ≤ (AV_{CC} – 400 mV)
V_{swing}	Single-ended output swing voltage	400 mV ≤ V_{SWING} ≤ 600 mV
V_{OFF}	Single-ended standby (off) output voltage	AV_{CC} ± 10 mV

Calculation of Minimum Opening at Transmitter

$V_{high}(max) = V_{swing}(max) + 15\% \times 2 \times (V_{swing}(max)) = 600 + 180 = 780$ mV

$V_{high}(min) = V_{swing}(min) – 25\% \times 2 \times (V_{swing}(min)) = 400 – 200 = 200$ mV

$V_{low}(max) = V_{swing}(max) – 15\% \times 2 \times (V_{swing}(max)) = –600 – 180 = –780$ mV

$V_{low}(min) = V_{swing}(min) + 25\% \times 2 \times (V_{swing}(min)) = –400 + 200 = –200$ mV

Minimum opening at transmitter = $V_{high}(min) – V_{low}(min) = 400$ mV

3.3.2 Supporting Both DVI and HDMI with a Single Video Source

HDMI builds on the DVI specification. DVI only handles video data and is widely used in LCD monitor displays. HDMI includes audio as well as video data with increased piracy protection in the form of a digital encryption protocol called HDCP and used in both LCD monitor display and LCD TV display.

The DVI 1.0 specification was released by the Digital Display Working Group (DDWG). DVI defines a single link (four pairs) and dual link (seven pairs) transferring only a video digital data. The HDMI transfer both video and audio and there are four versions developed over the years—HDMI 1.0, 1.1, 1.2, and 1.3. Both DVI 1.0 and HDMI 1.2 support the same 1.65-Gbps data rate, and HDMI 1.3 supports up to 3.4 Gbps by increasing the clock frequency.

DVI and HDMI have the same electrical characteristics and the same dc coupling. Both use four pairs of channels transmitting the data and clock. Figure 9 shows the switching route without passive switch.

DVI and HDMI 1.2 are often still used in portable equipment, because it usually does not need high data rates. HDMI 1.3 supports increased data rates, and its requirements must be used to select a higher data rate passive switch if the system is going to support both lower data rate DVI and higher data rate HDMI 1.3.

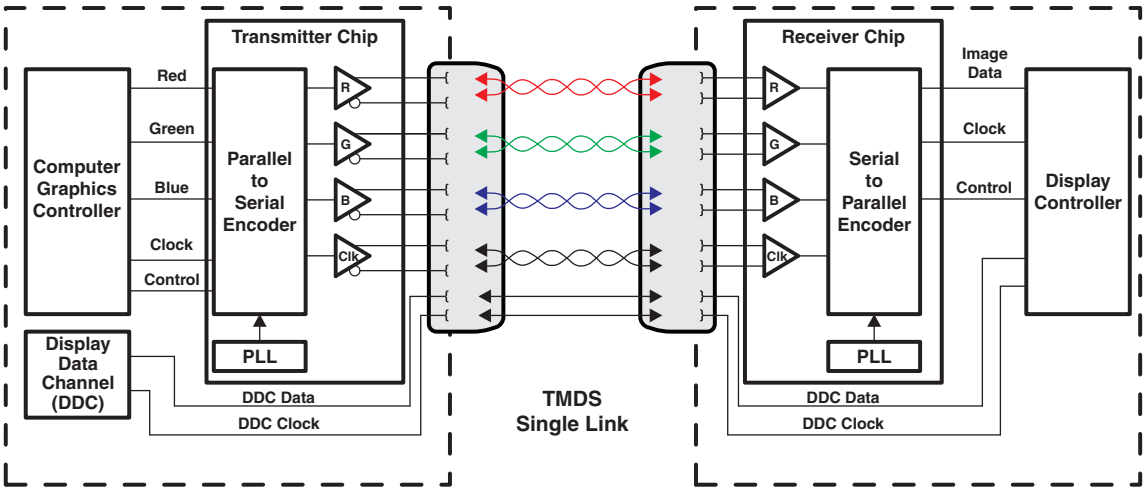


Figure 9. DVI/HDMI Interconnection by Source and Sink

To support both DVI and HDMI 1.2 or HDMI 1.3 video outputs, TS3DV520E is suitable for DVI and HDMI 1.2, and TS3DV421 is recommended for HDMI 1.3.

Supporting the HDMI 1.2 and DVI video outputs, TS3DV520E is recommended as it supports higher than 2 Gbps per pair and is a five-pair switching multiplexer. Four pairs can be used in multiplexing the source of TMDS to both DVI and HDMI 1.2 video connector, and the additional pair can be used for DDC (data and clock). TS3DV520E has 14-kV Human-Body Model ESD protection level, which can save some cost by not requiring an external ESD chip (see Figure 10).

Supporting DVI and HDMI 1.3 (2.25 Gbps or 3.4 Gbps), TS3DV421 is recommended as it can switch signals at 3.8 Gbps/pair. TS3DV421 is high-speed using 1.8-V technology. To meet the HDMI/DVI signaling, it is recommended to connect V_{SS} = 1.5 V and V_{DD} = 3.3 V to allow a signal path from 1.5 V to 3.6 V.

Both DVI and HDMI have four sideband control signals (DDC data and clock, CEC, and HPD), and the solution may need another 4-bit multiplexer (CBT3257C is recommended). Figure 11 shows the complete solution of HDMI 1.3 and DVI video output with a single video source. The CBT3257C is n-channel FET and I/Os can be pulled up to 5 V for DDC and CEC.

DVI dual link (DVI-DL) and HDMI Type B need an additional three pairs to achieve high definition video with higher total data rate. In this application, the main link becomes seven pairs and the DDC channel becomes one pair. TS3DV416 (four pairs) and TS3DV520E (five pairs) are recommended for easy combination using two devices.

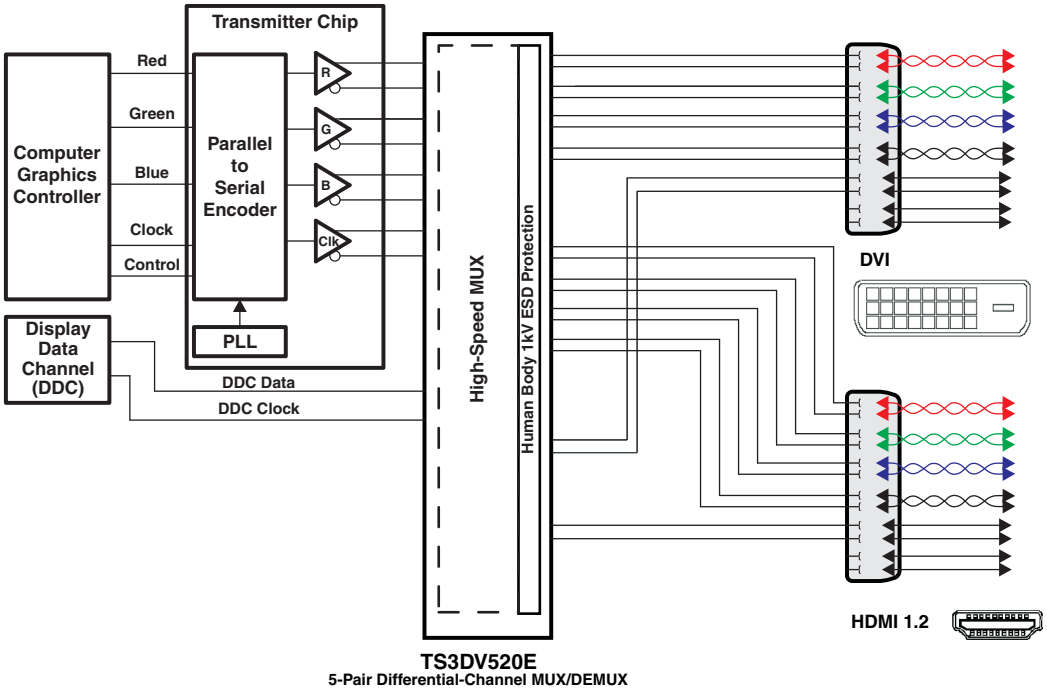


Figure 10. 1:2 Switching MUX to DVI and HDMI 1.2

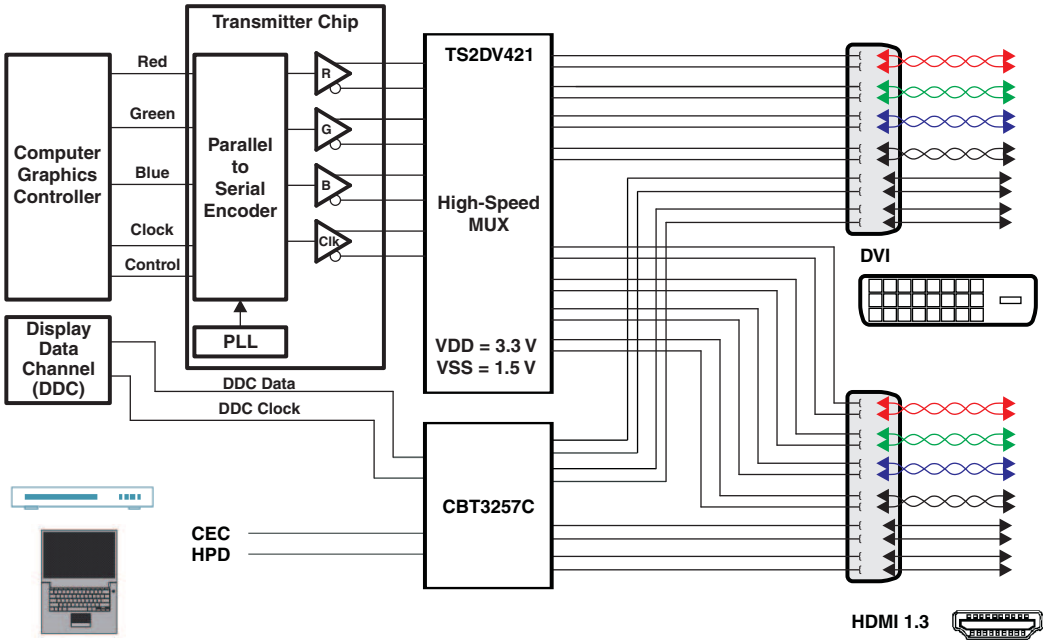


Figure 11. 1:2 Switching MUX to DVI and HDMI 1.3

3.3.3 Supporting DisplayPort and HDMI 1.3 With One Video Source

DisplayPort is defined by VESA, and the standard specifies an open digital communication interface. It is defined in both internal connection for panel bus and external video port for PC, monitor, projector, DVD player, and TV.

The DisplayPort physical layer is similar to the PCIe physical layer, with an ac-coupled voltage-differential interface supporting five channels at 2.7 Gbps per pair. Four pairs are used for data transfer with embedded clock and one pair for the auxiliary channel. Figure 12 shows detailed pin assignment of an external DisplayPort.

DisplayPort is also designed to be used as an internal LCD panel bus by increasing the data rate and configurable channels to support the required data rates of different LCD panels. The initial data rate per pair is defined at 1.6 Gbps or 2.7 Gbps. Table 7 shows DisplayPort Panel Bus pin assignment. Based on the total data rate requirements, it could be a pair, dual pairs or triple pairs.

A notebook with an embedded DisplayPort system needs a TMDS output translator (such as the TI SN75DP129) for HDMI 1.3 signaling. Because the limited DisplayPort Source, it requires a high-speed passive switch to expand DisplayPort outputs into two DisplayPort sources.

TS3DV421 is a 3.8-Gbps data rate four-differential-pairs multiplexer and can expand the DisplayPort source to two DisplayPort sources. One connects to DisplayPort video output connector, and the other connects to SN75DP129, which translates DisplayPort to TMDS output for HDMI video output. Figure 12 shows an example of supporting both DisplayPort and HDMI 1.3 on a PC.

Because DisplayPort is lower voltage signaling from 0 V to 1.8 V, TS3DV421 is recommended by connecting V_{DD} = 1.8 V and V_{SS} = 0 V.

DisplayPort has another auxiliary channel that requires 1-MHz bandwidth, and TS5A23157 can be used in multiplexing this AUX channel. TS5A23157 is a 200-MHz bandwidth analog switch dual SPDT.

The SN75DP129 is a dual-mode DisplayPort input to TMDS output. The TMDS output has a built-in level translator, compliant with DVI 1.0 and HDMI 1.3 standards. The SN75DP129 is specified up to a maximum data rate of 2.5 Gbps, supporting resolutions greater than 1920x1200 or HDTV 12-bit color depth at 1080p.

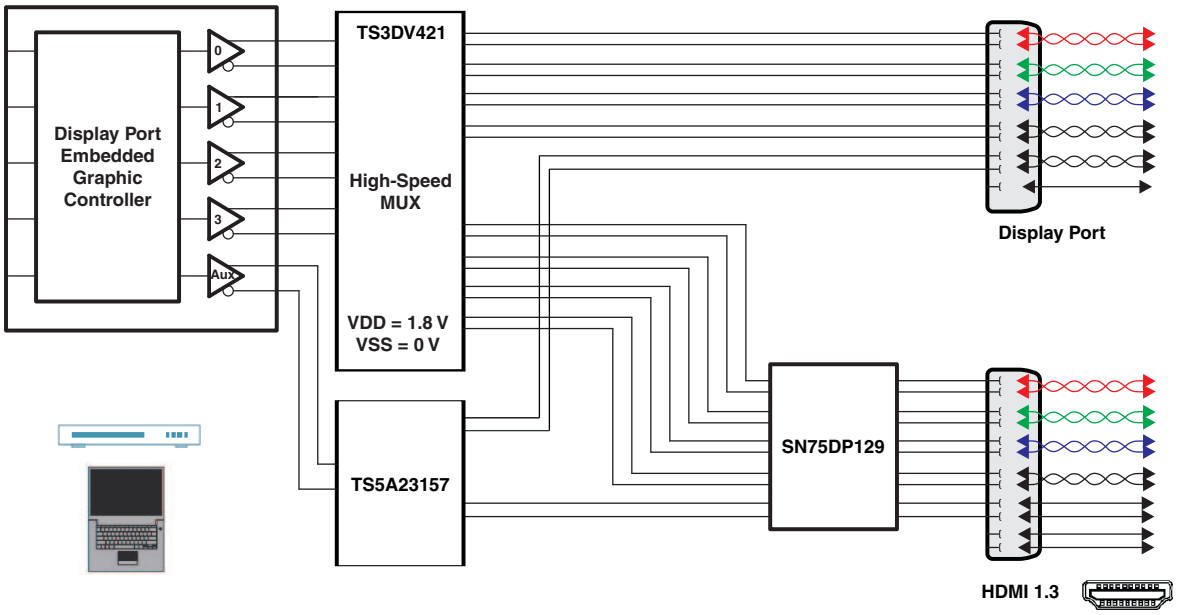


Figure 12. 1:2 Switching MUX to DVI and DP

Table 7. DisplayPort Panel-Side Internal Connector

Panel Standard Pin No.	Pin Name	Pin Definition
Frame		Outer shell
1	Reserved	
2	LCDVCC	Power to LCD panel
3	LCDVCC	
4	LCDVCC	
5	LCDVCC	
6	Ground	Power return (ground)
7	Ground	
8	Ground	
9	Ground	
10	Hot Plug Detect	Hot plug detect, optional
11	Reserved	
12	Reserved	
13	H_GND	High-speed (main link) ground
14	ML_Lane 3(n)	'True' signal - main link
15	ML_Lane 3(p)	'Complement' signal - main link
16	H_GND	High-speed (main link) ground
17	ML_Lane 3(n)	'True' signal - main link
18	ML_Lane 2(p)	'Complement' signal - main link
19	H_GND	High-speed (main link) ground
20	ML_Lane 1(n)	'True' signal - main link
21	ML_Lane 1(p)	'Complement' signal - main link
22	H_GND	High-speed (main link) ground
23	ML_Lane 0(n)	'True' signal - main link
24	ML_Lane 0(p)	'Complement' signal - main link
25	H_GND	High-speed (main link) ground
26	AUX_CH (p)	'True' signal - auxiliary channel
27	AUX_CH (n)	'Complement' signal - auxiliary channel
28	H_GND	High-speed (main link) ground
29	AUX_PWR	3.3-V trickle power
30	Reserved	
Frame		Outer shell

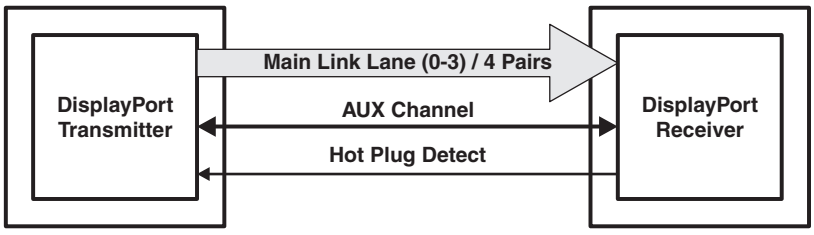


Figure 13. DisplayPort External Connector (Source)

Table 8. DisplayPort External Connector (Source) Pins

Pin No.	Signal Type	Pin Name
1	Out	ML_Lane 0+

Table 8. DisplayPort External Connector (Source) Pins (continued)

Pin No.	Signal Type	Pin Name
2	GND	Ground
3	Out	ML_Lane 0–
4	Out	ML_Lane 1+
5	GND	Ground
6	Out	ML_Lane 1–
7	Out	ML_Lane 2+
8	GND	Ground
9	Out	ML_Lane 2–
10	Out	ML_Lane 3+
11	GND	Ground
12	Out	ML_Lane 3–
13	GND	Ground
14	GND	Ground
15	I/O	AUX_CH+
16	GND	GND
17	I/O	AUX_CH–
18	In	HPD
19	Power Return	Return DP_PWR
20	Power Out	DP_PWR

3.4 External Video Inputs Multiplexing on Sink Link

All differential passive switches have bidirectional signal bypass capability and can be used for 2:1 multiplexing. In LCD monitor/TV applications, the differential switch is used as a video input multiplexer to connect the selected video input channel to connect to internal graphic processing unit.

Figure 14 is a typical design example using TS3DV520E switching between DVI and HDMI 1.2 inputs connected to a TMDS receiver. Because TS3DV520E offers high ESD protection on the connector sides (up to 14-kV HBM), it may not require an external ESD protection chip.

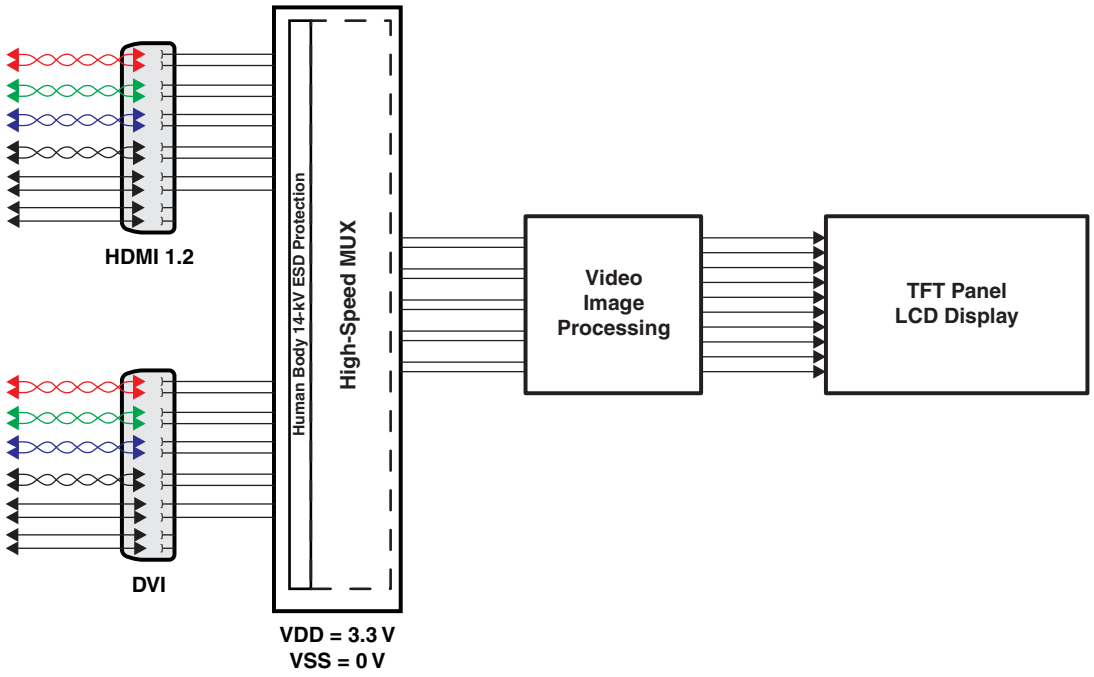


Figure 14. Multiplexing Dual Video Input Source (TS3DV520E)

If the system uses HDMI 1.3 input, TS3DV421 and CBT3257C are recommended—the TS3DV421 to switch the high-speed main links and the SN74CBT3257C to switch the other four signals of DDC data and clock, CEC, and HPD. The SN74CBT3257C I/O can be pulled up to 5 V to meet the HDMI requirements. Figure 15 is an example of using both TS3DV421/TS2DS30812 and SN74CBT3257C to multiplex the two types of DVI video input and HDMI inputs to a video controller TMDS receiver.

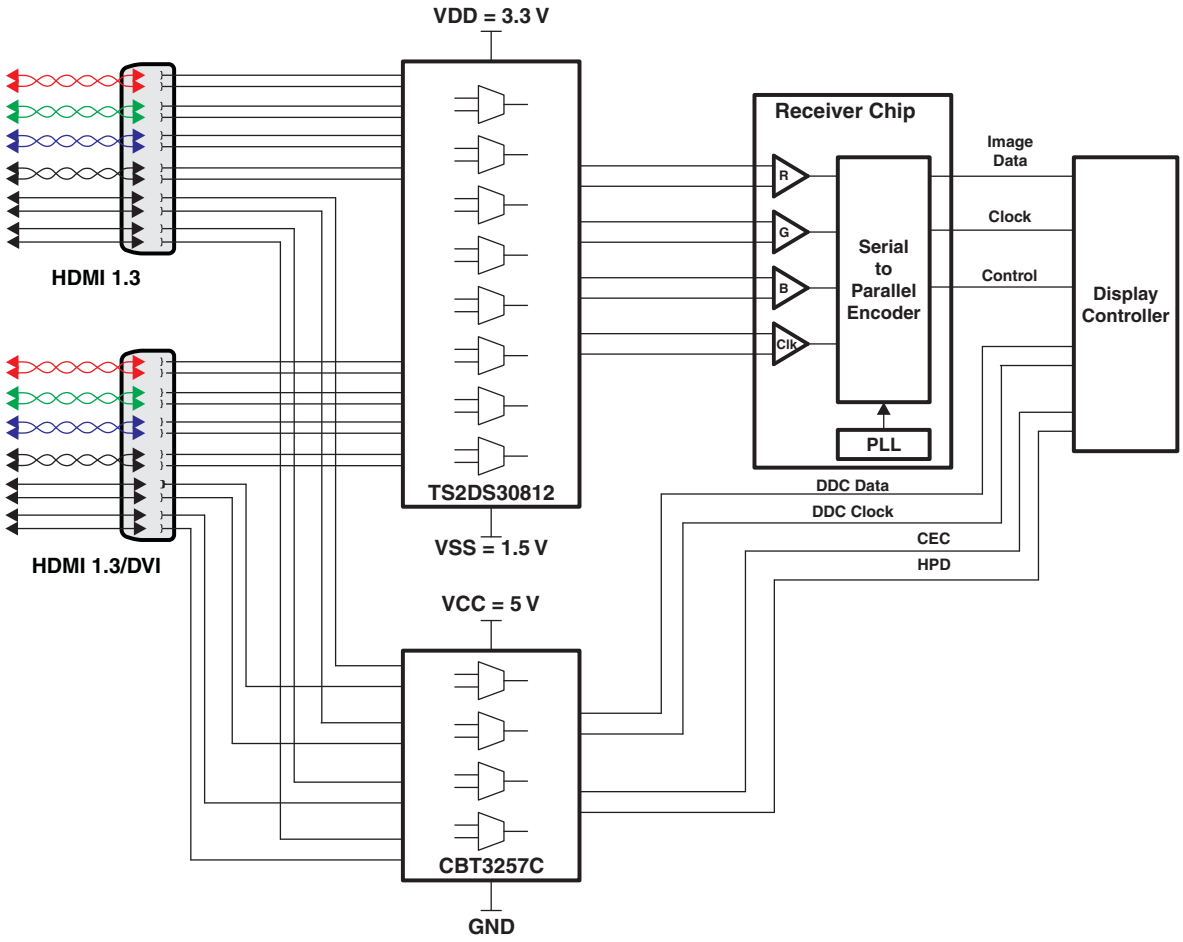


Figure 15. Multiplexing High Bandwidth HDMI 1.3a

3.4.1 Selecting the Right High-Speed Differential Switch

LCD displays such as monitors and TVs support multiple video input types for user convenience. Most of the LCD display controllers support a single video decoder to achieve the effective cost. Differential passive switches are inexpensive solution for video input multiplexing to support an LCD display with more video input types.

Both DVI 1.0 and HDMI 1.2a support a data rate of 1.65 Gbps, and the TS3DV520E, TS3DS20812 or TS3DV416 are recommended for their low cost and ease of design.

If the video input is a dual link, it needs a 10-pair differential signal switch and it may require two devices of TS3DV520E or TS3DS31012E.

LCD TV requires the higher bandwidth HDMI 1.3a and more HDMI video inputs to connect a DVD player, notebook PC, digital camera, or other audio/video equipment. TS2DV421 data rate is up to 3.8 Gbps, and it can be used for higher-bandwidth video multiplexing applications.

3.5 LCD Display Trend in Portable Equipment

Mobile phones have become multifunctional and are no longer simple communication appliances. An advanced mobile phone may be an MP3 player, digital camera, PDA, media player, GPS receiver, portable TV, and computer. The mobile phone's display screen plays an important role in supporting those functions.

One area where the display devices need to upgrade panel response and display performance is to

support video streaming. To achieve faster video streaming, mobile processors and their peripherals are moving away from a parallel TTL/CMOS interface to support a differential serial bus interface. A new mobile video interface uses LVDS signaling, and the initial data rate is about 200 Mbps per channel in both directions with maximum 20-cm cable length. Faster data transfer can be implemented by increasing number of channels (see Figure 16).

MDDI and MIPI are differential signaling interfaces for a mobile display bus with lower power consumption and lower voltage operation, compared to a TTL/CMOS display bus. Table 9 shows a differential bus between the display controller and the display driver. This system can be simplified by a portable processor with an embedded differential bus for the display controller, and a display driver with an embedded differential receiver.

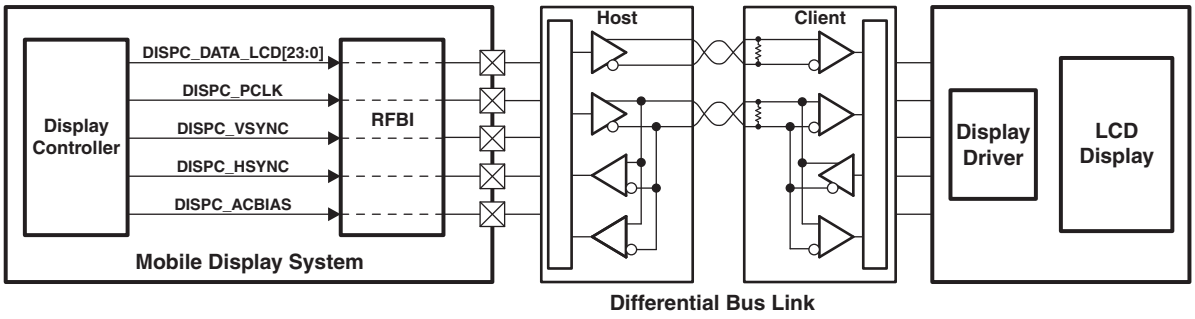


Figure 16. Mobile Phone Differential Bus for Panel Display

Table 9. MDDI Interface Connector Pinout

Pin No.	Signal Type	Description
1	Host_Pwr	200 mA (3.2 V to 4.3 V)
2	Host_Gnd	Ground
3	MDDI_Stb+	Differential signal
4	MDDI_Stb-	Differential signal
5	MDDI_Data0+	Differential signal
6	MDDI_Data0-	Differential signal
7	MDDI_Data1+	Differential signal
8	MDDI_Data1-	Differential signal
9	MDDI_Data2+	Differential signal
10	MDDI_Data2-	Differential signal
11	MDDI_Data3+	Differential signal
12	MDDI_Data3-	Differential signal
13	MDDI_DataPwr4+	Power
14	MDDI_DataPwr4-	Power
15	MDDI_DataPwr5+	Power
16	MDDI_DataPwr5-	Power
17	MDDI_DataPwr6+	Power
18	MDDI_DataPwr6-	Power
19	MDDI_DataPwr7+	Power
20	MDDI_DataPwr7-	Power

3.5.1 Mobile Phone Display

The new LVDS panel bus interface was implemented on the mobile phone for high-performance display for TV, game, and movie player. Some phones also support cradle docking with an external display and may need a passive switch to select between the internal display bus and the cradle I/O connector.

The current defined data rate is 200 Mbps per channel maximum, and TS3V340 is a 500-MHz high-speed

digital switch supporting a data rate up to 1 Gbps per pair. It may be used on a lower data rate differential bus. TS3V340 can operate at 2.5 V or 3.3 V, and the V_{IO} range is from 0 V to 3.6 V (2.5-V V_{CC}) or 0 V to 5 V (3.3-V V_{CC}). The signal output voltage (V_{OUT}) is equal to the voltage on the signal inputs (V_{IN}). TS3V340 I/O rail-to-rail feature enables switching any type of LVDS signaling within the defined data rate specified in the data sheet.

Figure 17 is a potential application of mobile connecting to internal display bus and cradle docking for external display.

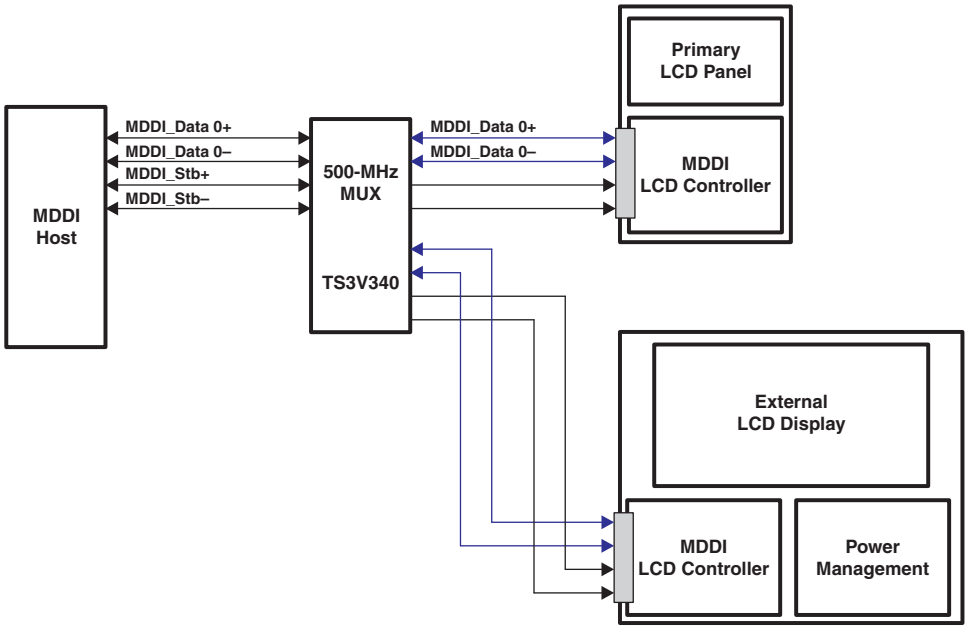


Figure 17. Multiplexing Host_MDDI Transmitter

3.6 PCI Express (PCIe) Signaling

PCIe is a standard local I/O bus for a wide variety of computing platforms including desktop, server and communication, workstation, and embedded devices. PCIe is a multi-drop parallel bus topology containing a hot bridge and several end points (the I/O devices) (see Figure 18).

The fundamental PCIe link consists of two low-voltage differential driven pairs of signals: a transmit pair and a receive pair as shown in Figure 18. A data clock is embedded using the 8b/10b encoding scheme to achieve a very high data rate—PCIe Gen 1 supports a 2.5-Gbps transfer rate, and PCIe Gen 2 supports a 5-Gbps transfer rate.

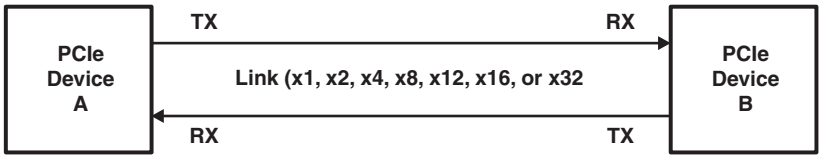


Figure 18. PCI-Express Link (Transmit and Receive Pairs)

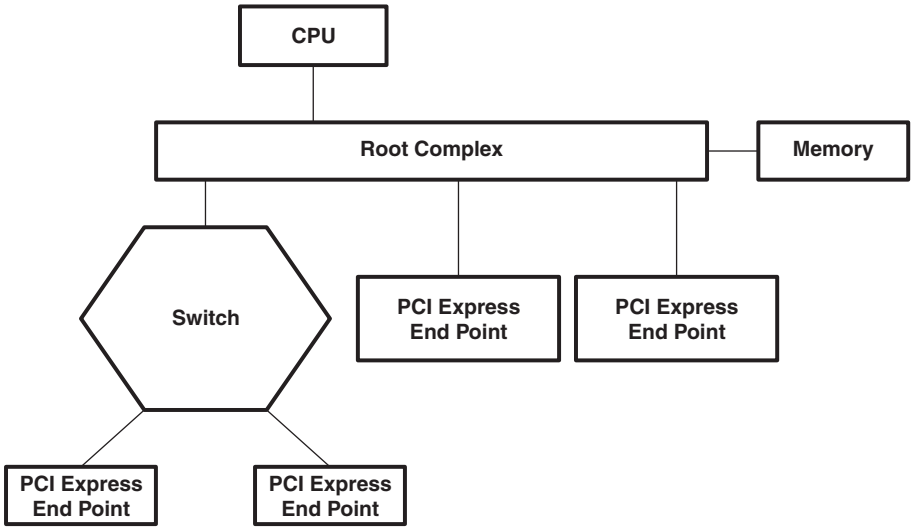
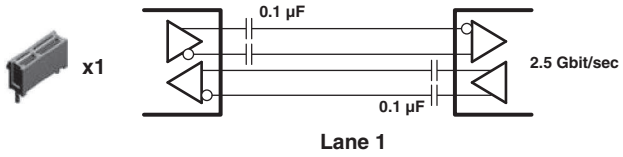


Figure 19. PCI Express System Topology

A PCIe bus can be configured as lanes of x1, x4, x8, and x16. Each PCIe lane contains two pairs of wires—one to send and one to receive, as shown in Figure 20. TI offers several product types of PCIe bridge, end points, physical layers, packet switches, and PCIe signal switches. A PCIe signal switch is a high-speed passive switch that supports both transmit and receive.



Lanes	Single Direction	Dual Direction	No. of Wires
x1	2.5 Gbps	5 Gbps	4
x4	10 Gbps	20 Gbps	16
x8	20 Gbps	40 Gbps	32
x16	40 Gbps	80 Gbps	64

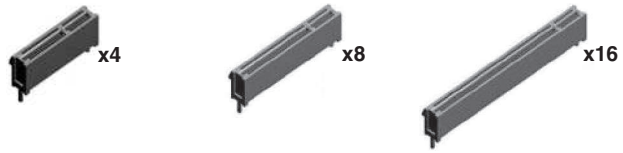


Figure 20. PCI Express Lane Bus Structure

TS2PCIE2212 and TS2PCIE412 are PCIe Gen I high-speed passive switch multiplexers/demultiplexers (MUX/DEMUX) supporting 2.5-Gbps bandwidth and allowing expansion of the PCIe lanes from the root complex to end points dynamically using the select control pin to assign the active PCIe slot.

TS2PCIE2212 is a four PCIe differential signal MUX/DEMUX with bypass switch (see Figure 21) and can be used for either single direction (on transmitter or receiver side) or dual direction.

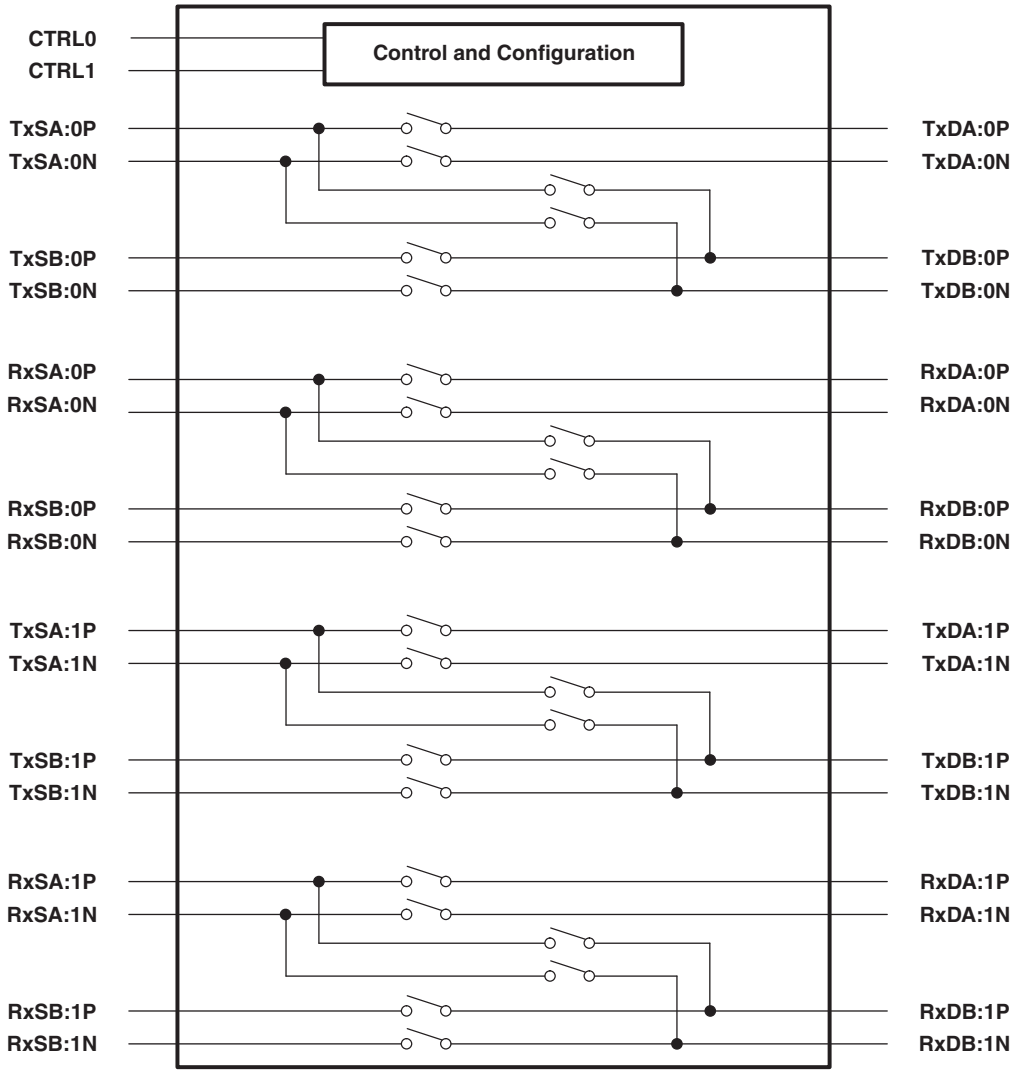


Figure 21. TS2PCIE2212 Switching MUX Diagram

The typical design example shown in Figure 22 is multiplexing dual PCIe root complexes to individual slots. This design allows each slot to connect to either the south bridge or the north bridge root complex.

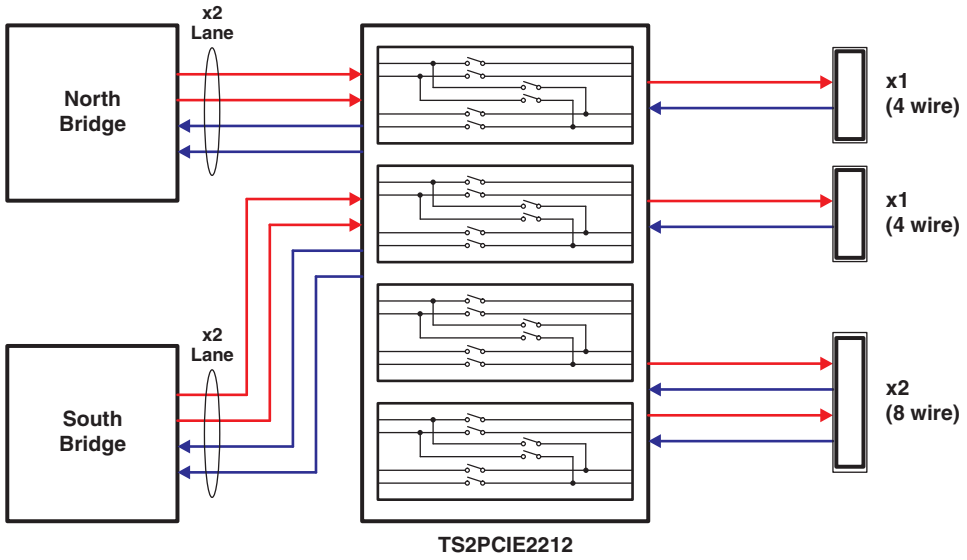


Figure 22. PCI Express Port and Multiplexers

TS2PCIE412 is another differential switch optimized for PCIe signaling. It has four pairs of signal for the PCIe signal multiplexer and it is used in the PC north bridge with embedded dual functions of SDVO and PCIe signals on the same pins. In this application, TS2PCIE412 multiplexes the shared input bus out to separate SDVO and PCIe buses connected to other chips or slots.

Figure 23 shows an example of interconnection with TS2PCIE412, with one output connecting SDVO to an HDMI converter and the other output connecting to a PCIe slot for possible external graphic card to upgrade the video output performance. Depending on the number of lanes, it may require up to four TS2PCIE412 devices to support a PCIe x16 slot.

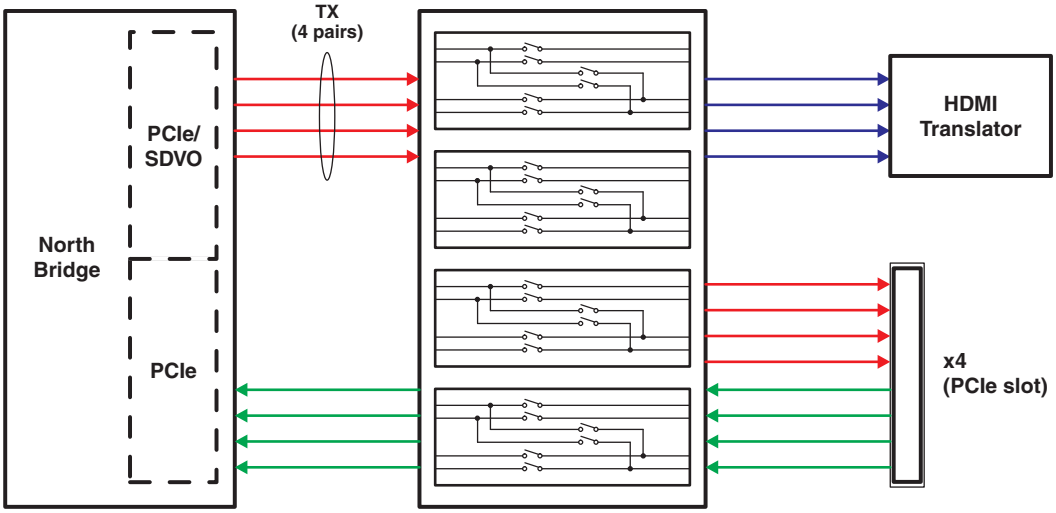


Figure 23. Multiplexing SDVO and PCI Express Slot

Figure 24 show another interconnection from root PCIe to expand the different type of PCIe Connector by x1, x2, or x4.

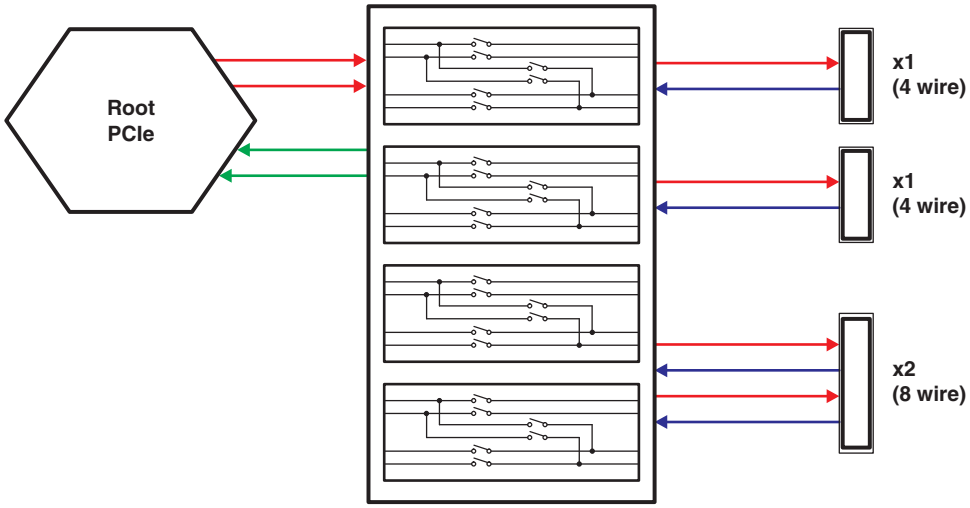


Figure 24. PCI Express Bus Expansion MUX

Because TS2PCIE412 is capable of passing high-speed differential signals, it can be used in non-PCIe application (for example, in a DisplayPort application) within the defined data rate and voltage swing range.

3.7 TS3DV416, TS3DV520E, TS3DV20812

The switches of this family are high-speed NMOS with a low and flat r_{ON}. The flat r_{ON} is achieved by an internal charge-pump circuit that generates a voltage up to 7 V at the gate of the N-channel pass transistors. As a result, these switches offer 0-V to 5-V rail-to-rail switching capability, which allows differential signal bypassing freely within the V_{IO} range of 0 V to 5 V.

In addition to the low and flat r_{ON} characteristics, this family has low input and output capacitance, making them suitable for differential signaling switching applications. The maximum switching frequency for I/O signals depends on various factors, such as type of load, input-signal magnitude, input-signal edge rates, type of packages, etc.

Figure 25 show the V_O vs V_I characteristics of this switch family at 3.3 V. These switches can be used for switching differential signals ranging from 0 V to 5 V.

TS3DV416 supports four signal pairs for high-speed multiplexing and is used for switching the main four channels.

TS3DV20812 supports three additional side-band bits to manage the DDC (SCL, SDA) and CEC control signals. These three signals are supported by PMOS and NMOS switches, and the I/O of each signal is up to V_{CC}.

TS3DV520E supports five signal pairs for high-speed multiplexing and can be used for either high-speed or low-speed signals. All I/Os can accept up to 5-V input even when the chip V_{CC} is 3.3 V. This 5-V tolerance enables the use of pullup resistors to 5 V to interface the DVI/HDMI defined 5-V DDC and 5-V CEC control signals.

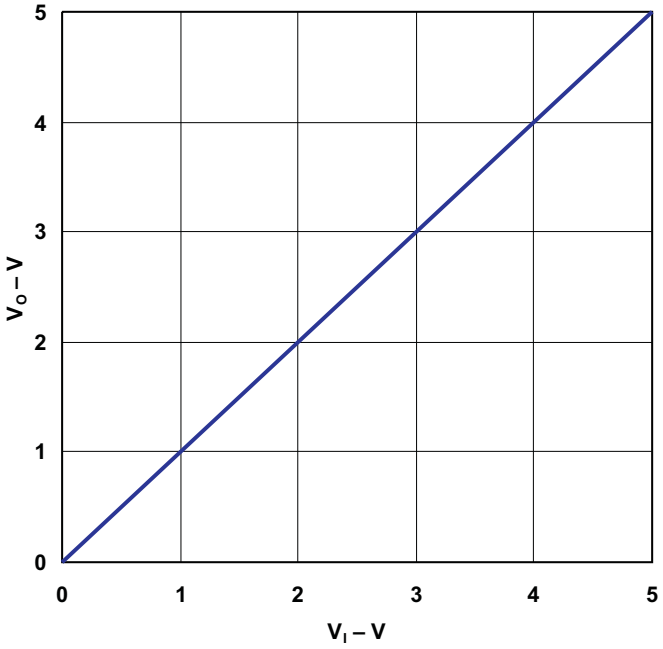


Figure 25. V_O vs V_I at 3.3-V V_{CC}

3.7.1 Multiplexing in DVI and HDMI

These digital video switches are designed for multiplexing high-speed bidirectional differential signals. They can be used on either the source side to expand the video ports or on the sink side to multiplex the multiple video sources into a single video port that communicates with a display controller that can support only one video port during decoding.

Because these switches support data rates greater than 1.65 Gbps, they can be used in for DVI and HDMI 1.2a, which are defined at 1.65-Gbps data-rate signaling.

3.8 TS3DV421

TS3DV421 uses a lower-voltage technology to enable up to 3.8-Gbps data rate and is ideal for HDMI 1.3a and DisplayPort, which need the higher data rate to transfer the video data stream.

TS3DV421 has two different operation mode. One mode, with V_{SS} = 1.5 V and V_{DD} = 3.3 V, allows V_{IO} from 1.5 V to V_{DD} + 0.7 V to support DVI/HDMI. The second mode, with V_{SS} = 0 V and V_{DD} = 1.8 V, allows V_{IO} from 0 V to 1.8 V ± 0.7 V to support DisplayPort.

Because select control pin of TS3DV421 is referred to V_{SS} and V_{DD}, it needs external voltage divider to set high or low under the condition of 1.5-V V_{SS} and 3.3-V V_{DD} (see Figure 26).

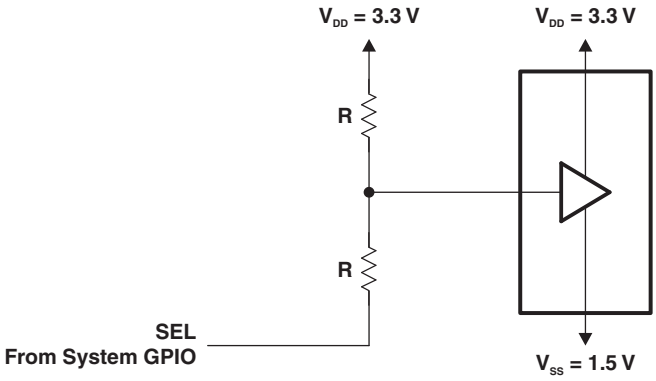


Figure 26. Example of Voltage Divider

3.9 TS3DS20812, TS3DS21012E

These switches are designed for use as internal LVDS switching, operating as 1:2 or 2:1 MUXes, where they do not need to support higher data rates such as 2.5 Gbps or 3.4 Gbps. They operate at >2-Gbps data rate and can pass any type of differential signaling within a 0-V to 5-V range. They can be used in for LVDS for panel display and also for other LVDS applications in telecommunication, base stations, and server applications.

These switches operate at V_{DD} = 2.5 V or V_{DD} = 3.3 V, and the voltage level changes the characteristics of r_{ON}, r_{ON} flatness, and V_{IO} range.

A 0-V to 5-V rail-to-rail V_{IO} range can be achieved when V_{DD} = 3.3 V. A 0-V to 3.3-V rail-to-rail V_{IO} range can be achieved when V_{DD} = 2.5 V. Because the LVDS signal range is 0 V to 2.4 V, either supply voltage is acceptable.

TS3DV20812 switches four pairs of high-speed differential signals and also supports three additional lower-speed signals. The high-speed switches can support LVDS channels, and the low-speed switches can support the DDC channel. Therefore, no additional external analog switch is required to switch the sideband control signals of DDC (SDA, SCL).

Figure 27 shows an example of using TS3DV20812 as a 1:2 MUX switching the LVDS source (transmitter) to dual LVDS sinks (LVDS receivers) connected to two different LCD panel displays.

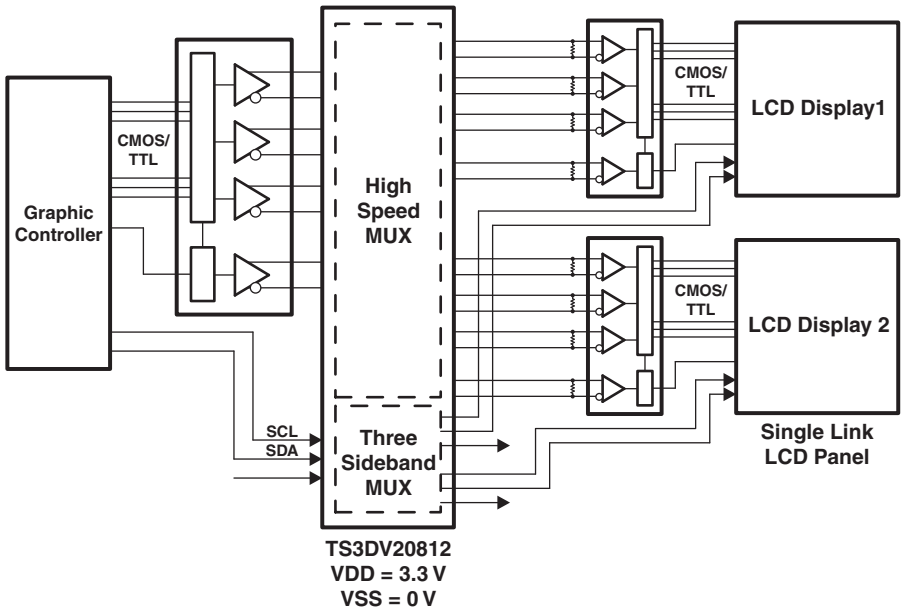


Figure 27. LVDS Switching MUX for 20-Pin LCD Panel Interface

According to the LCD standard panel interface (see Table 3), eight pairs or ten pairs are required for the main links in the 30-pin or 40-pin LCD interfaces, respectively. Therefore, the system requires two TS3DS21010E devices to get the ten pairs and or two TS3DS20812 devices to get eight pairs as 1:2 or 2:1 MUX/DEMUX application.

TS3DS20812 is a four-pair switching multiplexer for high-speed LVDS signaling, and TS3DS21012E is a five--pair switching multiplexer for LVDS. Both devices are bidirectional and can be used for 2:1 or 1:2 switching.

Figure 28 shows an example of using two TS3DS21012E devices switching the panel LVDS source for 30-pin or 40-pin LCD panel link interfaces to two LCD panel displays.

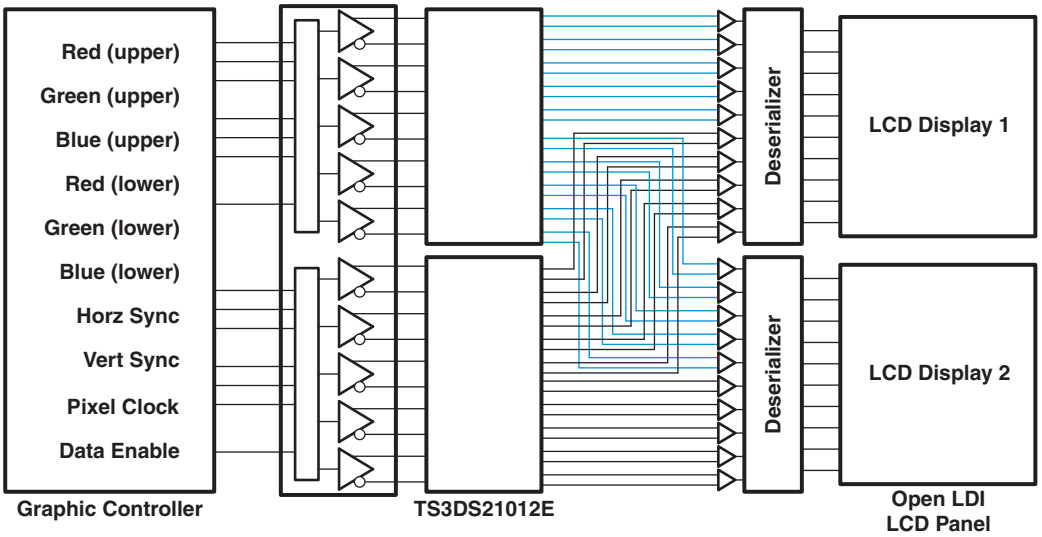


Figure 28. LVDS Switching MUX for 30-Pin LCD Panel Interface

Figure 29 shows an example of using TS3DS1012E switching LVDS as a 2:1 MUX from two LVDS transmitters to a single LVDS receiver connected to a TFT LCD panel display.

All of these switches are bidirectional and can also be applied as 2:1 multiplexers. One application for this feature is switching between dual sources of LVDS transmitters to a single receiver on an LCD panel display with the objective of changing the graphic video source for power saving (for example, when connected to ac, the external video controller is used, and when in battery mode, the embedded video is used). Two applications for such a system are PCs and mobile application processors.

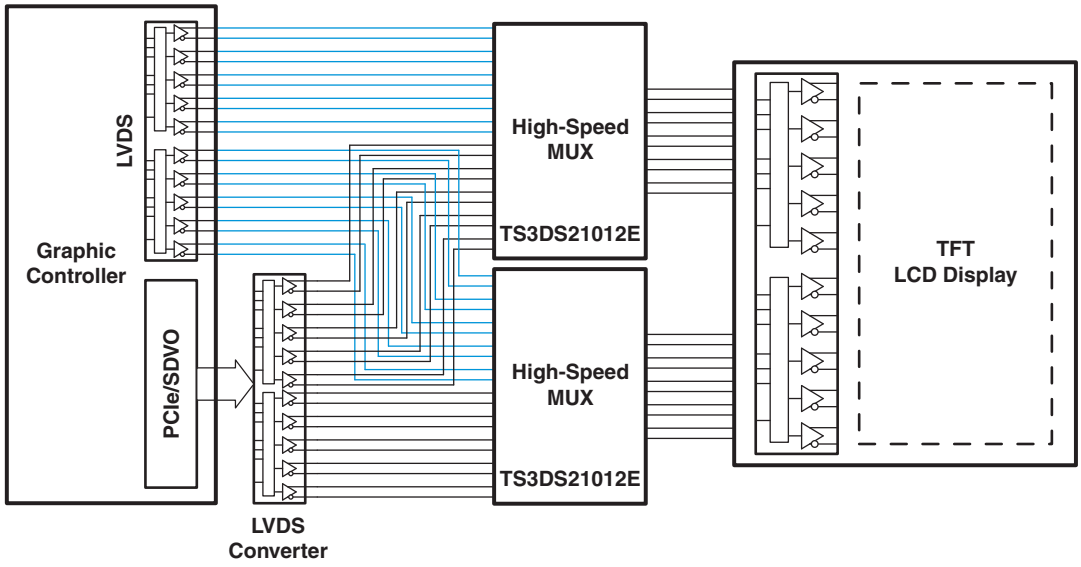


Figure 29. Two LVDS Transmitters to One LVDS Receiver (Dual Link)

The legacy LVDS data rate for LCD panel is from 1 Gbps to 1.65 Gbps. DisplayPort increases this rate to 2.7 Gbps per channel, which can reduce the number of LVDS channels while still achieving higher resolution. Therefore, DisplayPort may become the next standard LVDS signaling for LCD panels.

TS2DS30812 is ideal for this transition, because it supports >3-Gbps data rates and is operated at 1.8-V V_{DD} to achieve better dc characteristics and bandwidth switching in the V_{IO} range from 0 V to 2.4 V. It can be used for the current LVDS signal rates and for the higher-rate DP signaling.

3.10 Summary

The TS3DS, TS2DS, TS3DV, TS2PCIE, and TS3PCIE families are high-speed bidirectional high-performance low-resistance low-r_{ON} low-voltage switches with controlled channel skew, crosstalk, and insertion loss. These features enable differential signal bypassing with minimum distortion to keep the output signals as close to the input signals as possible, even when multiplexing.

Currently available passive switches support data rates up to 3.8 Gbps, and future devices will support 5 Gbps or even higher to meet future requirements.

There are several key features to consider when selecting the switch to use in particular differential signal application. The V_{IO} range is a key feature and must be within the differential signal input and output range. The other key feature of high-speed switches is bypassing any type of signal within the specified voltage I/O range and data rate with the least distortion.

4 Motherboards

Motherboards are high-volume applications that require flexibility in providing more standard PCIe bus slots. The high-speed passive switch is an inexpensive component that can switch the PCIe and DisplayPort signals.

Figure 30 shows an example how a motherboard can use high-speed passive switches to support both DisplayPort and HDMI. In a similar manner, TS2PCIE412 is shown being used in PCIe bus slot expansion.

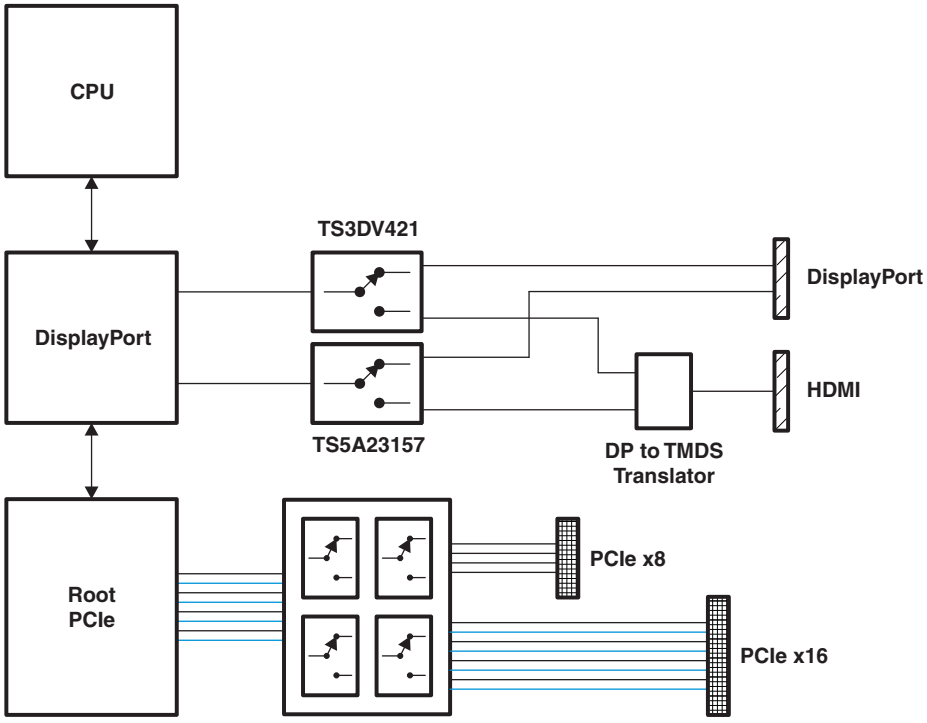


Figure 30. Typical Motherboard with High Speed Passive Switch

5 Notebooks

Notebooks designed for gaming, office use, or professional use have different requirements, and notebook designs can be varied using different types of high-speed differential switches.

For example, depending on the GPU that is embedded, the system could require a high-speed passive switch to select between LVDS and DP for the panel interface ,or it might need to select between two different LVDS sources to send to the panel display. To support two different video outputs, the system also needs a passive switch to connect two different video ports. Some embedded GPUs are designed with SDVO and PCIe signaling on the same pin and need passive switching to maximize the function of the notebook.

Figure 31 is a block diagram showing some applications of high-speed passive switches.

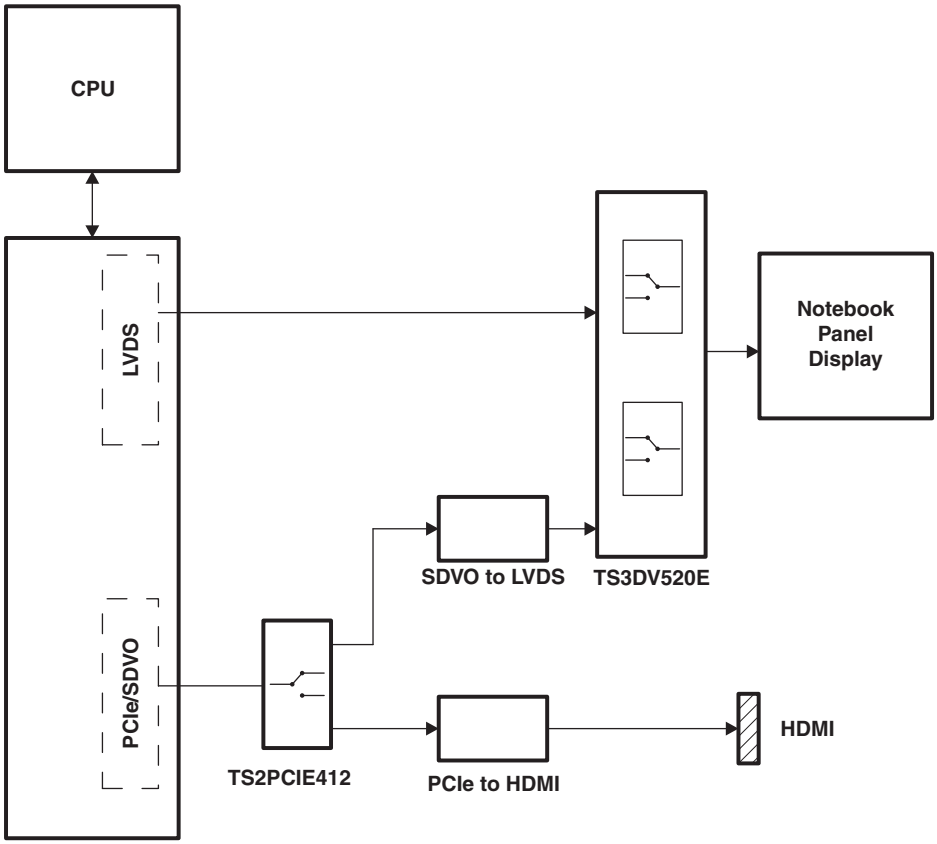


Figure 31. Typical Notebook with High-Speed Passive Switch

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7 Glossary of Terms

Bus LVDS— A parallel transmission system that uses a pair of low-voltage differential signals (LVDS). Also referred to as BLVDS.

DFP— Digital flat panel

DP— DisplayPort

DP++— Dual-Mode DisplayPort

DVI— Digital visual interface. A standard developed by Intel that defines the digital interface between devices such as projectors, computers, and monitors.

EVC— Enhanced video connector

GPU— Graphic processing unit

HDMI— High-definition multimedia interface

LVDS— Low-voltage differential signaling. The TIA/EIA-644A specification for high-speed transmission.

LVPECL— Low-voltage positive-emitter coupling logic

M-LVDS— Multipoint low-voltage differential signaling. Allows the use of multiple drivers and multiple receivers on a bus. M-LVDS also allows bidirectional half-duplex communication over a single media pair.

MDDI— Mobile Display Digital Interface

MIPI— Mobile Industry Processor Interface

Panel Bus Panel— A digital high-speed (1.65 Gbps) interface used primary for LCDs, digital televisions, and digital CRTs.

PCI Express— PCI Express (PCIe) fits common system architectures, provides greater speed and independence, and increases bandwidth and scalability. PCIe offers 4 Gbps of peak bandwidth per direction and 8 Gbps of concurrent bandwidth. PCIe is referred to as a third-generation input / output (3GIO).

SGI OpenLDI— The connector used on SGI digital flat panel monitors

TMDS— Transmission minimized differential signaling

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