Bus FET Switch Solutions for Live Insertion Applications

Tomdio Nana and Gary Khazan *Standard Linear & Logic*

ABSTRACT

In today's competitive computing and networking industry, any equipment downtime due to component interconnects or bus failures impedes communication, hinders productivity, and hampers financial growth. In recognizing this increasingly costly unplanned downtime, the industry introduced live-insertion technology to minimize the impact of any such failures. The live-insertion feature enables a network administrator to replace a failed unit without powering down the system, thereby maintaining high-availability solutions. This application report discuses the Texas Instruments bus-switch solutions for live-insertion technology. The following TI products are used as examples: SN74CBT6800A, SN74CBTLV16800, SN74CBTS6800, and SN74CBTK6800.

Keywords: bus contention, CBT, CBTLV, electrical performance, hot plug, live insertion, partial power down, precharged outputs

Contents

List of Figures

List of Tables

Introduction and Background

In today's computing industry, there is a tremendous increase in the demand for enhanced subsystem functionalities, prevailing mass storage capacity, extensive block data transfer, and improved system operating speed. This remarkable leap in technology and functionality has led to more dependence on computing systems having reliable and accurate information. To keep the varied and critical information flowing to end users, the computer industry has made innovations to overcome the challenges that face it. The peripheral component interconnect (PCI) technology is one of the latest innovations to meet the growing demand for information computer systems to be continuously available. PCI provides a high-speed data path between the central processing unit (CPU) and peripheral devices (video, disk, network, etc.)

Computing systems based on the industry-standard personal computer architecture have undergone steady improvement in the areas of reliability and availability. Some subsystems have been further enhanced by a process commonly referred to as live insertion, which allows the rest of the system to remain operational when circuit boards are removed or inserted.

The PCI bus has been improved with live-insertion capabilities, enabling standard PCI adapter cards to be inserted and removed in systems without turning off the system power. The PCI live-insertion technology benefits those systems in which a PCI adapter failure affects productivity of a large number of users, or affects sales; or, where the applications are too critical to have even a minimal amount of down time. It gives the network administrator valuable tools that keep the system operational by conducting the live-insertion operation without interfacing with the other PCI devices on the bus. The PCI adapter cards that are designed to meet *PCI Local Bus Specification, Revision 2.1,*[1] have a standard for removal and installation.

The reduction or complete elimination of noise and transients generated during live-insertion is a primary concern in the preservation of signal integrity on the PCI bus. Texas Instruments (TI) manufactures field-effect transistor (FET) bus switches that are designed to isolate the local bus from the PCI adapter during live insertion and removal. This application report introduces TI's bus-switch solutions for live-insertion applications, discusses their logic functionality, and their use in the intended applications. The information in this application report, along with the data sheets, should enable a system designer to successfully implement a live-insertion solution.

Definition of Terms

This section lists and defines some key terms used in this application report. The following definitions are specifically defined by TI and may or may not agree with other semiconductor vendor definitions.

Bus Contention

Bus contention occurs in a system when two (or more) drivers connected on the same bus are inadvertently placed in opposing states (one driver is driving a low while the other is driving a high). For example, if several bus drivers with 3-state outputs are connected to a single bus, it often cannot be ensured that, while switching from one bus driver to another, both are not simultaneously active for a short time. During this time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation also is known as bus conflict.

Figure 1 shows an illustration of bus contention in a system in which two devices are driving the same bus. One has high-level output and the other has low-level output. This results in the opposing logic levels producing a short between the drivers, creating a current surge that may damage the devices. However, an FET switch in the data path (see Figure 1) can isolate the two drivers when opposite logic levels are driven.

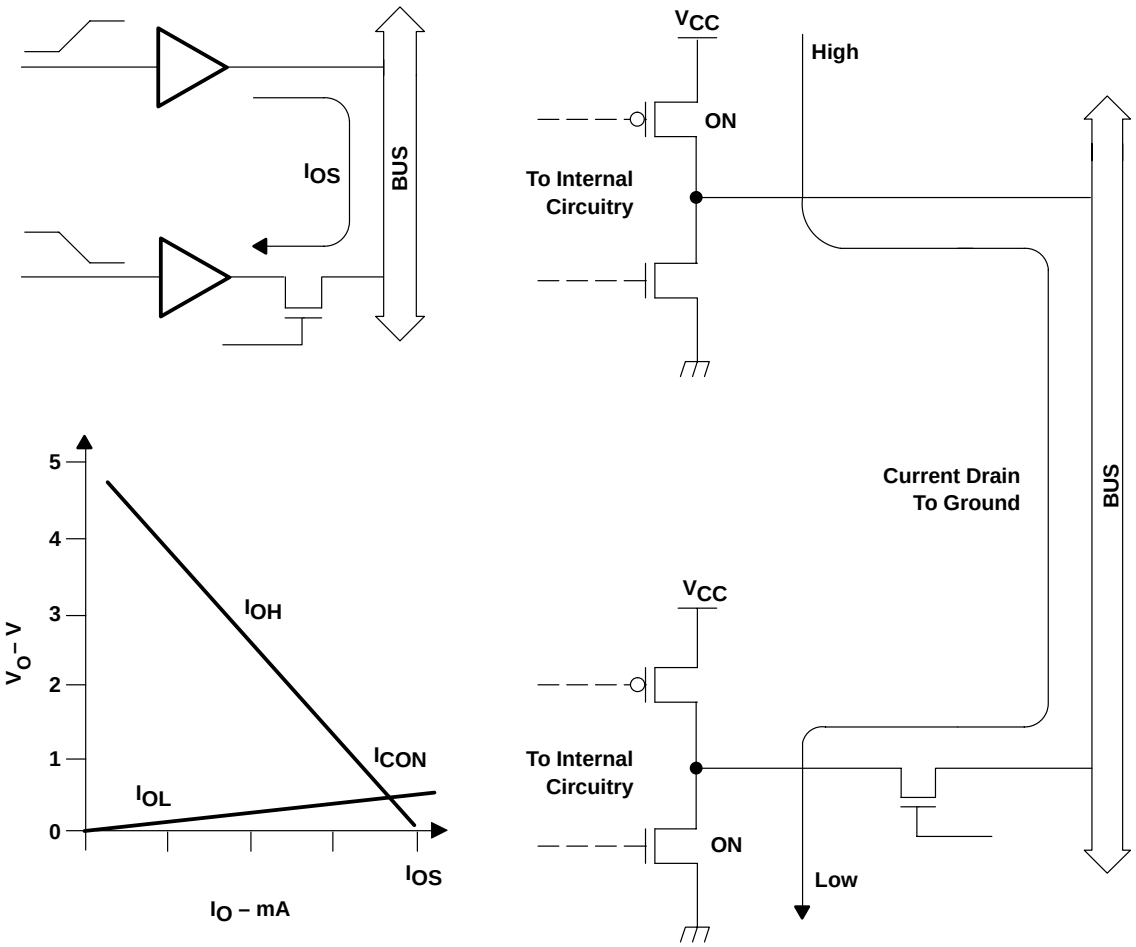


Figure 1. Short-Circuit Current With Bus Contention

During bus contention, the bus state may be unpredictably low, high, or somewhere in between. This unpredictable state during bus contention can cause data corruption during system operation. The current that results from bus contention can be calculated by means of the output characteristics of the devices. As shown in Figure 1, the short-circuit current (I_{OS}) is limited by the high output current of the device involved in the bus-contention situation.

TI data sheets specify the maximum continuous current through a single output or through V_{CC} and GND. These values are absolute maximum ratings, which are stress ratings, not recommended operating conditions. If bus contention occurs, these specifications can be exceeded, and it may cause permanent damage to the devices.

Partial Power Down

Partial power down is a system function or capability in which it is desired to power off some part of the system in order to conserve power. The system recognizes that some part of the system is not in use and places it in a power-off mode (in which the supply voltage, V_{CC}, is 0 V for the affected part of the system).

Because the system coordinates and controls the power-down/power-up sequence, typically it is required only to ensure that no circuit (either those that are powered on or those that are powered off) is damaged during the partial-power-off mode. This can be ensured if the circuits to be powered off have input and/or output circuits that maintain a high-impedance state while V_{CC} = 0 V.

With TI standard CMOS logic devices, this circuit capability is indicated by the specification of pin current at V_{CC} = 0 V, I_{off}. Typically, I_{off} is tested at pin voltages that approximate valid logic low and high levels (0.5 V, 3 V) and is specified in the range of ±100 μA.

For TI standard CMOS logic devices, the circuit modifications that are/may be required to support the I_{off} specification are the elimination of any diodes placed explicitly (as for ESD protection) between the pin and V_{CC} terminals. Many input and/or output circuits also may have parasitic diodes from pin to V_{CC}. In such cases, it is required to insert a reverse-oriented blocking diode to prevent unwanted currents from moving from the I/O pin to V_{CC}.

TI CBT and CBTS FET switches basically are pass transistors, with no path from the I/O to V_{CC}. Consequently, there is no leakage current from the I/O to V_{CC} when the device is powered off. I_{off} is, therefore, inherent to the CBT and CBTS FET switch devices due to the nature of their design, and I_{off} is not specified on the FET switches data sheets. Conversely, when the TI CBTK and CBTLV FET switches are powered off, a current leakage path from the device input may exist. Thus, a current-limiting circuit is included in the switch design to limit the current leak through the channel when the device is powered down. With the SN74CBTK6800 device, I_{off} is characterized over the valid input voltage range (0 V to 5 V) and is specified at 20 μA. Similarly, with the SN74CBTLV16800 device, I_{off} is characterized over the valid input voltage range (0 V to 3.6 V) and is specified at 10 μA.

Precharged Inputs/Outputs

During insertion (or removal) of a daughter card into (or from) a live bus, the data may be corrupted to the point where the signal transition actually traverses through the threshold region of an input device and switches the logic state of its output. This situation results in false data transfer, and damage to the device is possible.

Precharging the driver I/Os before insertion is a method used to minimize data corruption during insertion. Consider, for example, an energized bus at a high logic state. Before a daughter card is inserted into the live bus, the daughter card output voltage could be close to, or at, GND. Each signal pin that is being attached to the bus has an inherent capacitance due to the input and output IC structure, the IC package, the stub, and the connector itself.

The purpose of a capacitor is to resist a change in voltage. Therefore, when the connector pin makes contact, the daughter card's capacitance tries to force the bus signal as close to GND as it can and then increase, asymptotically, toward the original voltage. The degree to which the voltage can be forced low is dependent on the parasitics of the daughter card and the live bus. The larger the supporting parasitics, the bigger the perturbation.

Figure 2 shows what can happen when a high-parasitic capacitance is associated with the plug-in card. When the voltage spike crosses the input threshold voltage of a receiver, the data is corrupted. Insertion or removal of a daughter card does not present a concern when a live bus is biased to a logic-low level because any perturbation will, at most, force the bus voltage very close to 0 V.

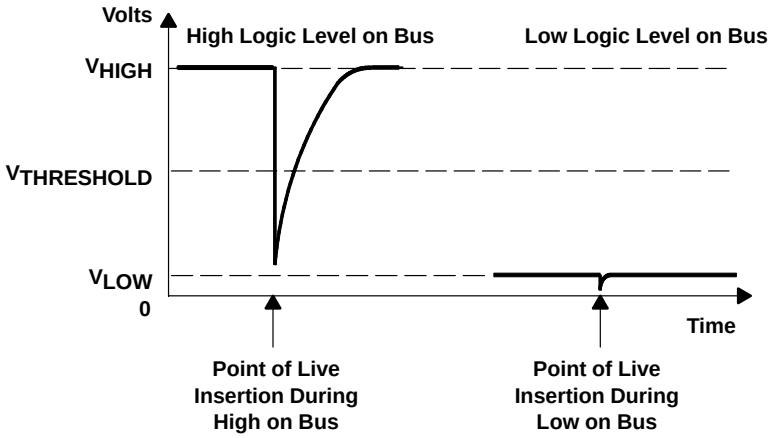


Figure 2. Possible Data-Corruption Scenarios Without Precharged Outputs

One way of limiting the glitch from crossing the threshold voltage is to reduce the parasitic capacitance. Ideally, it would be better to eliminate the capacitance altogether, but that is not possible. Another way in which the glitching effect can be reduced is to precharge the output pin of the device to a voltage centered between the low-level and high-level output voltage before the connector pin is attached to the active bus.

Figure 3 shows that, by setting the precharged voltage (BIASV) equal to the input threshold voltage, this perturbation can be reduced. Any glitch produced on the bus no longer crosses the input threshold region of the receiver, regardless of the state the bus is in when the glitch is generated. However, in the low state, the bus voltage is forced high and approaches the precharged voltage level, but never actually crosses the threshold, eliminating any chance of propagating a false data bit throughout the system.

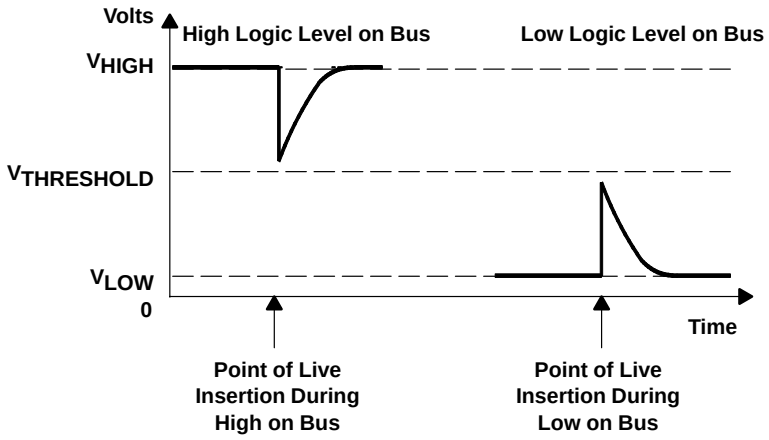


Figure 3. Precharge BIASV Functionality Eliminates Data Corruption

Live Insertion

Live insertion is a system functionality or capability in which it is desired to be able to insert unpowered circuit elements into a fully operational system. Generally, it also must support removal of powered circuits. This is typified by a card-rack system in which a malfunctioning card might need to be removed and replaced with a properly functioning card, without interrupting or otherwise adversely affecting the operation of other system circuits.

In many applications, there is a strict requirement for it to be possible to exchange system modules without interrupting normal system operation. A typical example is an electronic telephone exchange, in which the replacement of an individual telephone circuit must be possible at any time, without adversely affecting the operation or use of other telephone circuits. From a quality-of-service perspective, this capability is essential for such applications.

Since the act of live insertion (or removal) cannot take place in a maintenance mode in which the system is not expected to operate normally or without interruption, it is necessary to not only ensure that no circuits are damaged while the module is inserted or removed, but also to ensure that the insertion (or removal) does not cause the bus state to become invalid (even in a transient, glitch sense). The latter requirement is necessary to ensure that the live insertion (or removal) does not adversely affect bus transactions that may be occurring at the instant of insertion (removal).

Due to the capacitive nature of a circuit pin and the fact that this capacitance typically is uncharged upon insertion, a negative transient can occur on bus lines, which should be driven high. If the capacitive effect is idealized, the bus voltage would be expected to drop to 0 V at the point of insertion. However, if this capacitance can be precharged to a level that mitigates the magnitude of the bus glitch (approximately $V_{CC}/2$ for totem-pole signaling and V_{OH} for open-collector or open-drain signaling), the transient will have no ill effect.

This circuit capability is indicated by the specification of a precharged bias voltage, BIASV. Typically, bias currents also are provided as supporting specifications.

The required circuit provisions are referred to collectively as a precharge circuit. Typically, this consists of a voltage-divider resistor network, or something similar. Of course, since the primary supply voltage, V_{CC}, is 0 V, the precharge circuit must be powered otherwise. This requires the provision of a special supply-voltage terminal, typically designated BIASV. In use, it must be possible for BIASV to be powered before the primary supply voltage, V_{CC}. Typically, this is ensured through the use of mechanical sequencing, in which the connector pins, which bring BIASV (and GND) onto the module, make contact before the connector pins that bring V_{CC} onto the module.

Hot Plug

Hot plug is a system functionality or capability in which unpowered circuit elements are inserted into a fully powered (hot) system. Generally, also it must support removal of powered circuits. This is typified by a card-rack system, in which a malfunctioning card might need to be removed and replaced.

If this can be done while the system remains powered, then, although the system may be placed in a nonoperational or maintenance mode, the system can be returned more quickly to normal operation than if the system were powered off for maintenance. PCMCIA is a familiar example in which card-based functions can be removed or inserted without having to power off and cold-start the system. From a quality-of-service perspective, this capability is essential for many applications.

Because the act of hot plug (or removal) usually can take place in a maintenance mode in which the system is not expected to operate normally (i.e., without interruption), typically it is required only to ensure that no circuits are damaged while the module to be inserted (or removed) is unpowered, as well as during its power-up (or power-down) sequence. This requires that circuits that interface the module to be inserted in the system bus have input and/or output circuits that maintain the high-impedance state while V_{CC} = 0 V (see I_{off}, above) *and* while V_{CC} is powering up to (or powering down from) an operational level. The latter requirement ensures that these circuits do not contend on the system bus with circuits already in place and powered up.

TI Live-Insertion FET Switch Devices

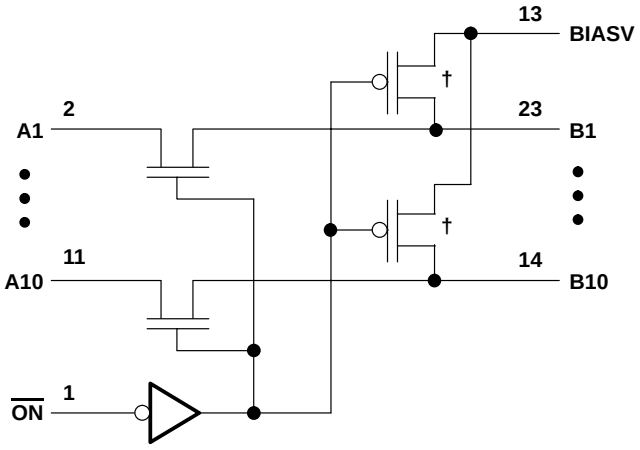
SN74CBT6800A 10-Bit FET Bus Switch with Precharged Outputs

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on, and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open. When $\overline{ON}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor. The functional operation of the SN74CBT6800A is shown in Table 1 and the logic diagram is shown in Figure 4.

Table 1. SN74CBT6800A Function Table

INPUT $\overline{ON}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



† Equivalent 10-kΩ resistance when turned on

Figure 4. SN74CBT6800A Logic Diagram (Positive Logic)

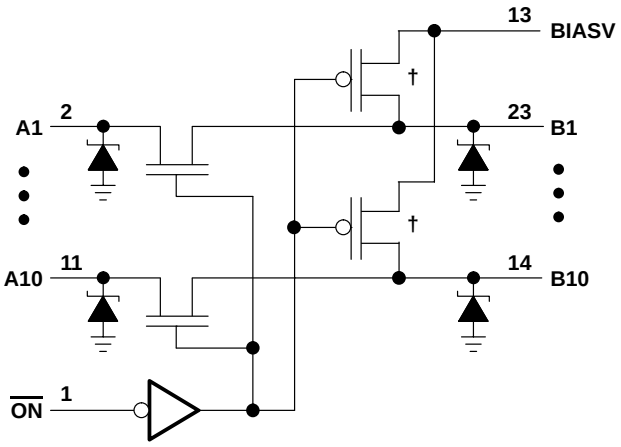
The SN74CBT6800A is characterized for operation from –40°C to 85°C, with a supply voltage from 4-V to 5.5-V V_{CC}.

SN74CBTS6800 10-Bit FET Bus Switch with Precharged Outputs and Schottky-Diode Clamping

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching, with Schottky diodes on the I/Os to clamp undershoots. Functionally, the device is identical to and pin-to-pin compatible with, the SN74CBT6800A. In addition, the SN74CBTS6800 has Schottky diodes at the I/O ports for undershoot protection.

The undershoot event does not affect performance of the switch when the switch is on. But, if undershoots occur when the bus switch is off, passing unwanted data can cause data errors. To prevent this, two Schottky diodes are connected from the source and drain to ground. When one of the buses has negative voltage that exceeds the forward turn-on voltage of the Schottky diode, the diode turns on and clamps the source or drain voltage of the NMOS switch, keeping the buses isolated.

Functional operation of the SN74CBTS6800 is same as that for the SN74CBT6800A (see Table 1). The logic diagram of the SN74CBTS6800 is shown in Figure 5.



† Equivalent 10-kΩ resistance when turned on

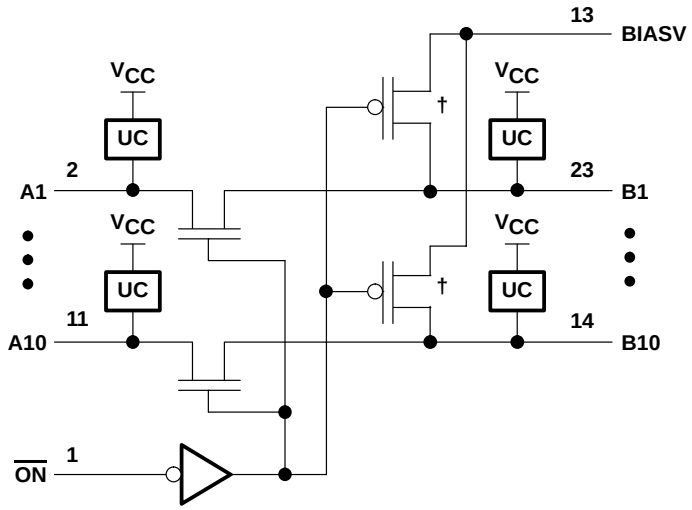
Figure 5. SN74CBTS6800 Logic Diagram (Positive Logic)

SN74CBTK6800 10-Bit FET Bus Switch with Precharged Outputs and Active-Clamp Undershoot-Protection Circuit

The SN74CBTK6800 provides ten bits of high-speed TTL-compatible bus switching with an active-clamp undershoot-protection circuit. Functionally, the device is identical to, and pin-to-pin compatible with, the SN74CBT6800A. When there is an undershoot, the active-clamp circuit in the SN74CBTK6800 is enabled, and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

In the active-clamp circuit, a bias generator sets a voltage slightly above ground potential, which allows the active-clamp pullup voltage to turn on during an undershoot event. The clamp counteracts the undershoot voltage and limits V_{GS}, V_{GD} of the n-channel, and V_{be} of the parasitic npn transistor.

Functional operation of the SN74CBTK6800 is same as that for the SN74CBT6800A (see Table 1). The logic diagram of the SN74CBTK6800 is shown in Figure 6.



UC = undershoot clamp circuit
† Equivalent 10-kΩ resistance when turned on

Figure 6. SN74CBTK6800 Logic Diagram (Positive Logic)

The SN74CBT6800A, SN74CBTS6800, and SN74CBTK6800 are 10-bit FET bus switches that are characterized for operation from –40°C to 85°C, with a supply voltage from 4-V to 5.5-V V_{CC}. The major differences between the three devices are summarized in Table 2.

Table 2. Differences Between the SN74CBT6800A, SN74CBTS6800, and SN74CBTK6800

FEATURES	SN74CBT6800A	SN74CBTS6800	SN74CBTK6800
Undershoot protection	No undershoot protection. This could cause the n-channel pass transistor to turn on and affect the buses.	Some undershoot protection. Slow to react to undershoot voltage with fast edge rates.	Excellent undershoot protection
I/O capacitance	Low C_{io}	Minimal addition of the input/output capacitance	Increased C_{io}
Power requirement	More power required	Less power required	Average power required
Overvoltage tolerance	No overvoltage tolerance	No overvoltage tolerance	Overvoltage-tolerant I/Os

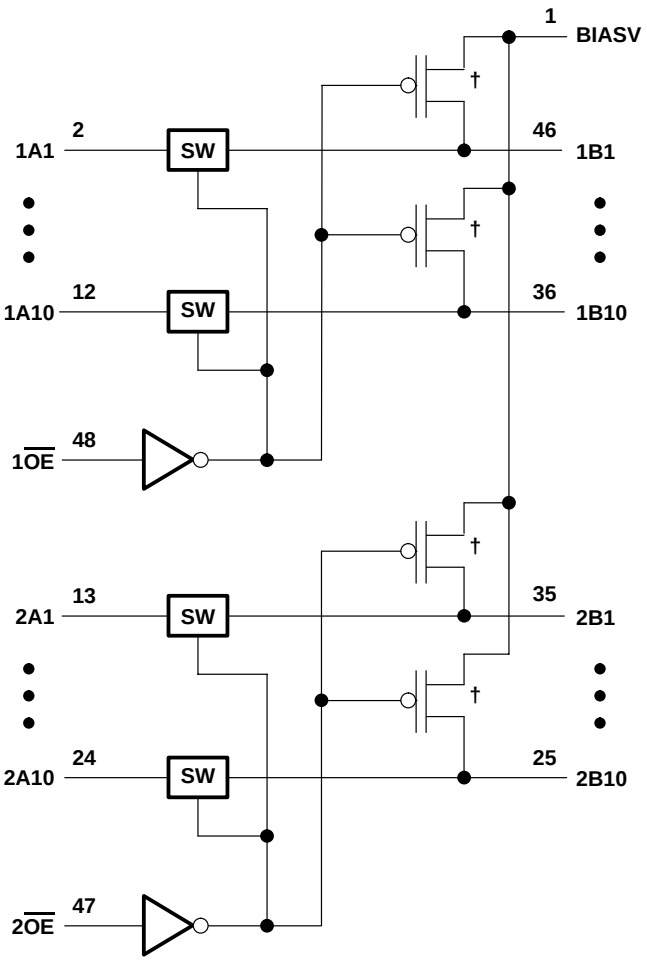
SN74CBTLV16800 Low-Voltage 20-Bit FET Bus Switch with Precharged Outputs

The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to BIASV to minimize live-insertion noise.

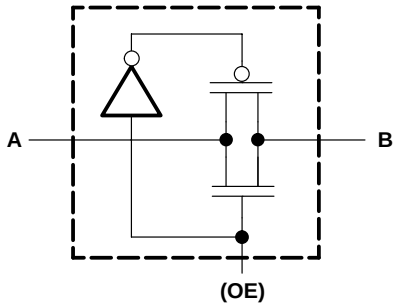
The SN74CBTLV16800 is organized as dual 10-bit bus switches with separate output-enables ($\overline{OE}$) input. It can be used as two 10-bit bus switches or one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, the high-impedance state exist between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor. The functional operation of the SN74CBTLV16800 is shown in Table 3 and the logic diagram is shown in Figure 7.

Table 3. SN74CBTLV16800 Function Table for Each 10-Bit Bus Switch

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



Simplified Schematic of Each FET Switch (SW)



† Equivalent 10-kΩ resistance when turned on

Figure 7. SN74CBTLV16800 Logic Diagram (Positive Logic)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. For information on calculating the desired pullup resistor value, refer to application report *HCMOS Design Considerations*, literature number SCLA007.[8]

The SN74CBTLV16800 is characterized for operation from –40°C to 85°C and the supply voltage from 2.3-V to 3.6-V V_{CC}.

Live-Insertion Applications with FET Switch Devices

In many applications, the system cannot be shut down at any time. Examples include industrial control systems, communications, and financial networks. All maintenance and replacements should be done when the system is running without bus disruptions. Figure 8 shows a diagram of a typical distributed control system.

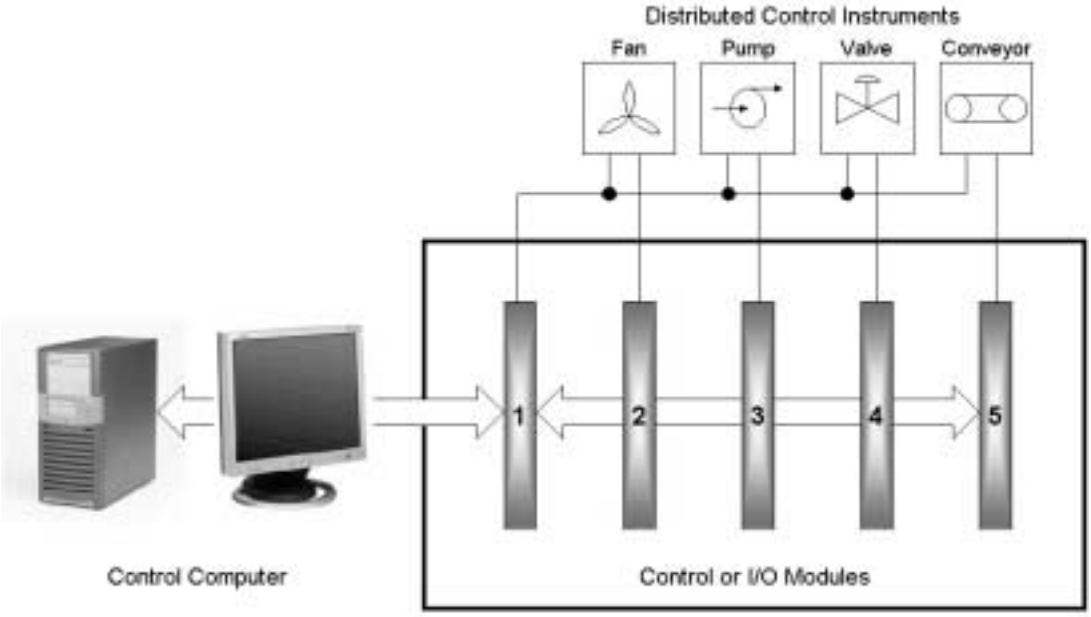


Figure 8. Example of a Typical Distributed Control System

In most cases, control modules should be replaced without shutting down the system, without interruptions for other modules, and without bus errors. The TI live-insertion FET switches can be used for this purpose.

TI FET switches, with precharged outputs, offer an opportunity for successful live-insertion design. A proper insertion sequence always should be followed to avoid excessive current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. A good ground connection must make the first contact with the bus connector.
2. Power-up of BIASV supply. BIASV supply should make contact consistent with, or after, GND.
3. The V_{CC} power supply, output-enable control, and then the signal lines (in that order) must make the connection.
4. The full insertion of the PCI adapter should prompt the PCI local bus to start communicating with the new device.

A six-slot board was made to accommodate six PCBs, each having one SN74CBTLV16800, driven independently as if it were a separate control module. The modules were connected as shown in Figure 9. In the experiment, only two modules were used, module 1 and module 6.

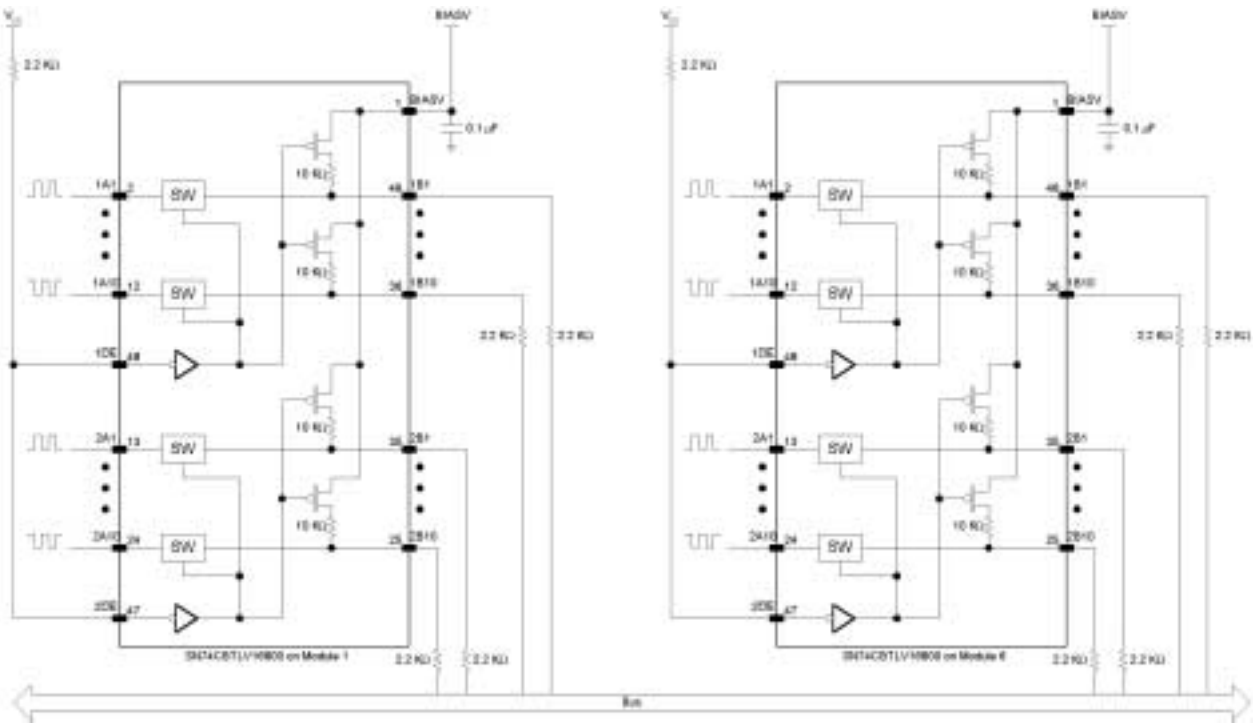


Figure 9. Laboratory Set-Up for Live-Insertion Experiments With the SN74CBTLV16800

The laboratory tests were done with different bus input-level combinations and, in all cases, the GND and BIASV made contact first, followed by V_{CC}, $\overline{OE}$s, and signal lines. 1$\overline{OE}$ was tied to V_{CC} through a 2.2-kΩ resistor (for a data generator used as an input source).

Figures 10 through 13 show the relationships of the module 1 1B1 output (CH1) and module 6 BIASV (CH2) signal, 1$\overline{OE}$ (CH3) input, and 1A1 (CH4) input. During the experiment, module 1, with one SN74CBTLV16800, already was plugged into the six-slot PCB, and module 6, with one SN74CBTLV16800, was inserted at the time, T, as shown on the plots. The 1A1 input signal of the inserted module 6 is driven either low or high during insertion, and the 1B1 output signal (from module 1) driven on the bus is either low or high.

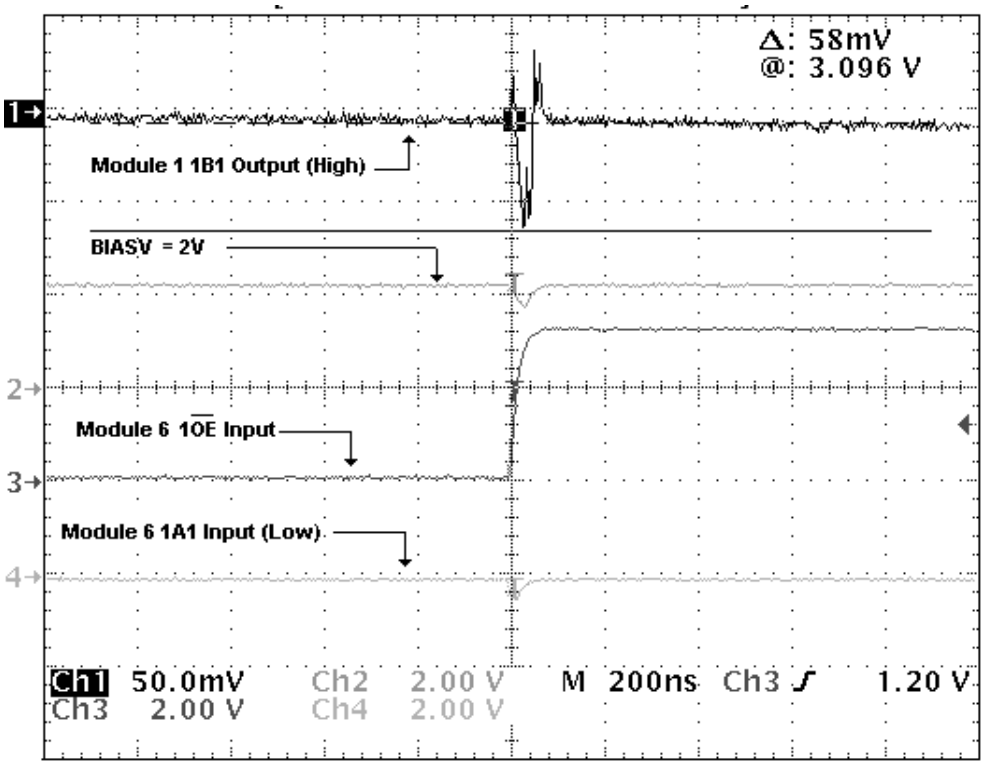


Figure 10. SN74CBTLV16800 Signals During Live Insertion (1A1 = Low, 1B1 = High)

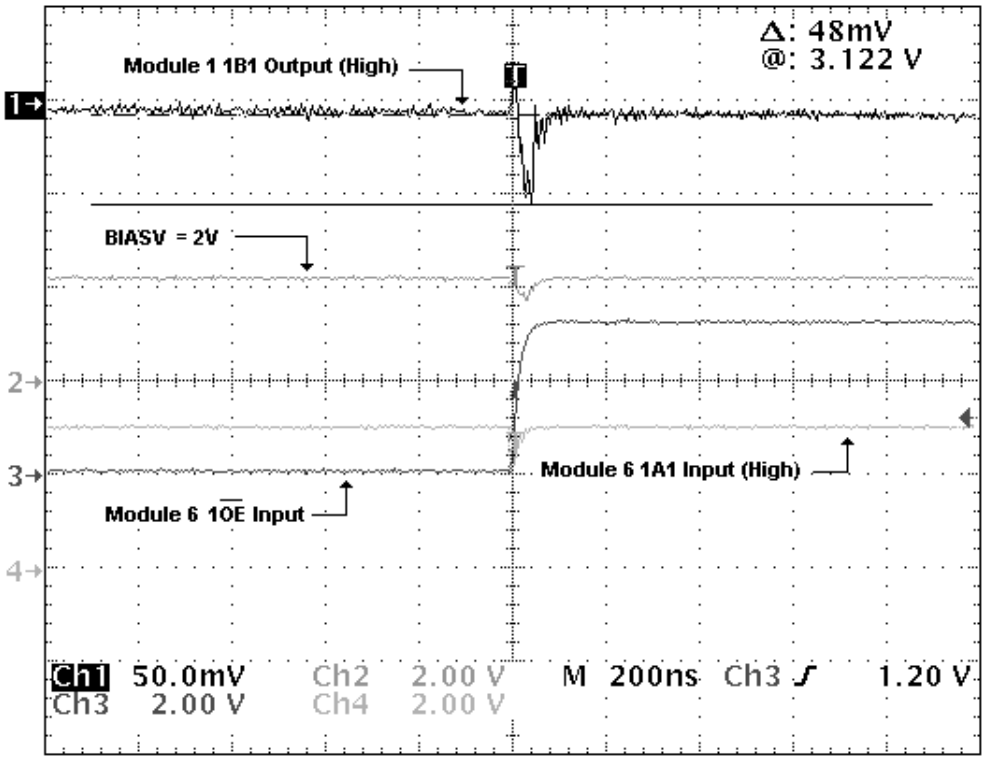


Figure 11. SN74CBTLV16800 Signals During Live Insertion (1A1 = High, 1B1 = High)

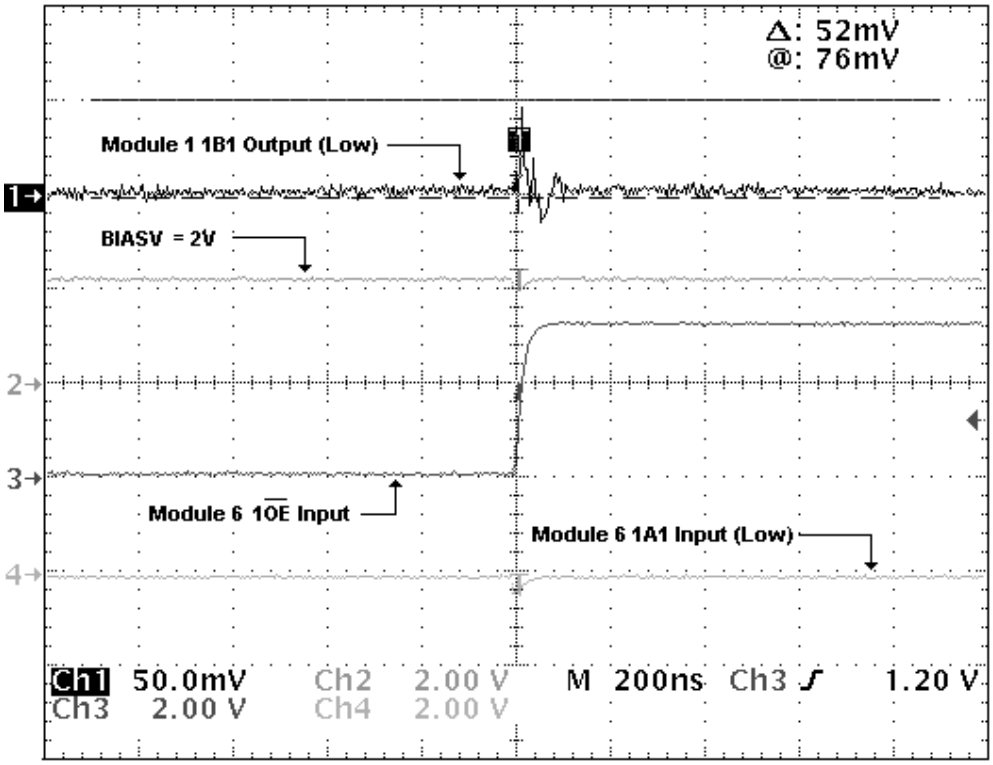


Figure 12. SN74CBTLV16800 Signals During Live Insertion (1A1 = Low, 1B1 = Low)

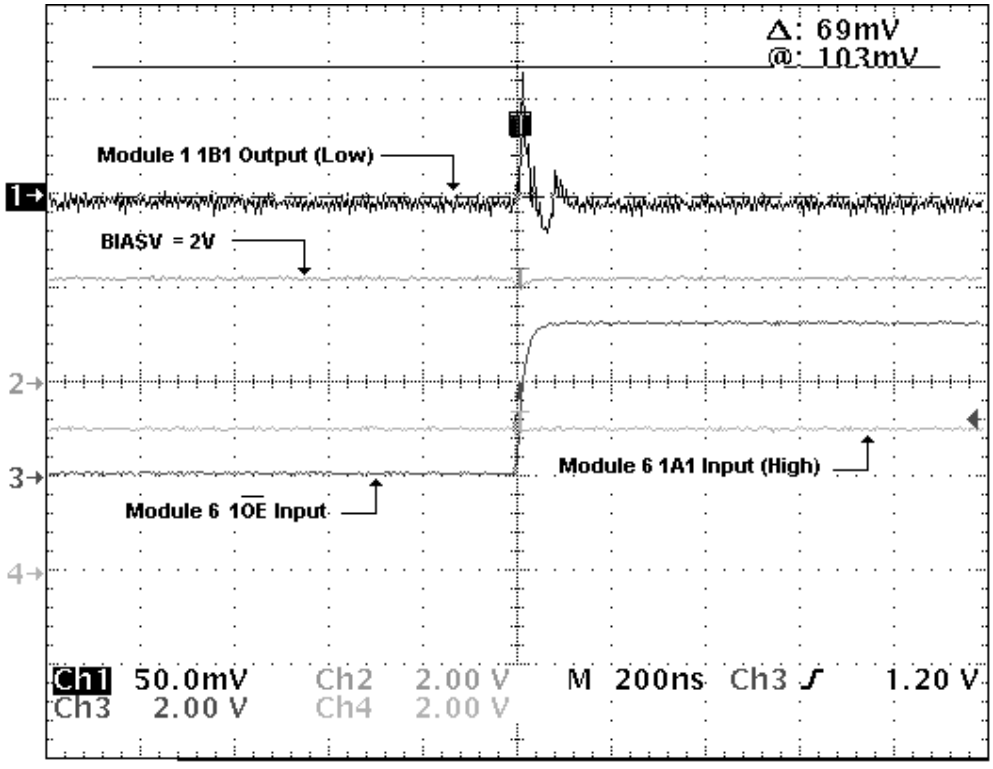


Figure 13. SN74CBTLV16800 Signals During Live Insertion (1A1 = High, 1B1 = Low)

During the tests, the outputs were pulled to BIASV level (set to 2 V in these cases) when they are disabled (1$\overline{OE}$ = high). As observed in the plots, the bus-signal glitch does not exceed 100 mV and cannot cause data corruption. Also, the glitch is very narrow (in these cases, less than 0.5 μs). In reality, the duration of the “pulse” depends on signal level, connector quality, bus impedance at the insertion point, and operating frequency.

To demonstrate the benefit of using the FET switch with precharged output, the same test was done using the SN74CBTLV16800, with BIASV disconnected (floating). In this case, during live insertion, the outputs were not precharged and the signal quality was the same as using any ordinary FET switch without the precharged feature. Figure 14 shows the relationships of input (1A1), 1$\overline{OE}$, BIASV, and Output (1B1) signals for one channel of the SN74CBTLV16800 that is being inserted at time, T. The 1A1 input signal of the inserted module either is driven low or high during insertion, and the 1B1 output signal driven on the bus either is low or high.

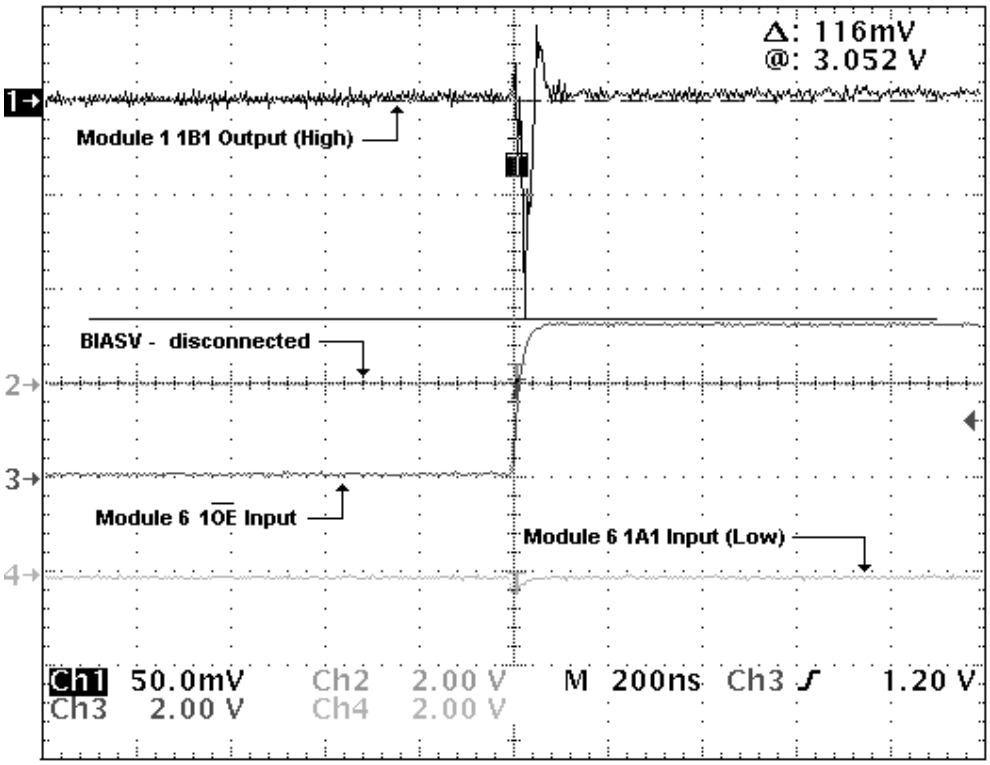


Figure 14. SN74CBTLV16800 Signals During Live Insertion, No Precharge

As shown in Figure 14, without the precharge feature, the bus signal glitches and exceeds 150 mV (peak-to-peak).

Features and Benefits

Table 4 summarizes the features and benefits of TI live-insertion FET switch devices.

Table 4. Features and Benefits

FEATURES	BENEFITS
Live insertion with uninterruptable operation	Ability to replace or upgrade a card without disrupting the operation or degrading the signal on the bus
User-selectable bias voltage	Enables the user to set the outputs precharged voltage
Output-enable feature	Allows device to be placed in the high-impedance state and prevent bus contention
Flow-through pinout	Ease of trace routing

Conclusion

The live-insertion technology has raised the level of system availability with zero-downtime support. Therefore, it is possible to have a system that may never need to be shut down for maintenance. These new hardware designs have built-in redundancy and, at the same time, provision for upgrades. This application report presents TI bus-switch solutions for live-insertion applications, discusses their logic functionality, and their use in the intended applications.

Frequently Asked Questions (FAQs)

What are Texas Instruments crossbar switches?

Crossbar switches are high-speed bus-connect devices. Each CBT FET switch consists of an n-channel MOS transistor driven by a CMOS gate. When enabled, the n-channel transistor gate is pulled to V_{CC} and the switch is on. Conversely, each CBTLV FET switch consists of an n-channel MOS transistor in parallel with a p-channel MOS transistor. The control signal driving the gate of the n-channel transistor is inverted to drive the gate of the p-channel transistor. When enabled, the n-channel transistor gate is pulled to V_{CC}, the p-channel transistor gate is pulled to GND, and the switch is on. The crossbar switches typically have an on resistance of 5 Ω and a propagation delay of 250 ps.

How do I get copies of the logic data sheets and samples?

The logic data sheets can be obtained by accessing http://www.ti.com. Samples of the logic devices can be obtained by contacting your local TI sales representative.

How do I get copies of logic HSPICE and IBIS models?

The HSPICE models for logic devices can be obtained by contacting your local TI sales representative. The IBIS models can be obtained by accessing http://www.ti.com.

What is important about live insertion?

Many systems in communication applications must remain operational 24 hours a day, 7 days a week. These systems cannot be shut down when a board is inserted or removed from the system, as frequently happens during regular maintenance or system upgrades, nor can active system data be disturbed.

The devices discussed in this application report fully support live insertion, with BIASV circuitry for precharging the outputs during power-up. BIAS circuitry allows easy internal precharging of the daughter-card connections to mid-threshold levels to prevent glitching active data during card insertion or removal.

What are the advantages of using the live-insertion bus FET switch solutions?

The advantages of using the live-insertion bus FET switch solutions include:

- Live insertion with uninterruptable operation makes them usable in systems that require replacing or upgrading a card without disrupting the operation or degrading the signal on the bus.
- User-selectable bias voltage enables the user to set the outputs' precharge voltage.
- The output-enable feature allows the device to be placed in the high-impedance state, preventing bus contention.
- Flow-through pinout eases PCB trace routing.

References

1. *PCI Local Bus Specification*, Revision 2.1, June 1, 1995, PCI Special Interest Group, Portland, Oregon.
2. *PCI Hot-Plug Specification*, Revision 1.0, October 6, 1997, PCI Special Interest Group, Portland, Oregon.
3. *Logic in Live-Insertion Applications With a Focus on GTLP*, application report, literature number SCEA026.
4. *SN74CBT6800A 10-Bit FET Bus Switch with Precharged Outputs*, data sheet, literature number SCDS005.
5. *SN74CBTS6800 10-Bit FET Bus Switch with Precharged Outputs and Schottky Diodes Clamping*, data sheet, literature number SCDS102.
6. *SN74CBTK6800 10-Bit FET Bus Switch with Precharged Outputs and Active-Clamp Undershoot-Protection Circuit*, data sheet, literature number SCDS107.
7. *SN74CBTLV16800 Low-Voltage 20-Bit FET Bus Switch with Precharged Outputs*, data sheet, literature number SCDS045.
8. *HCMOS Design Considerations*, application report, literature number SCLA007.
9. *Live Insertion*, application report, literature number SDYA012.

Glossary

BiCMOS	Bipolar and complementary metal-oxide-semiconductor process
BIASV	A user-selectable bias voltage to which a live-insertion device is precharged in order to minimize live-insertion noise.
CBT	Crossbar technology logic
CBTLV	Low-voltage crossbar technology logic
CMOS	Complementary metal-oxide-silicon; a device technology that has balanced drive outputs and low power consumption
CPU	Central processing unit
FET	Field-effect transistor
IBIS	I/O buffer information specification
I_{OFF}	Input/output power-off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input or output to 2.7 V and V_{CC} = 0 V
PCB	Printed circuit board
PCI	Peripheral-component interconnect
SPICE	Simulation program with integrated-circuit emphasis
TI	Texas Instruments
TTL	Transistor-transistor logic
V_{OH}	High-level output voltage. The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.
V_{OL}	Low-level output voltage. The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265