Fast GTLP Backplanes With the GTLPH1655

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ABSTRACT

This revision of the *Fast GTL Backplanes With the GTL1655* application report addresses improvements, such as the improved OEC™ circuitry and implementation of the Texas Instruments TI-OPC™ circuitry, that have been incorporated in the GTLPH1655 device. These improvements significantly improve signal integrity in distributed loads.

This application report describes the physical principles of fast bus systems and the problems that can arise in their development. These descriptions are based on line theory, and various specifications of TTL, backplane transceiver logic (BTL), Gunning transceiver logic (GTL), and Gunning transceiver logic plus (GTLP) integrated circuits are compared.

In addition, this application report presents the performance of the SN74GTLPH1655. This new UBT™ device provides an optimum solution for the design of backplanes for future high-speed bus systems.

Comprehensive measurement results of the SN74GTLPH1655 also are included in this application report.

Contents

Introduction 4
Physical Principles 5
Does a Line Behave Like a Capacitive Load? 5
Transmission-Line Theory in Practice 7
Effects on Bus Lines 11
Beginning of the Line: The Incident Wave 11
End of the Line: The Reflected Wave 13
New Bus Systems Are Needed 15
BTL Bus 16
GTL Bus 17
Comparison Between BTL and GTL 18
New Backplane Solution: SN74GTLPH1655 From TI 19

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Features of the SN74GTLPH1655 20
Functional Description: SN74GTLPH1655 – UBT 20
SN74GTLPH1655: Link Between a GTLP Backplane and an LVTTL Module 21
Termination Voltage, V_{TT} 22
Reference Voltage, V_{REF} 23
Static Characteristics of the SN74GTLPH1655 24
TI-OPC Circuitry 29
Edge-Rate Control (ERC) 29
Removal and Insertion Under Voltage and Partially Switched-Off Systems 32
Measurements on GTLPH1655 Test Board 34
Measurement Results With an Unloaded Backplane (Z_O = 30 Ω, R_{TT} = 25 Ω) 36
Measurement Results With a Loaded Backplane (Z_O = 25 Ω, R_{TT} = 25 Ω) 42
Summary 48
References 49
Glossary 50

List of Figures

1 Physical Relationships on a Connecting Line Between Two Components 5
2 Physical Relationships on a Bus Line 6
3 Waveform on a Line Compared to Waveform With a Load Capacitor 7
4 Wavefronts on Lines 8
5 Signals at End of the Line 10
6 Example of a Bus Line 11
7 Load on a Driver in the Middle of the Bus is $0.5 \times Z_O$ 12
8 Termination Methods With TTL and CMOS Circuits 14
9 Circuit Concept of BTL Bus 16
10 Circuit Concept of GTL Bus 17
11 Comparison of Logic Voltage Levels of BTL and GTL 18
12 Typical Bus Application for a UBT 20
13 LVTTL and GTLP Signal Levels of SN74GTLPH1655 21
14 Proposed Layout of Termination Resistors and Bypass Capacitor on a Circuit Board 22
15 Suggested Connection of V_{REF} Pin 23
16 Input Characteristics of SN74GTLPH1655 24
17 Bus-Hold Characteristics at LVTTL Input of SN74GTLPH1655 25
18 GTLP Bus: An Open-Drain Bus 26
19 Output Characteristics of GTLP Port of SN74GTLPH1655 27
20 Output Characteristics of LVTTL Side of SN74GTLPH1655 28
21 TI-OPC Circuitry Replacement of GTLP 29
22 Setup for Measuring Edge Rate at GTLP Side of SN74GTLPH1655 30
23 Falling Edge, ERC = V_{CC} (Slow Edges), Input Signals t_f = 2 ns, 10 ns 30
24 Falling Edge, ERC = GND (Fast Edges), Input Signals t_f = 2 ns, 10 ns 31
25 Rising Edge, ERC = V_{CC} (Slow Edges), Input Signals t_r = 2 ns, 10 ns 31
26 Rising Edge, ERC = GND (Fast Edges), Input Signals t_r = 2 ns, 10 ns 32
27 Influence of Precharge Function on Bus Signal 33
28 Principle of Construction of GTLP Bus on GTLPH1655 Test Board 34

29 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 10 MHz 36
30 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 10 MHz 36
31 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 10 MHz 37
32 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 10 MHz 37
33 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 50 MHz 38
34 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 50 MHz 38
35 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 50 MHz 39
36 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 50 MHz 39
37 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 160 MHz 40
38 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 160 MHz 40
39 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 160 MHz 41
40 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 160 MHz 41
41 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 10 MHz 42
42 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 10 MHz 42
43 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 10 MHz 43
44 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 10 MHz 43
45 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 50 MHz 44
46 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 50 MHz 44
47 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 50 MHz 45
48 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 50 MHz 45
49 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 160 MHz 46
50 GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 160 MHz 46
51 LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 160 MHz 47
52 GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 160 MHz 47

List of Tables

1 Additional Capacitive Loading of a Bus Line by a Module 6
2 Typical Characteristic Properties of Lines 8
3 Signal Delay Using Figure 6 as an Example 11
4 Comparison of Characteristics of BTL and GTL 18
5 SN74GTLPH1655 Compared With BTL and GTL 19
6 Choice of GTL/GTLP Level (Using V_{TT} and V_{REF}) 21
7 Measurement Results on SN74GTLPH1655 Demonstration Board 35

Introduction

Since the 1970s, bus systems have been used in every microprocessor system. In the early systems, the delay time of the driver was in the range of 15 ns to 20 ns, and the frequency of the system clock was about 1 MHz. The speed of the total system was determined primarily by the delay time of the active electronics, for example, the processor, gates, and bus drivers.

With increasing clock rates, the bus began to limit the performance of the total system. To circumvent this limitation, numerous improvements have been introduced in modern bus systems:

Pipelining	By pipelining, instructions and data are transmitted continually from the memory to the processor.
Cache memory	To avoid having the fast processor continually waiting for the slow main memory (DRAM, EPROM), an intermediate storage of the current data is implemented in a fast cache memory.
Block transfer	The transfer of individual words of data is replaced by the transmission of complete data blocks.
Multimaster	Every device connected to the bus can initiate the transmission of data. The cumbersome and slow route of transferring data exclusively via the CPU is, therefore, no longer necessary.
Bus width	The bus width has grown from 8 bits to 64 bits, and larger.
Clock rate	The clock rate of the backplane has increased into the range of many tens of megahertz, e.g., with a PCI bus to 33 MHz or 66 MHz. The processor itself operates internally at far higher clock rates, e.g., at 400 MHz. The memory is connected by a dedicated bus that operates at very high clock rates, e.g., up to 400 MHz. The memory is connected by a special bus (e.g., the Direct *RAMBUS*™), operating at 800 MHz) to the processor.

The first sections of this application report deal exclusively with general physical principles and conditions. The engineer developing a bus system must be concerned with these to achieve high data rates on the bus.

Circuit solutions based on TTL, BTL, and GTL logic families are compared. Particular attention is devoted to the GTLP transceiver circuit having increased drive capability and support for live insertion.

The SN74GTLPH1655 is presented and examined in detail.

Direct *RAMBUS* is a trademark of Rambus Inc.

Physical Principles

In data sheets, the delay times of driver circuits are commonly given with a load circuit of 50 pF and 500 Ω at the outputs. However, this load circuit does not correspond well to the actual effective loads in current application. Rather, it is intended to match the conditions existing with IC testers. In particular, a load of this kind does not correspond to reality with bus systems. If the connecting line between two components is compared with the relationship on a bus line, significant differences exist.

Does a Line Behave Like a Capacitive Load?

The conditions shown in Figure 1 represent a typical connecting line between two components. If the connecting line is 20 cm long, then there is a very small capacitive load of 12 pF. As shown in Figure 2, modules are connected to a bus line with a 2-cm space between them, and these contribute an additional capacitive loading of 20 pF/2 cm (= 10 pF/cm) (see Table 1). A typical bus line on the backplane wiring of a 19-inch rack having a length of 40 cm, therefore, has a total capacitance of 424 pF (10.6 pF/cm × 40 cm).

The development engineer needs to know the effect of the capacitive load on the signal delay of drivers under the previously mentioned conditions (C_L = 12 pF, or C_L = 424 pF). The delay times given in data sheets assume a load of 50 pF.

However, now the line cannot be considered a capacitive load, but instead must be treated from the point of view of transmission-line theory. With the bus line described previously, a signal delay of 10 ns (25 ns/m × 0.4 m) from one end of the line to the other is observed. If a pulse edge is applied at the beginning of the line having a rise time of 2 ns, the signal proceeds 8 cm (2 ns/25 ns/m) within this rise time. During this pulse edge, nothing happens over the length of the rest of the bus line (32 cm). Therefore, during this time, the capacitance of a 32-cm line (340 pF) has not been charged. The capacitance of this part of the line has no influence on the waveform or the signal delay of the driver circuit.

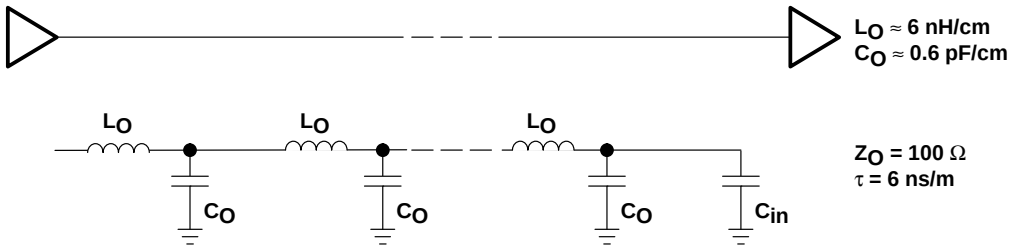

Figure 1. Physical Relationships on a Connecting Line Between Two Components

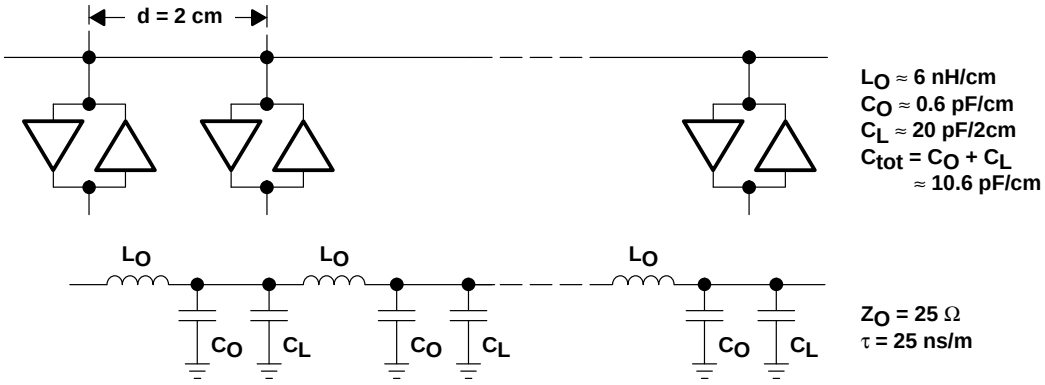

Figure 2. Physical Relationships on a Bus Line

Table 1. Additional Capacitive Loading of a Bus Line by a Module

CONTRIBUTOR	CAPACITANCE (pF)
Capacitance of the connector plug	≈5
Capacitance of the feedline from the driver I/O	≈5
Capacitance of the driver I/O	≈10
Capacitive loading from a module (total)	≈20

To illustrate this situation, Figure 3 shows a comparison between the waveform on a line with that from a load consisting of a lumped capacitance. It can be seen clearly in the diagram on the left that the length of a line and, therefore, its capacitance, has no influence on the waveform. To better observe the various loads, the rising edge is shown shifted by 10 ns. In the diagram on the right, instead of a line, a capacitor having the equivalent total capacitance value has been connected to the output of the test circuit. In this case, the output edge takes the form of a capacitor-charging curve. If the two measurement results are compared, it is clear that signals on a line behave very differently than in the case of a capacitive load. Therefore, an analysis using transmission-line theory is necessary.

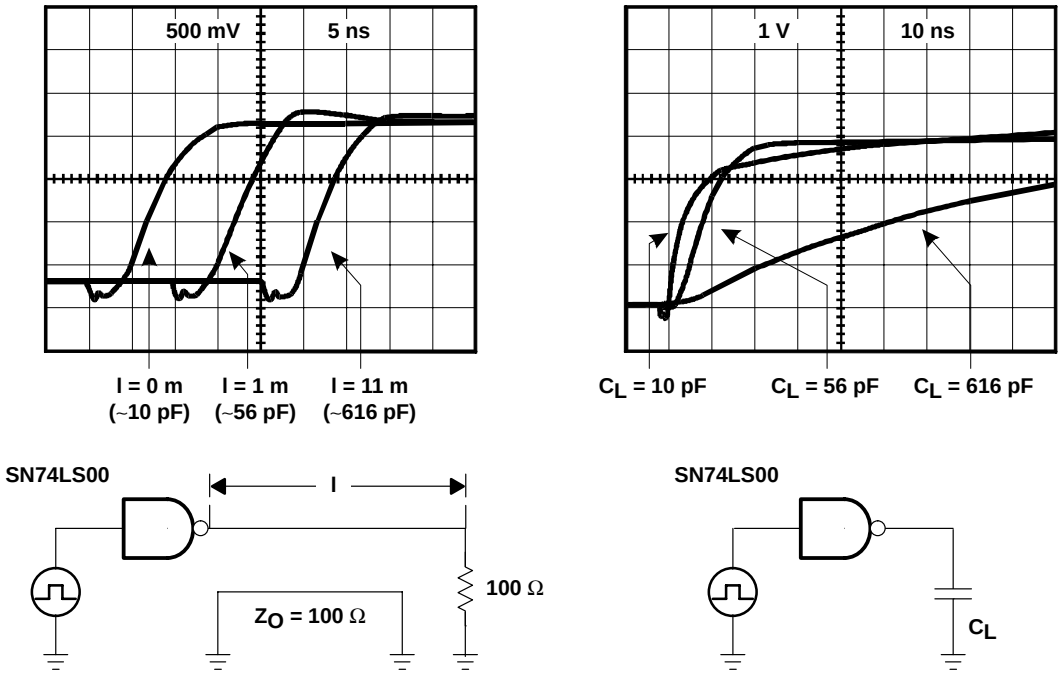

Figure 3. Waveform on a Line Compared to Waveform With a Load Capacitor

Transmission-Line Theory in Practice

With lines of more than a certain length, the behavior of signals must be analyzed using transmission-line theory. There is a simple rule that applies in this situation:

> *If the rise time or fall time of a signal is shorter than twice the line propagation delay time, transmission-line theory must be used.*

In practice, transmission-line theory must be used for a bus line with a propagation delay of 25 ns/m and a signal with an edge rise time of 2 ns, from a line length of 4 cm (2 ns/25 ns/m $\times$ 2). Because buses usually are longer than 4 cm, transmission-line theory is a necessary basis for examining the physical characteristics of bus lines.

With the frequencies and lengths of lines that now are used commonly in bus systems, the transmission-line theory can be simplified by neglecting any resistive component of the impedance. Equations 1 and 2 can be used for lossless lines with sufficient accuracy. Table 2 lists typical values for the characteristic properties of point-to-point lines between two components and bus lines.

$$Z_O = \sqrt{\frac{L'}{C'}} \quad (1)$$

$$\tau = \sqrt{L' \times C'} \quad (2)$$

Where:

Z_O = impedance of the line (Ω)
τ = propagation delay of the line (ns/m)
L' = inductive component of the line (nH/cm)
C' = capacitive component of the line (pF/cm)

Table 2. Typical Characteristic Properties of Lines

	L' (nH/cm)	C' (pF/cm)	Z_O (Ω)	τ (ns/m)
Point-to-point line between two components	5 to 10	0.5 to 1.5	70 to 100	≈5
Bus line	5 to 10	10 to 30	20 to 40	10 to 20

If a signal edge is fed into the beginning of the line (see Figure 4), a signal amplitude is created that can be calculated from the simple voltage divider, consisting of the internal resistance of the signal generator and the impedance of the line (Equation 3). The termination resistor R_{TT} has no influence on the edge because, at this point, the edge changes the voltage only at the beginning of the line, and at the end of the line no voltage change occurs.

$$U_i = U_G \frac{Z_O}{Z_O + R_G} \quad (3)$$

Where:

U_i = amplitude of the incident wave (V)
U_G = open-circuit voltage of the signal generator (V)
R_G = output resistance of the signal generator (Ω)
Z_O = impedance of the line (Ω)

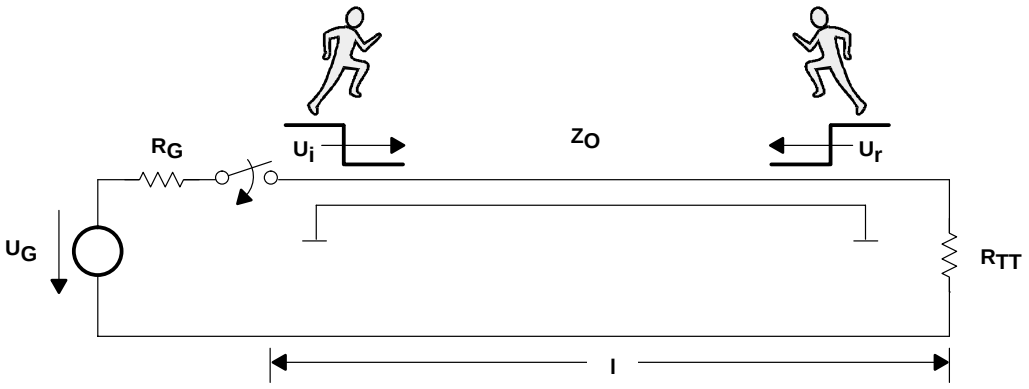

Figure 4. Wavefronts on Lines

This voltage edge now runs from the beginning of the line to the end. This first wave is called the incident wave. When the voltage wave reaches the end of the line, a reflected voltage wave is generated, the amplitude of which can be calculated from the reflection factor ρ, as shown in Equations 4 and 5.

$$\rho = \frac{R_{TT} - Z_O}{R_{TT} + Z_O} \quad (4)$$

$$U_r = U_i \times \rho \quad (5)$$

Where:

U_r = amplitude of the reflected wave (V)
U_i = amplitude of the incident wave (V)
ρ = reflection factor
R_{TT} = termination resistor at the end of the line (Ω)
Z_O = impedance of the line (Ω)

Using Equations 3, 4, and 5, results at the end of the line can be predicted:

$R_{TT} = 0 \Rightarrow \rho = -1$ (see Figure 5a)

The incident wave is inverted and reflected at the end of the line. Incident and reflected waves therefore cancel out each other, and there is no voltage increase at the end of the line.

$R_{TT} = Z_O \Rightarrow \rho = 0$ (see Figure 5b)

No line reflections occur. The end of the line is perfectly terminated.

$R_{TT} = \infty \Rightarrow \rho = +1$ (see Figure 5c)

The incident wave is fully reflected at the end of the line. There is a doubling of the amplitude at the end of the line.

A detailed analysis follows in *End of the Line: The Reflected Wave*.

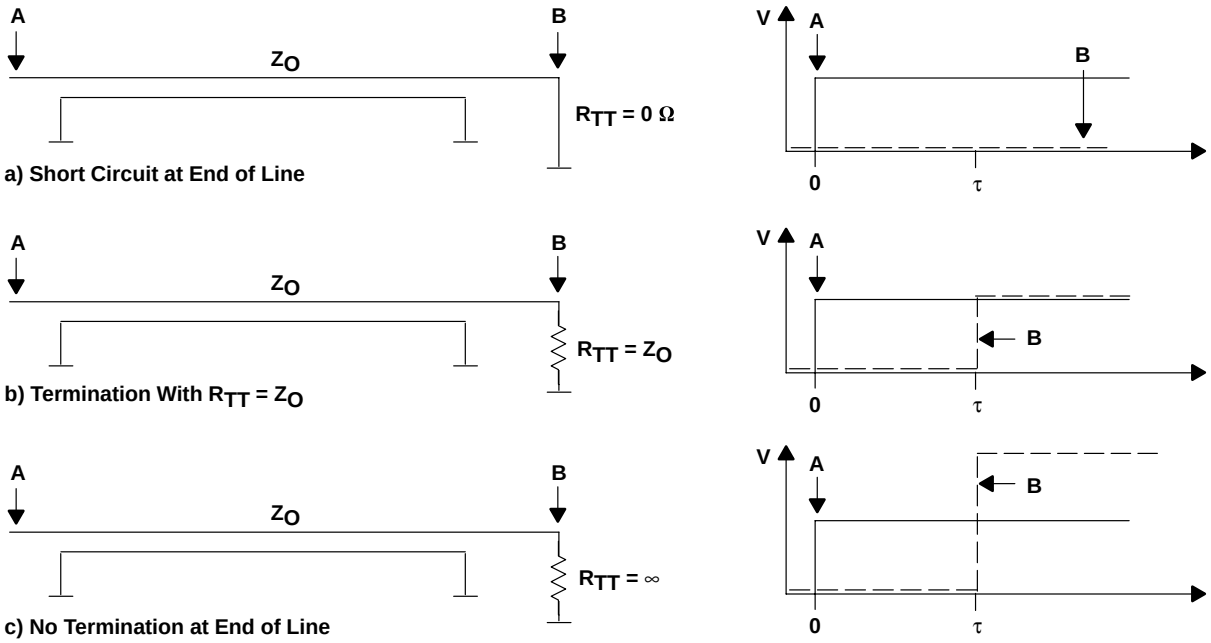

Figure 5. Signals at End of the Line

Effects on Bus Lines

Beginning of the Line: The Incident Wave

A fundamental characteristic of bus drivers is their output resistance. Together with the line impedance, this forms a voltage divider (Equation 3) and, thus, is responsible for the amplitude of the incident voltage wave.

If the driver can generate an incident voltage edge that has an amplitude above (below) the defined voltage threshold for the high logic state (low logic state), the logic level of all inputs that are connected on the bus will be changed over with the incident wave. For TTL-compatible bus systems, the rising edge of the incident voltage wave must exceed 2 V, and the falling edge must fall below 0.8 V. To calculate the maximum signal delay on the bus for an incident-wave-switching system, only the simple line propagation delay must be added to the delay time of the driver circuit (see Table 3).

Table 3. Signal Delay Using Figure 6 as an Example

	SWITCHING WITH THE INCIDENT WAVE	SWITCHING WITH THE REFLECTED WAVE
A⇒B	t_{pd} Driver + t_{pd} Receiver = 5 ns + 5 ns = 10 ns	t_{pd} Driver + t_{pd} Line + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 10 ns + 5 ns = 30 ns
A⇒C	t_{pd} Driver + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 5 ns = 20 ns	t_{pd} Driver + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 5 ns = 20 ns
Worst case	20 ns	30 ns

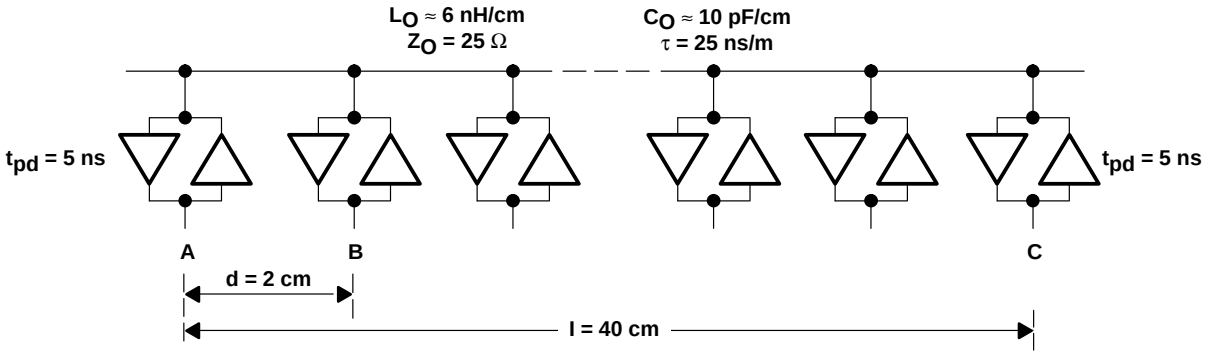

Figure 6. Example of a Bus Line

However, if the amplitude of the incident wave is insufficient, it is necessary to wait until the reflected wave returns from the end of the line to the beginning. Only then is a valid logic level reached on the entire bus line. In the example of Figure 6, according to Table 3, the signal delay time of 30 ns maximum results. Thus, when compared with switching with the incident wave, the signal delay time of the system is increased by 10 ns, or 50%.

This demonstrates one of the basic problems of bus systems. Since the amplitude of the incident wave depends on the voltage divider between the output resistance of the driver and the impedance of the line (≈25 Ω), a driver is needed with a particularly low output impedance. Only then is it possible to switch over a bus line with the incident wave. This is made more difficult because there are only two bus drivers at the beginning or end of the line. Most drivers sit in the middle of the bus line and, from there, must effectively drive two lines, one to the left and one to the right (see Figure 7). In this case, the resulting load impedance for drivers in the middle of the bus line effectively is halved (≈12.5 Ω).

Taking into account the voltage-divider rule for the incident wave, with TTL-compatible systems, an output resistance of <10 Ω is needed for the rising edge, and <4 Ω for the falling edge; the assumption here is that V_{OH} = 3.5 V, V_{OL} = 0 V. Even the most modern bus-driver families (such as the ABT family) do not have an output resistance that meets this requirement. For such applications, Texas Instruments (TI™) offers special TTL-compatible circuits, featuring the low output resistances that are needed: the incident wave switching (IWS) devices from TI, SN74ABT25xxx, for example, the SN74ABT25245. All other circuits that have the required low-resistance outputs were developed for new bus systems that are not TTL compatible. Examples of these new bus systems include BTL and GTLP.

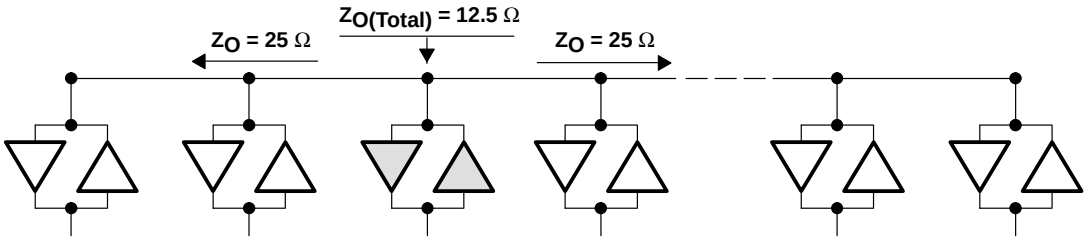

Figure 7. Load on a Driver in the Middle of the Bus is 0.5 × Z_O

TI is a trademark of Texas Instruments.

End of the Line: The Reflected Wave

As explained in *Transmission-Line Theory in Practice*, a voltage wave is reflected at the end of a line, and this reflected wave moves back to the beginning of the line. The amplitude of the reflected wave is determined by the amplitude of the incident wave and the reflection factor (Equation 5). This reflection factor is determined by the line impedance and the termination resistance (Equation 4). Therefore, the termination resistance has a major influence on the waveform of a bus line.

For the case of no termination resistance at the end of the line ($R_{TT} = \infty$), as shown in Figure 8a, the reflection factor is $\rho = 1$. The amplitude of the reflected wave is, therefore, exactly the same as the amplitude of the incident wave. In practice, this means that a low-resistance driver that generates an incident wave of 3 V, generates a reflected wave that also has an amplitude of 3 V. This results in an overshoot at the end of the line of 6 V ($V_{incident} + V_{reflected} = 3\ V + 3\ V$). The worst case would be a very low-resistance CMOS driver with an incident wave of 5 V, which would result in an overshoot of 10 V at the end of the line.

If the value of the termination resistance is assumed to be exactly the same as that of the line impedance, a reflection factor of $\rho = 0$ (Figure 8b) results. In this case, no reflection of the arriving wave occurs; thus, it is an ideal line termination. However, this method cannot be used with TTL and CMOS-compatible bus systems, because the impedance of the line would make it necessary to have a termination resistor of 25 Ω. With bidirectional lines, it would be necessary to connect this termination resistor at both ends, and each driver then would have to drive a load of 12.5 Ω. The maximum current through these resistors would be 280 mA (3.5 V/12.5 Ω) per line. Because, in practice, a bus often has more than 100 lines, the maximum total current of the bus termination would be >28 A. For this reason, with TTL systems, one operates with other terminating networks (Figure 8c to 8f) and, in such cases, accepts a mismatch ($R_{TT} > Z_O$).

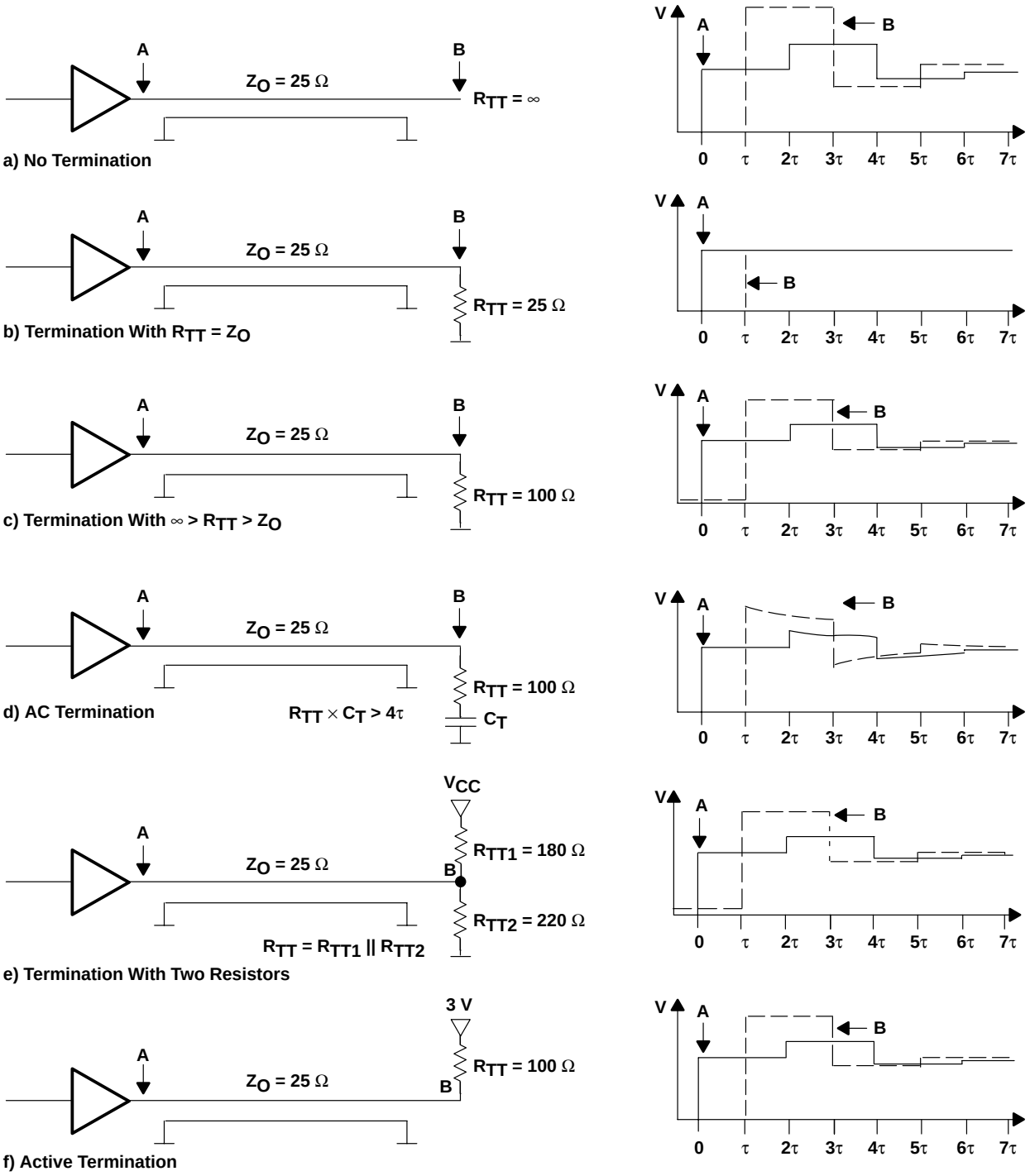

Figure 8. Termination Methods With TTL and CMOS Circuits

New Bus Systems Are Needed

The cause of most problems with bus lines is the distributed capacitive loading on the line by the modules connected to it. The impact on TTL and CMOS buses is:

- Very low signal speed on the line (about 25 ns/m, instead of 5 ns/m)
- The impedance of the line is reduced from about 80 Ω to about 25 Ω.
- As a result of the low impedance, adequate incident-wave amplitude is possible only with extremely low-resistance drivers.
- Correct termination is not possible because, otherwise, excessively high currents would flow through the terminating resistors.

It is not possible to solve these problems adequately with the circuit techniques commonly used with TTL- and CMOS-compatible circuits. With the commonly used techniques, it always would be necessary to accept a compromise in the circuit layout.

To develop a new bus system meeting the requirements imposed by the situation mentioned above requires the following:

- The capacitance of a module must be reduced, and also the capacitance of the I/O pins of the bus-driver circuit.
  - Because of the reduced capacitive component of the bus line, the impedance is reduced only to about 30 Ω.
  - The smaller capacitive component also results in less degradation of the signal speed (to about 20 ns/m).
- The drivers must be of low resistance to switch the bus with the incident wave.
- The signal amplitude must be reduced to allow correct termination of the line impedance. For example, with a signal amplitude of 1 V, a termination resistor of 30 Ω is adequate because the current flowing is only 33 mA per signal line.

The two bus systems that meet these basic physical requirements are BTL and GTL.

BTL Bus

The specification of the BTL bus was conceived especially for large backplane systems. The basic circuit layout of a BTL bus is shown in Figure 9.

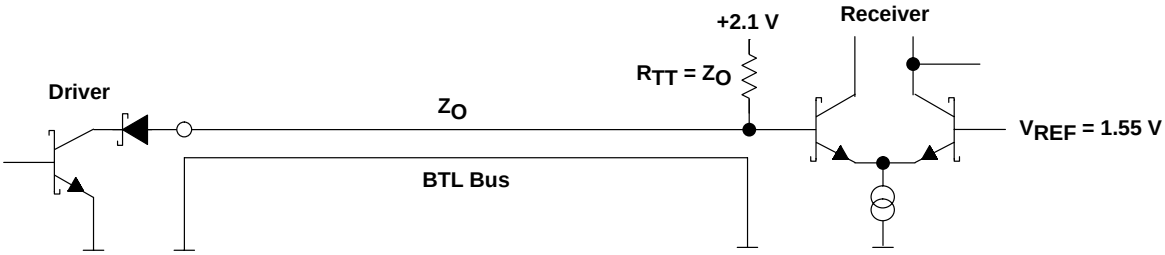

Figure 9. Circuit Concept of BTL Bus

The outputs of a BTL driver are provided with open-collector pins. The maximum capacitance of an I/O pin was fixed at 5 pF. To attain this goal, a diode is connected in series with the output transistor. The series connection of the capacitance of the transistor with the capacitance of the diode results in a reduction of the total capacitance. This circuit results in a low level of 1 V.

To allow switching of the bus lines with the incident wave, the specification for the drive capability was fixed at I_{OL} = 100 mA.

The high level is generated using a terminating resistor connected to 2.1 V at the end of the line. With bidirectional lines, a termination resistor must be provided at both ends of the line. As a result of the low signal amplitude of 1.1 V, the bus line can be terminated correctly with BTL systems. The maximum output current (I_{OL} = 100 mA) allows driving a terminating resistor of as low as 11 Ω (1.1 V/100 mA). If the BTL driver is in the middle of the bus line, the lower limit for the impedance is 22 Ω. This is sufficient for all bus systems that are used, particularly when the impedance and the signal speed are kept high, as a result of the limitation in the I/O capacitance.

By definition, the threshold voltage is 1.55 V, exactly midway between the low and high levels.

In large systems, it is essential that it be possible to remove and reinsert boards during system operation (live insertion). To meet this requirement, the precharge function has been implemented in BTL circuits. By means of this function, the capacitance of the pin, the stub line, and the I/O pin on the insertable board can be charged to the threshold voltage (1.55 V) before this pin comes in contact with the signal line on the backplane. Thus, it is possible to prevent signals on the backplane wiring from being so seriously interfered with that the data is corrupted.

The most serious disadvantage of the BTL bus is its high power consumption. If the transistor of a driver stage is operated to the limits of its specification, at the low level, a current of 100 mA can flow, with a voltage drop of 1 V. This results in the output stage dissipating 100 mW. If a 16-bit bus driver is used, in the worst case, 1.6 W may be consumed in the output transistors alone. With small surface-mounted components, this power consumption makes it necessary to use packages with a special heat sink.

GTL Bus

As shown in Figure 10, the basic circuit layout of the GTL bus is very similar to that of BTL. In this case, there also is a system with open-drain drivers and correct bus termination. The voltage levels of the logic states are 0.4 V in the low-logic state, and 1.2 V in the high-logic state. The signal amplitude is reduced to 0.8 V, whereby the threshold voltage lies exactly between the low and high levels, also at 0.8 V.

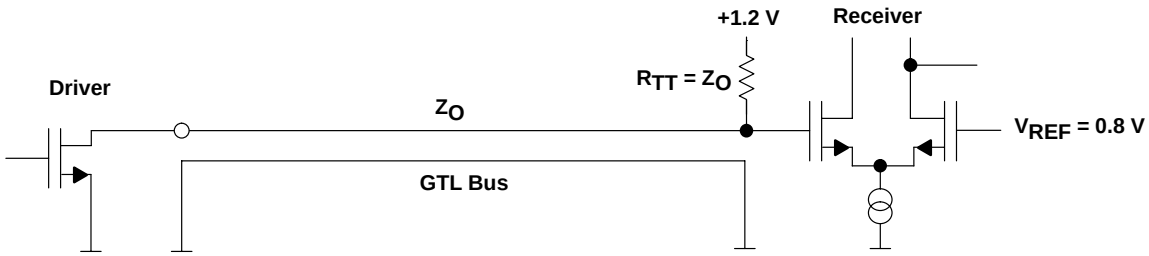

Figure 10. Circuit Concept of GTL Bus

In contrast to the BTL circuits, the drive capability of the output transistor is 40 mA. Therefore, the lower limit of the termination resistance (also of the line impedance) is 20 Ω (0.8 V/40 mA). For a driver connected to the middle of a bus line, the limit for the impedance of the line is 40 Ω. To attain impedance of the bus lines of 40 Ω, the capacitive component of the line must not be too high. Therefore, GTL is not the first choice when driving extensive backplane wiring with many modules.

Since the GTL bus was conceived for smaller buses on a circuit board, for example a memory bus between CPU and memory modules, the specification does not include the precharge function. The reason is that, when the bus is on a circuit board, there is no question of withdrawal and reinsertion during operation.

Comparison Between BTL and GTL

The structure of the two bus concepts (BTL and GTL) is similar. Both operate with open-collector/open-drain outputs and correct line termination. The most obvious difference is the definition of the logic voltage levels (Figure 11). The characteristics are listed and compared in Table 4. For large backplane wiring systems, the BTL circuits have the better characteristics, whereas the GTL bus features significantly lower power consumption. The target applications, which were considered when designing each of these bus systems, are apparent: BTL for large backplane systems, and GTL for smaller buses on a circuit board.

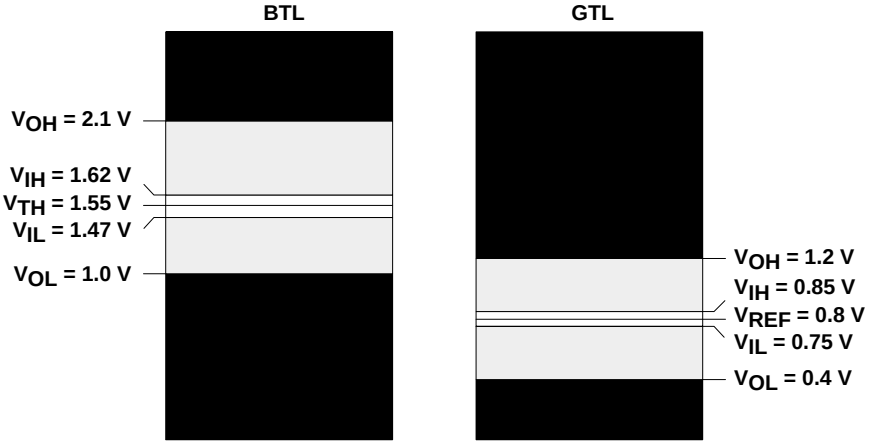

Figure 11. Comparison of Logic Voltage Levels of BTL and GTL

Table 4. Comparison of Characteristics of BTL and GTL

CHARACTERISTICS	BTL	GTL
Capacitance of an I/O pin	5 pF	Not defined, typically 5 pF to 9 pF
I_{OL}	100 mA	40 mA
Maximum power consumption of an output driver	100 mW	16 mW
Minimum Z_O for point-to-point connection	11 Ω	20 Ω
Minimum Z_O for a bus system	22 Ω	40 Ω
Precharge for withdrawing and reinserting boards during operation	Yes	No

New Backplane Solution: SN74GTLPH1655 From TI

It would be ideal to have a bus concept that combines all the desirable characteristics of both BTL and GTL. Meanwhile, TI offers a new generation of GTLP drivers that is compatible with existing GTL systems, but provides both the advantages of BTL and also the positive aspects of GTL drivers. A comparison is given in Table 5.

- The logic levels are compatible with GTL buses, and also bus systems with GTLP levels. GTLP represents a modification of the GTL specification that uses different termination voltage (V_{TT}) and reference voltage (V_{REF}) (see Table 6).
- Low capacitive loading of the bus (typical 6 pF)
- High drive capability (100 mA)
- Switching of a 11-Ω unidirectional line with the incident wave
- Switching of a 22-Ω bidirectional line with the incident wave
- Built-in precharge function

Table 5. SN74GTLPH1655 Compared With BTL and GTL

CHARACTERISTICS	BTL	GTL	GTL1655	GTLP MEDIUM	GTLP HIGH
Supply	5 V	5 V/3.3 V	3.3 V	3.3 V†	3.3 V†
I_{CC}	120 mA	120 mA	80 mA	50 mA	40 mA
I/O capacitance	<6 pF	<9 pF	8 pF	<9 pF	<9 pF
I_{OL}	100 mA	40 mA	100 mA	50 mA	100 mA
Maximum power consumption per output driver	100 mW	16 mW	40 mW	20 mW	55 mW
Minimum line impedance for point-to-point connection	11 Ω	20 Ω	11 Ω	19 Ω	9.5 Ω
Minimum line-impedance bus system	22 Ω	40 Ω	22 Ω	38 Ω	19 Ω
Precharge for line insertion	Yes	No	Yes	Yes	Yes
Overshoot-protection circuit	No	No	No	Yes	Yes
Edge-rate control (ERC)	No	No	Yes	Yes	Yes
Bus hold (A port)	No	Yes	Yes	Yes	Yes
Backplane switching characteristics in data sheet	No	No	No	Yes	Yes
Operational frequency on the backplane	≤30 MHz	≤40 MHz	~100 MHz	~100 MHz	~100 MHz

† Features 5-V tolerance at A port

The individual characteristics of the SN74GTLPH1655 are discussed in detail in the following sections.

Features of the SN74GTLPH1655

Functional Description: SN74GTLPH1655 – UBT

The SN74GTLPH1655 is described as a UBT, i.e., a bus driver for a wide variety of applications.

The function of this component can be controlled and changed in accordance with the signals and static voltage levels applied to the various control inputs.

By means of the control inputs OE, $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$, LEAB, and LEBA, one of the following three operating modes for the SN74GTLPH1655 can be selected:

- Transparent mode

  The SN74GTLPH1655 behaves like a bidirectional bus driver, for example, the ’245.

- Level-sensitive storage (latch) mode

  The SN74GTLPH1655 behaves like a level-sensitive register (latch), for example, a ’373. However, in this case, it can be used bidirectionally.

- Edge-triggered storage (flip-flop) mode

  The circuit behaves like an edge-triggered register, for example, a ’374. In this mode, it can be used bidirectionally.

The operating mode can be set separately for each direction of transmission. An example of a typical application is shown in Figure 12.

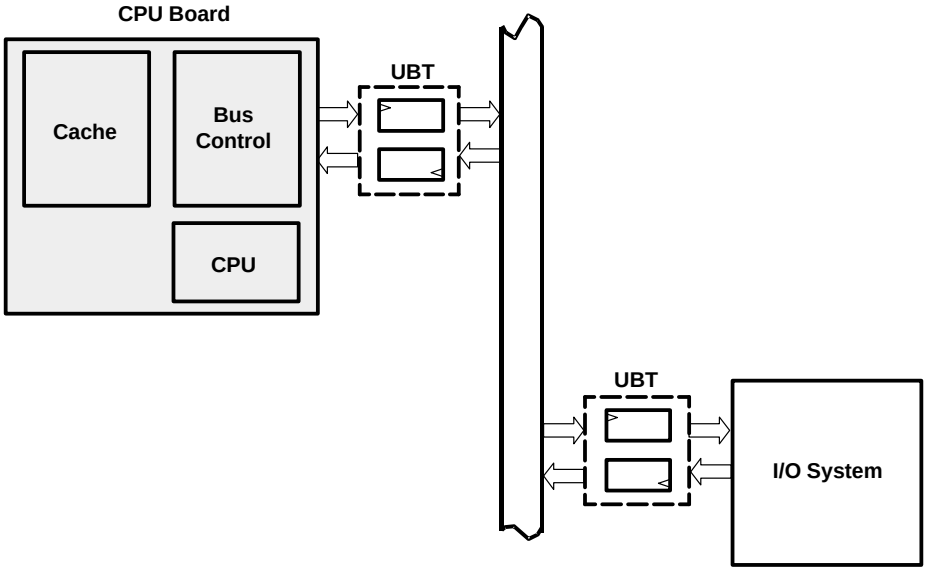

Figure 12. Typical Bus Application for a UBT

SN74GTLPH1655: Link Between a GTLP Backplane and an LVTTL Module

The SN74GTLPH1655 converts LVTTL-level signals (A port) into GTL- or GTLP-level signals (B port), and *vice versa*. The user decides, by choosing the termination voltage and the reference voltage, which level will be provided on the B-port side (see Table 6). The A port is, in every case, compatible with LVTTL.

This conversion is useful when continuing to work with LVTTL levels on the module, while the GTL and GTLP levels, specially developed for this application, are transmitted on the backplane. The low-voltage TTL and GTLP signal levels are shown in Figure 13. The SN74GTLPH1655 needs 3.3 V as the operating voltage.

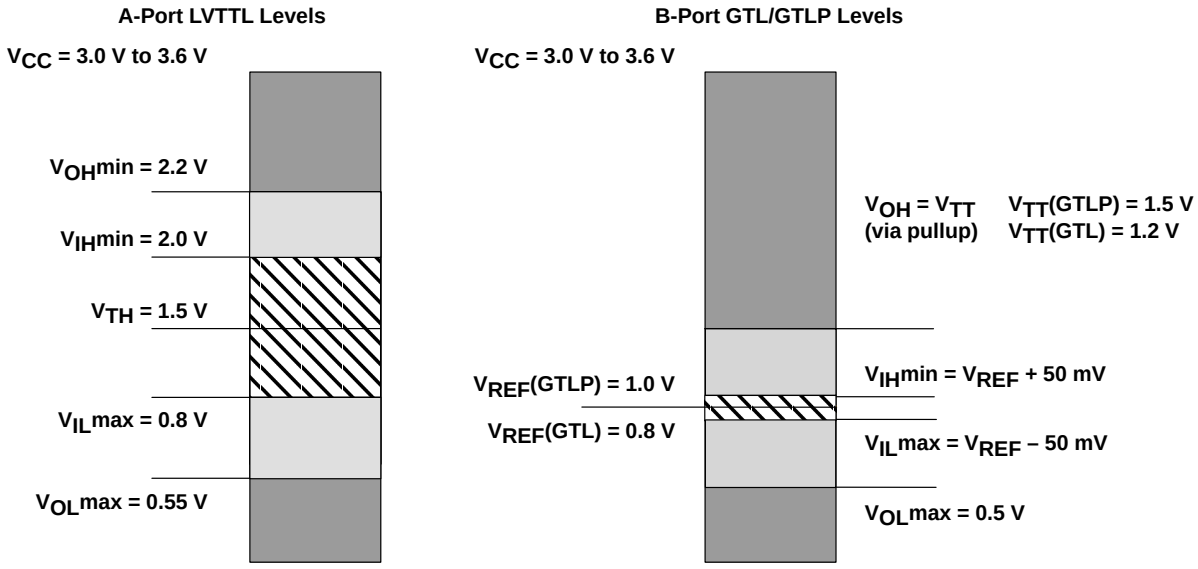

Figure 13. LVTTL and GTLP Signal Levels of SN74GTLPH1655

Table 6. Choice of GTL/GTLP Level (Using V_{TT} and V_{REF})

LEVEL		MIN	TYP	MAX	UNIT
GTL	V_{TT}	1.14	1.2	1.26	V
	V_{REF}	0.74	0.8	0.87	
GTLP	V_{TT}	1.35	1.5	1.65	V
	V_{REF}	0.87	1	1.1	

Termination Voltage, V_{TT}

There are various rules and techniques regarding proper line termination that should be observed for a successful development using SN74GTLPH1655.

The termination voltage (V_{TT}) should be derived from a voltage regulator. The current requirements, e.g., up to 100 mA per output, must be observed. There are various voltage regulators available that meet these requirements. Depending on the application, the regulators should be situated either directly on the backplane or on the module boards connected to it.

If several signal lines are switched simultaneously, considerable current fluctuations may occur at the termination voltage. For this reason, bypass capacitors should be provided close to the termination resistors (Figure 14).

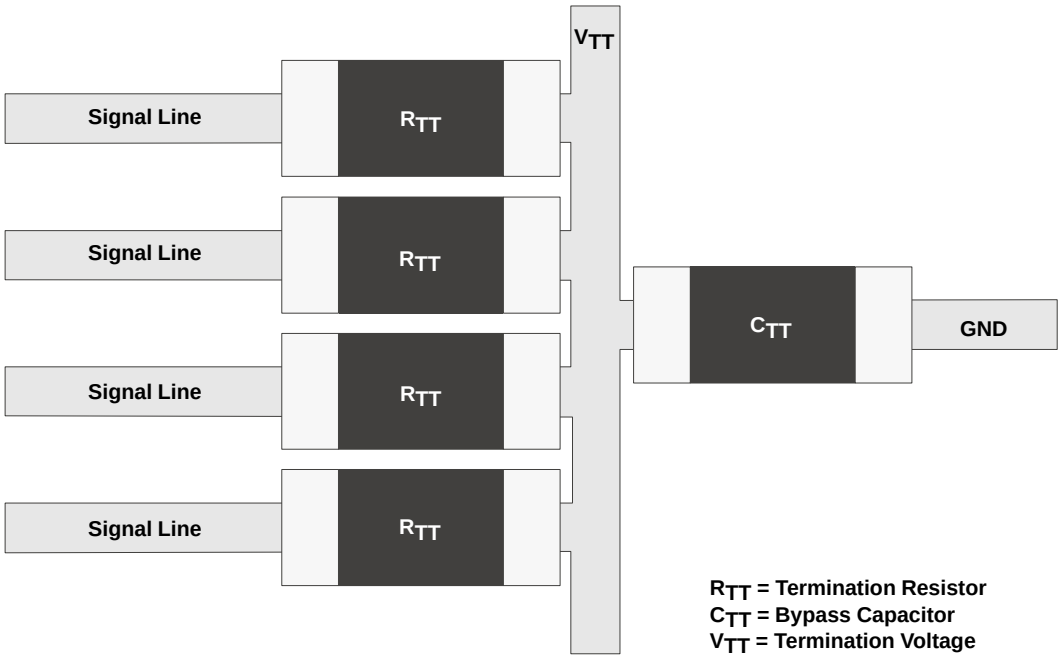

Figure 14. Proposed Layout of Termination Resistors and Bypass Capacitor on a Circuit Board

Since the bypass capacitor should have the lowest possible inductance, it is recommended that ceramic capacitors in surface-mount packages be used. The value of capacitance can be calculated from Equation 6.

$$C = I\frac{\Delta t}{\Delta U} \tag{6}$$

I = 50 mA — For bidirectional lines with a termination resistor at both ends of each line, a maximum of one-half the output current of an SN74GTLPH1655 (I_O = 100 mA) can flow through one of the two termination resistors.

ΔU = 10 mV — In this example, the collapse of the termination voltage V_{TT} must not exceed 10 mV.

Δt = 4 ns — The collapse of the termination voltage V_{TT} should be postponed for at least 4 ns.

$$C = I\frac{\Delta t}{\Delta U} = 50\ mA \times \frac{4\ ns}{10\ mV} = 20\ nF \tag{7}$$

If 82-nF ceramic capacitors are used, a bypass capacitor should be provided for every four signal lines. A proposed layout for the four termination resistors and the bypass capacitor on a circuit board is shown in Figure 14.

Reference Voltage, V_{REF}

The GTL or GTLP reference voltage (V_{REF}) can be derived, using a simple voltage divider and a bypass capacitor (0.01 μF to 0.1 μF), from the termination voltage. The circuit shown in Figure 15 has the advantage that V_{REF} follows voltage fluctuations of the termination voltage, V_{TT}. In this way, the maximum possible signal-to-noise ratio (SNR) always is ensured, even with an unstable termination voltage. Since only a very small current (maximum 10 μA) flows in the V_{REF} pin of the SN74GTLPH1655, the pin can be connected to the voltage divider without adversely affecting the GTL/GTLP reference voltage.

Ensure that the bypass capacitor is placed as close as possible to the V_{REF} pin of the SN74GTLPH1655.

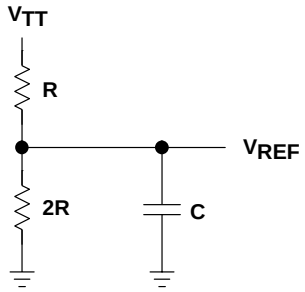

Figure 15. Suggested Connection of V_{REF} Pin

Static Characteristics of the SN74GTLPH1655

An understanding of the static characteristics of a component is necessary for a circuit development to be successful. The input and output characteristics of the SN74GTLPH1655 were, therefore, measured under laboratory conditions.

Input Characteristics

In principle, the input characteristics appear identical on both sides (A and B ports) of the device.

In Figure 16, the input protection diode easily is recognized; it is found both at the inputs of the LVTTL side (A port) and also at the inputs of the GTLP side (B port) of the device. The diode circuit provides protection against high negative-voltage spikes, which can occur as the result of electrostatic discharges or line reflections. In such cases, the diode conducts and prevents more-sensitive components from being destroyed.

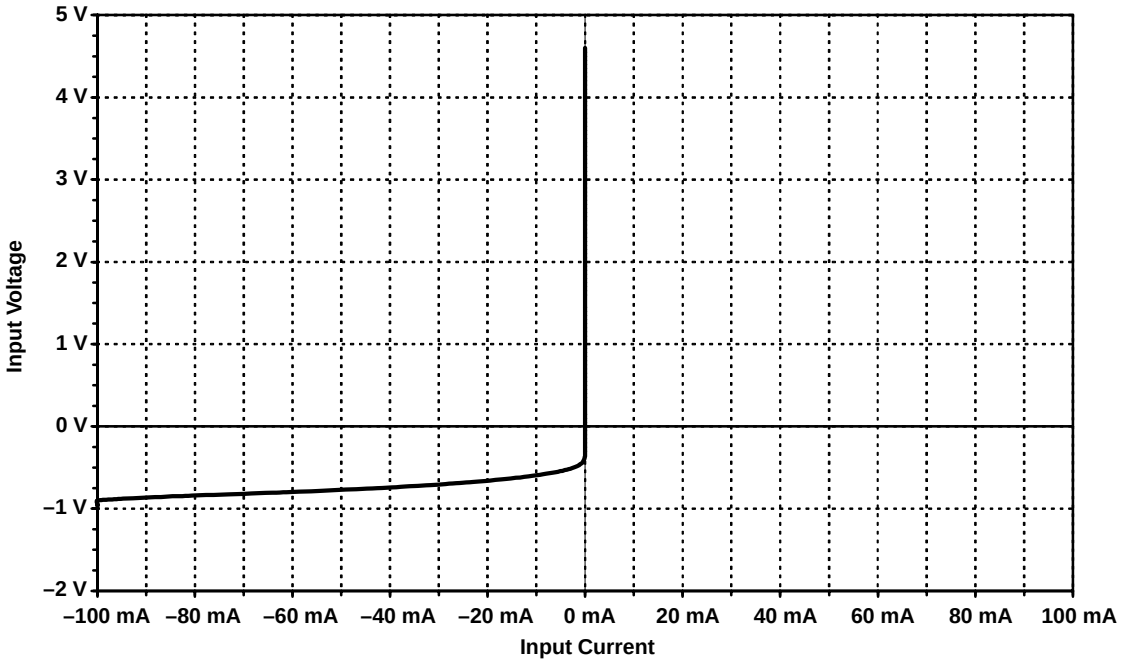

Figure 16. Input Characteristics of SN74GTLPH1655

Bus-Hold Circuit

If the input characteristics of the LVTTL side (A port) are recorded in small increments, and over a narrow range of current, the curve shown in Figure 17 results. This curve clearly demonstrates the effectiveness of the bus-hold circuit.

To change the logic state stored by the bus-hold circuit, a current of about 250 μA must be overridden.

This circuit is useful when, for example, all drivers on the bus are in a high-impedance state. Thus, an undefined state can be prevented.

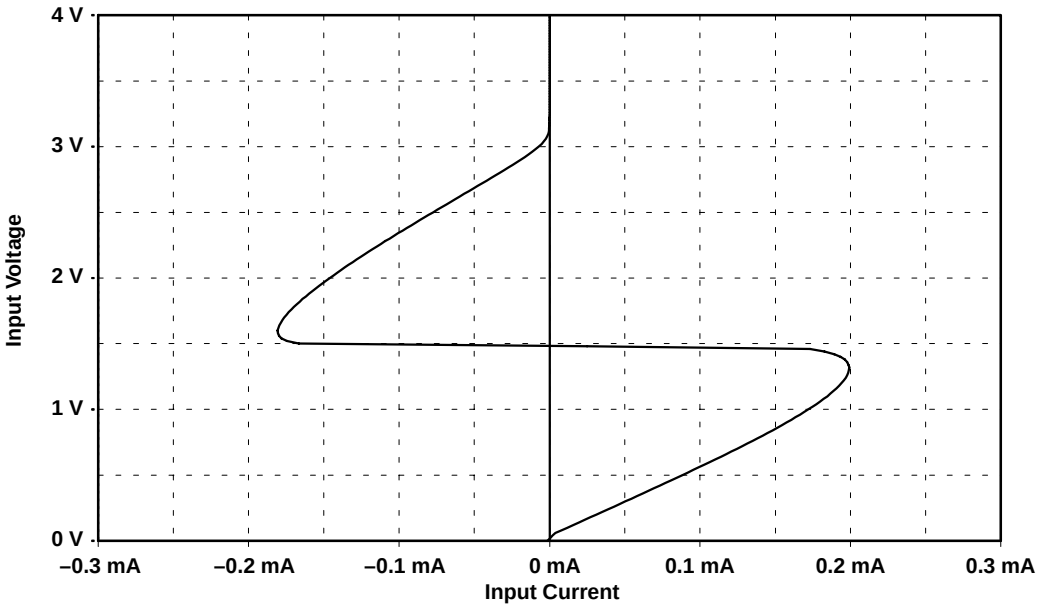

Figure 17. Bus-Hold Characteristics at LVTTL Input of SN74GTLPH1655

There is no bus-hold circuit on the GTLP side (B port). A bus-hold circuit on the GTLP side would defeat the principle of operation of the open-drain outputs, which take on the high-impedance state to allow the bus to achieve a logic high state (via the pullup resistors).

GTLP Output Characteristics

Because the SN74GTLPH1655 has been conceived as an interface between LVTTL partial systems and a GTLP backplane, the output characteristics of both sides are shown here. The characteristics for the various logic states of the output stage are shown in a single voltage-current diagram.

The principle of the GTLP bus is based on open-drain drivers, as shown in Figure 18.

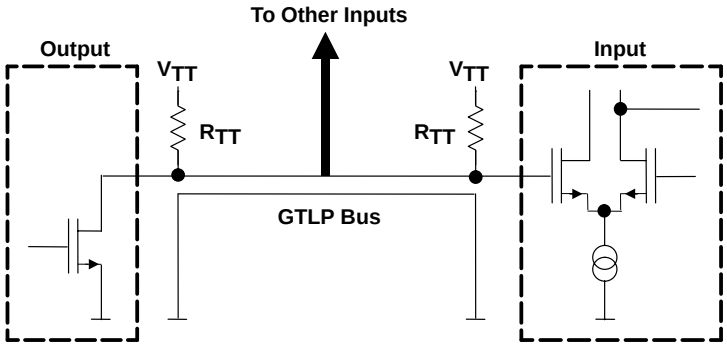

Figure 18. GTLP Bus: An Open-Drain Bus

The device actively drives only the low state on the bus; whereas, for the high state, the required current flows directly from the termination voltage source, V_{TT}. The current is limited only by a pullup resistor (R_{TT}), which usually is of very low resistance. According to the specification, the pullup resistor must be not less than the minimum value of 22 Ω. A primary purpose of resistor R_{TT} is to provide an optimum termination of the bus to avoid line reflections (see *Transmission-Line Theory in Practice*).

Figure 19 shows that in the low state, the output resistance of the GTLP output stage is in the range of about 4 Ω.

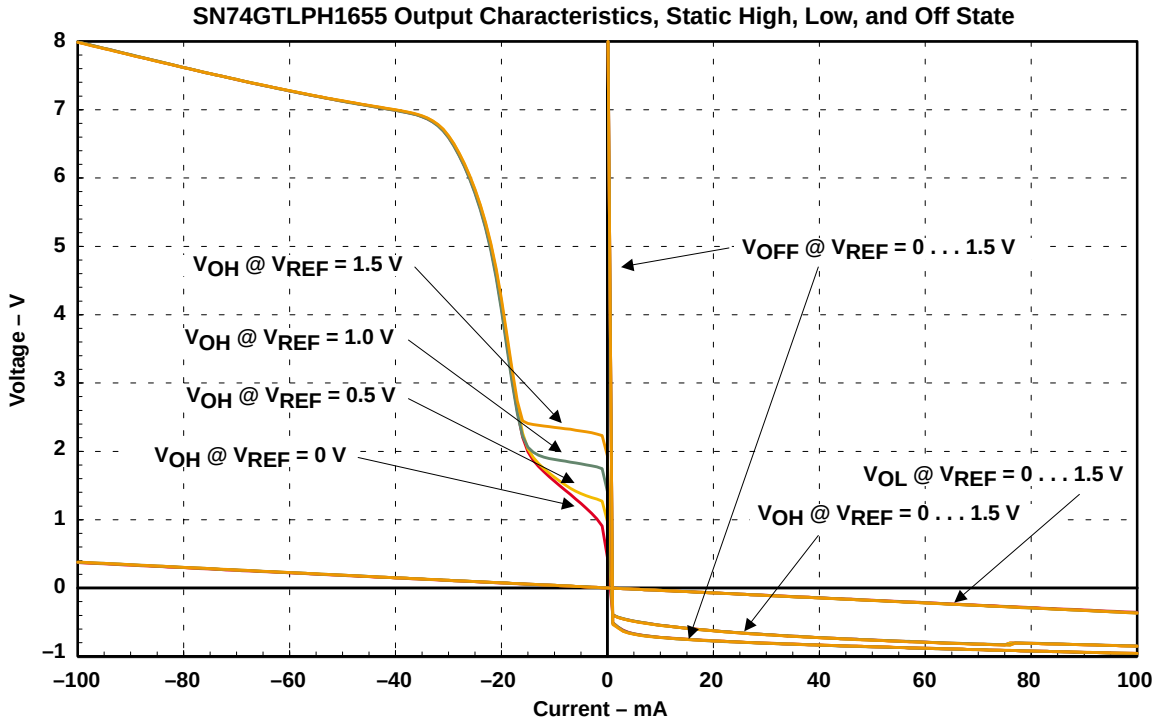

Figure 19. Output Characteristics of GTLP Port of SN74GTLPH1655

In the high state, the output transistor is blocking up to V_{REF} + one diode forward voltage. Thus, the output is at a very high resistance, as shown in Figure 19. Above V_{REF} + 0.7 V, a low resistive part follows, and then a high-resistive section, up to 7 V. Above 7 V, the curve again shows diode behavior. The special curve of output characteristics is caused by implementation of the TI-OPC into the GTLP outputs.

Because of the bidirectionality of the SN74GTLPH1655, the input protection diode also can be seen at the output during off state (for V_{CC} = 0 V) and 3-state. The outputs and inputs of the device are connected together and routed to a single pin.

LVTTL Output Characteristics

The output characteristics of the LVTTL output side of the SN74GTLPH1655 are shown in Figure 20, recorded with a supply voltage V_{CC} = 3.3 V. The output resistance for the low state is around 10 Ω, and in the case of the high state, a value of about 25 Ω is typical.

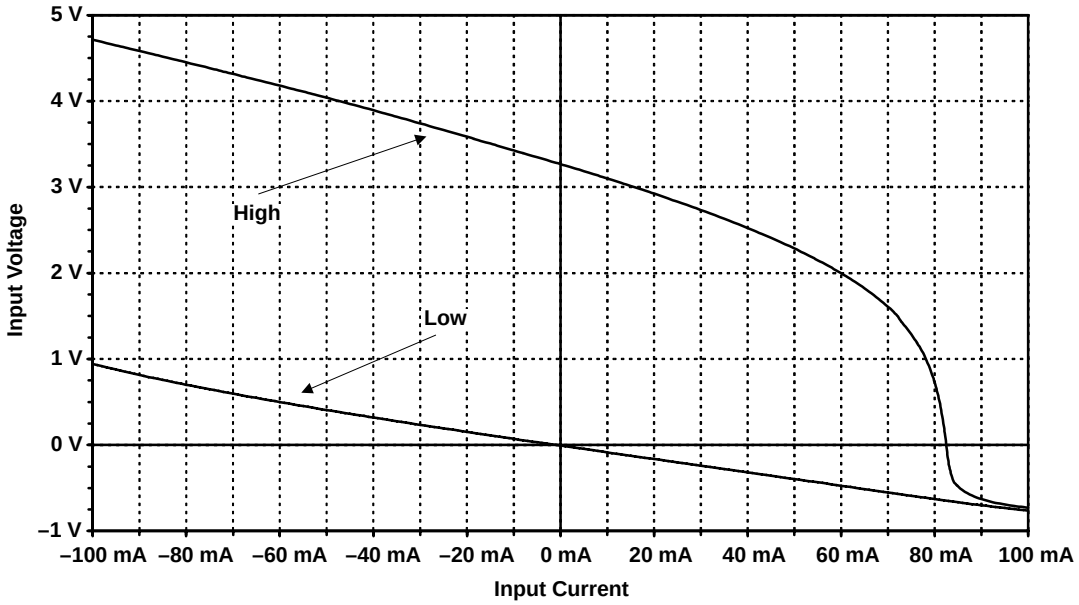

Figure 20. Output Characteristics of LVTTL Side of SN74GTLPH1655

TI-OPC Circuitry

TI-OPC circuitry is a new feature of the GTLP backplane family.

This circuit improves signal integrity by using a control circuit that compares the output voltage at the GTLP port with the reference voltage. The principle is shown in Figure 21.

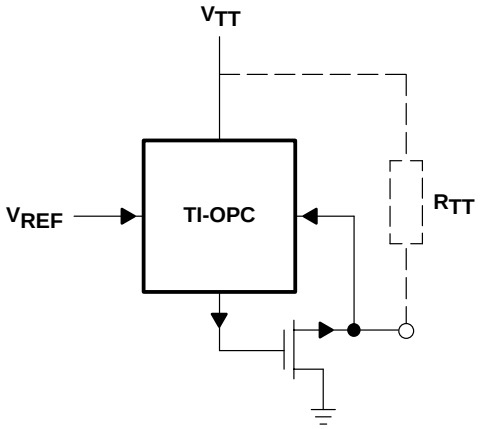

Figure 21. TI-OPC Circuitry Replacement of GTLP

If the output voltage exceeds about one diode forward voltage referred to the reference voltage, the TI-OPC circuitry limits currents below about 14 mA to the voltage to $V_{REF} + V_{diode}$. If this output current is exceeded, the output resistance increases again rapidly (compare to Figure 19).

Edge-Rate Control (ERC)

In the GTLP output stage, a circuit is included that allows two different values of edge rate to be set. With the use of the ERC input pin, different rise and fall times can be set, allowing the optimum configuration under various loading conditions of the backplane. If the SN74GTLPH1655 ERC is connected to the supply voltage (V_{CC}), the GTLP outputs are switched with longer rise and fall times than when it is connected to GND. Some GTLP devices have the $\overline{\text{ERC}}$ feature, which is the opposite of ERC. If $\overline{\text{ERC}}$ is connected to GND, the GTLP outputs are switched with a longer rise and fall time.

In two series of measurements, the voltage at the control input ERC was varied to determine the influence of the ERC circuit on the behavior of the signal.

As shown in Figure 22, the measurements on the SN74GTLPH1655 were made with a single device under no-load conditions, using GTLP voltage levels. During the measurement, only the 25-Ω pullup resistor was at the GTLP output. There were LVTTL signals from a signal generator at the A port of the device, each having different rise and fall times: t_r, t_f = 2 ns and t_r, t_f = 10 ns.

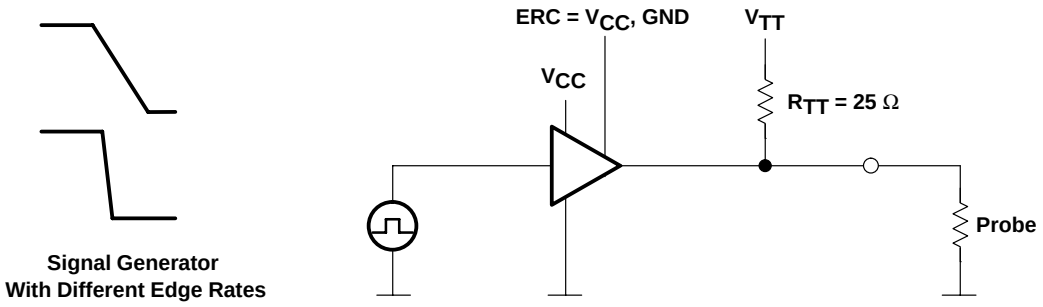

Figure 22. Setup for Measuring Edge Rate at GTLP Side of SN74GTLPH1655

Additional measurement results on the SN74GTLPH1655 test board are presented in a later section, which explains the behavior with a bus under realistic conditions.

The measurement results for falling edges are shown in Figures 23 and 24; Figures 25 and 26 show the curves for rising edges.

Using the definition of edge rate (slew rate) $dV/dt = (V_{OH} – V_{OL})/t_r$, t_f, a slew rate results in 0.2 V/ns for slow edge rate (ERC = V_{CC}) and 0.35 V/ns for fast edge rate (ERC = GND). As a comparison, these values are significantly less than those of standard TTL devices, which are usually about 1 V/ns, or more.

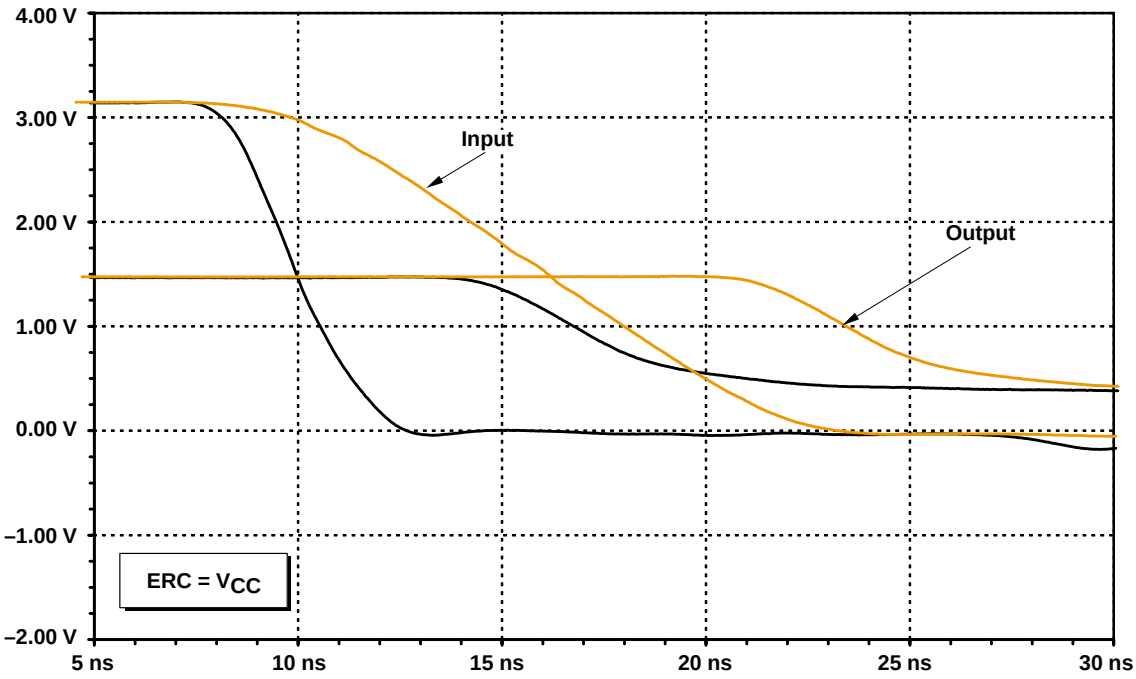

Figure 23. Falling Edge, ERC = V_{CC} (Slow Edges), Input Signals t_f = 2 ns, 10 ns

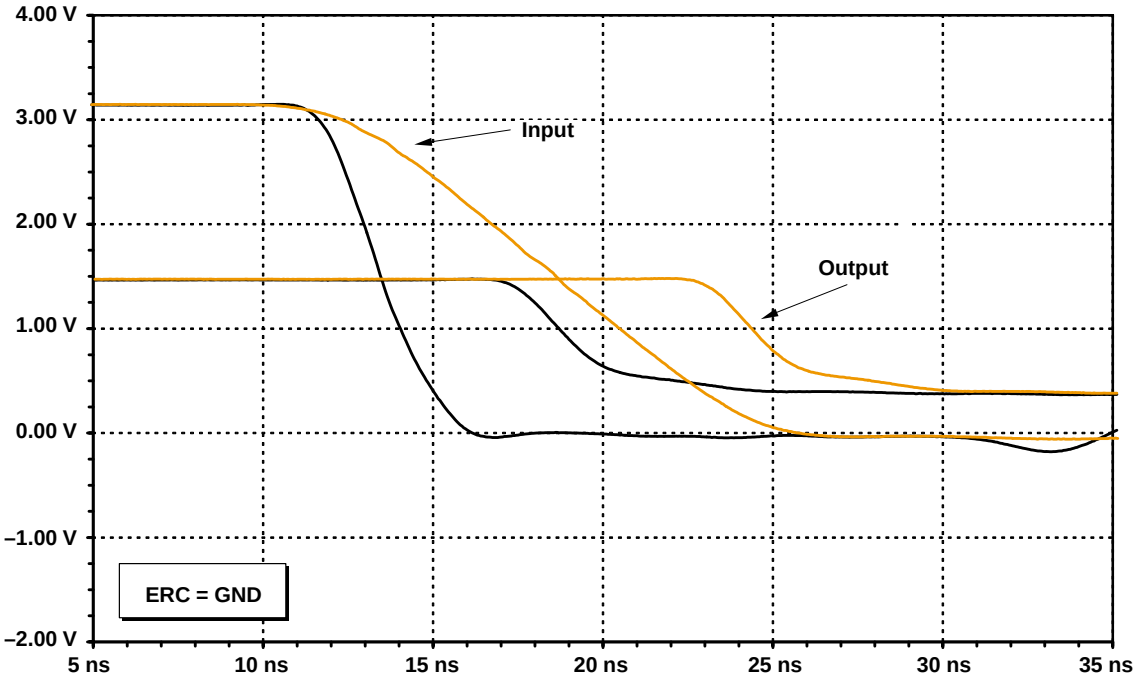

Figure 24. Falling Edge, ERC = GND (Fast Edges), Input Signals t_f = 2 ns, 10 ns

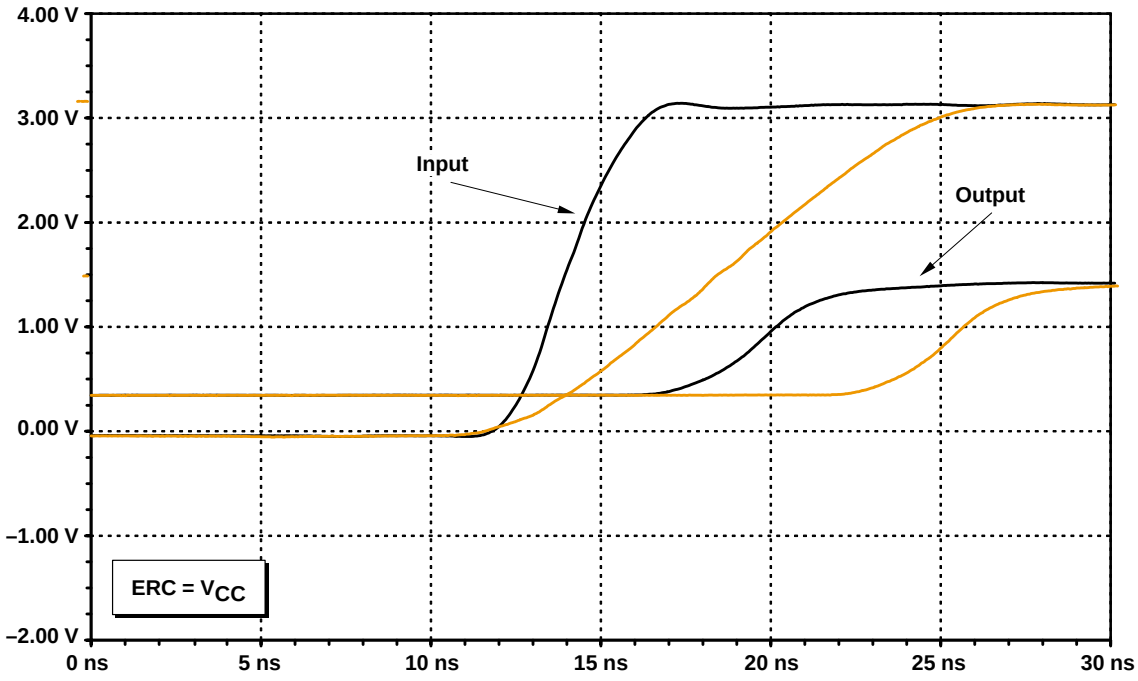

Figure 25. Rising Edge, ERC = V_{CC} (Slow Edges), Input Signals t_r = 2 ns, 10 ns

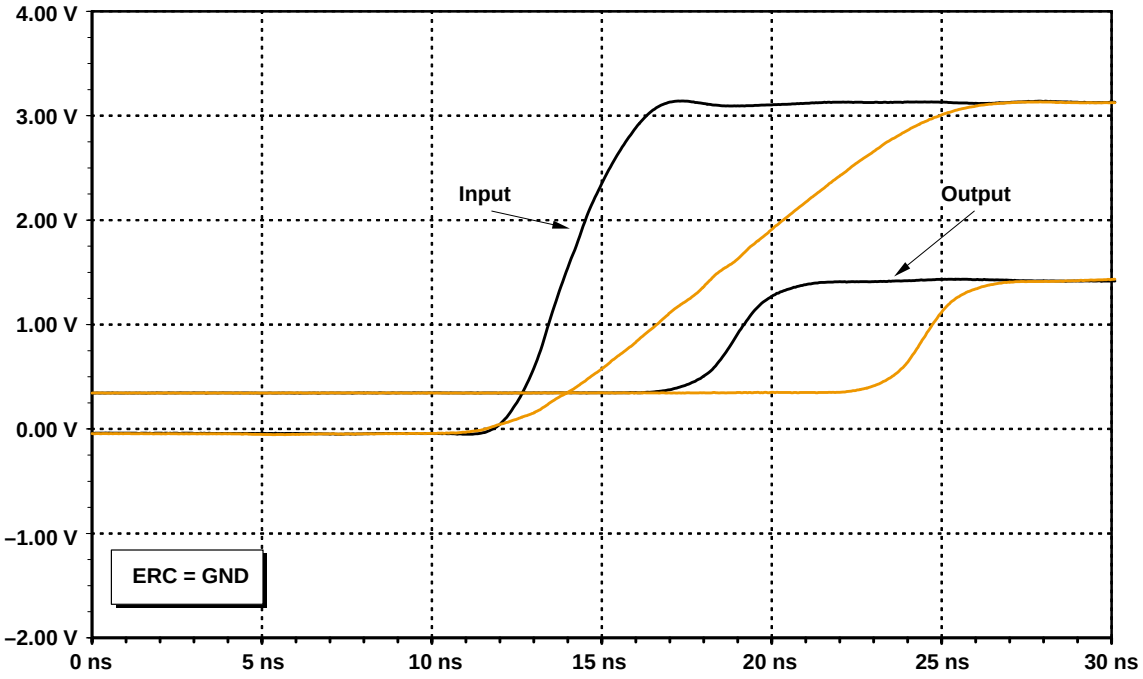

Figure 26. Rising Edge, ERC = GND (Fast Edges), Input Signals t_r = 2 ns, 10 ns

Removal and Insertion Under Voltage and Partially Switched-Off Systems

If it is possible to remove and reinsert plug-in boards in a system while it remains in operation (live insertion), special precautions must be taken with the signal lines.

- The outputs of the boards to be inserted or removed must be at a high impedance when the boards are inserted or removed.
- Before inserting a board, all pins must be charged to the threshold voltage (1.5 V with TTL-compatible systems, or V_{CC}/2 with CMOS-compatible systems). Thus, destructive voltage spikes on the signal line in excess of the threshold voltage range, which might otherwise corrupt the data on the bus, can be avoided.

Figure 27 shows this principle. The data pins are charged to the switching threshold (V_{TH}). As a maximum, the switching threshold can be reached when inserting; however, it no longer can be exceeded as a result of a voltage spike.

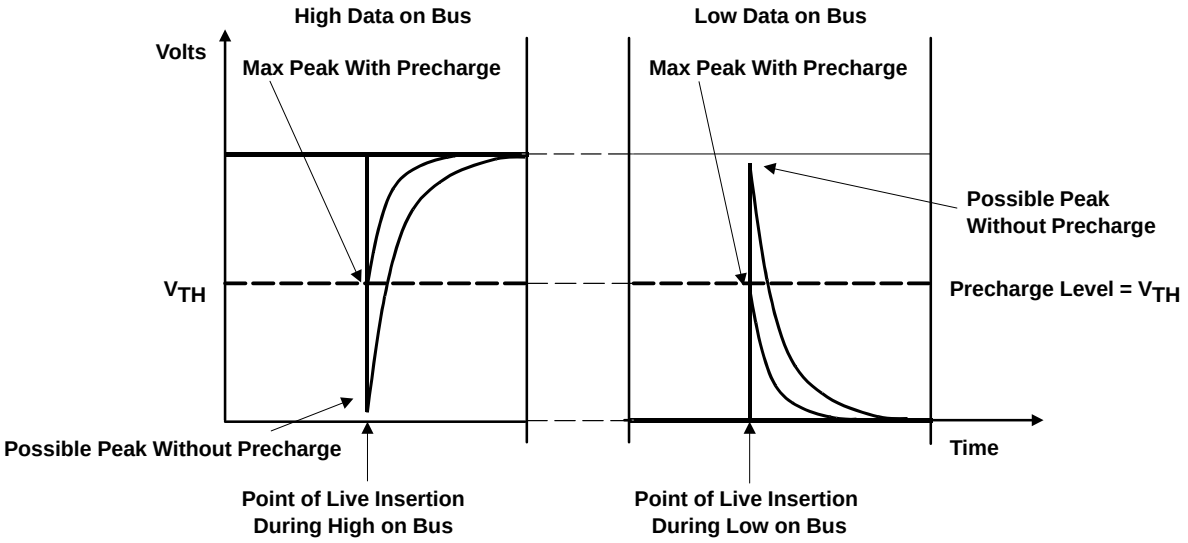

Figure 27. Influence of Precharge Function on Bus Signal

The SN74GTLPH1655 has the characteristics discussed above, which are necessary for the successful development of a live-insertion application.

Using the OE control input, it is possible to set the outputs of the SN74GTLPH1655 on both sides simultaneously to a high-resistance state. As a result of the integrated power-up 3-state circuit, the device is definitely inactive at a V_{CC} of less than 1.5 V.

To ensure that there is also a definite high-resistance state at a supply voltage between 1.5 V and the operating voltage, it is recommended that OE be connected to V_{CC} via a pullup resistor.

High-impedance outputs can be precharged to a definite voltage level by means of the precharge circuitry (BIAS V_{CC}). Disturbances to the active bus arising from insertion (charging/discharging of the I/O capacitance) will thus be kept to a minimum.

In a similar fashion, in modern applications, particular parts of a system are switched off from the source of power without having first removed them from the complete system. This is a partial switching off of the system, or a partial power down.

If a device is used in a partial power-down application, the inputs and outputs for V_{CC} = 0 V must be at high impedance, and thus be able to tolerate active bus signals.

The property of being partial-power-down compatible is reflected in the parameter I_{OFF}, which specifies the maximum leakage current in an input or output.

I_{OFF} is defined as:

- The device is disconnected from the operating voltage (V_{CC} = 0 V), and
- A logic level is applied to the input or output.

With the SN74GTLPH1655, the maximum value of I_{OFF} is 100 μA.

Refer to the TI application report *Live Insertion,* literature number SDYA012, which discusses this subject in detail.

Measurements on GTLPH1655 Test Board

A GTLPH1655 test board has been constructed to examine the characteristics of the SN74GTLPH1655 in a practical application. The principle of this board is shown in Figure 28.

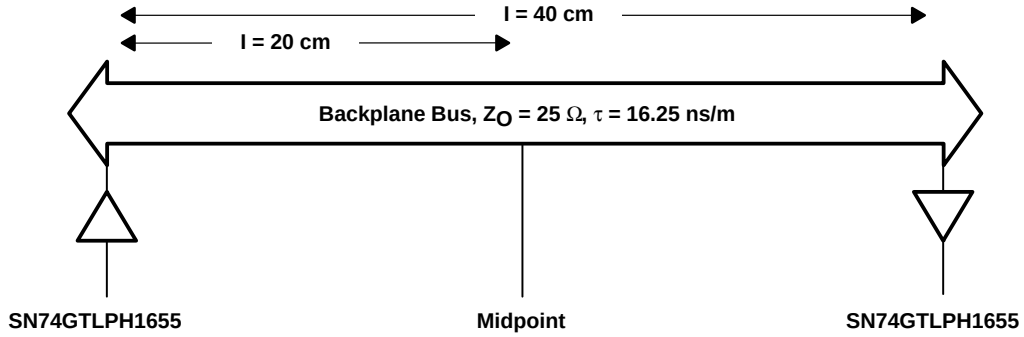

Figure 28. Principle of Construction of GTLP Bus on GTLPH1655 Test Board

This bus consists of a straight connecting line, 40 cm long, between two SN74GTLPH1655 devices.

In practice, a backplane wiring system provides the option for multiple plug-in modules. The bus impedance is reduced as a result of the additional input capacitances of the modules that are connected to it (see Figure 2). This effect can be approximated by connecting capacitors between the bus line and ground at intervals of 2 cm.

Both sides of the bus are provided with termination resistors that are connected to V_{TT}. The termination voltage is set at 1.5 V. A 1-V reference voltage (V_{REF}) was chosen. In this way, GTLP signals are transmitted on the bus.

The termination resistors for this setup were chosen to match the line impedance, which, for a fully loaded backplane, results in Z_O = 25 Ω. This case provides optimum line termination, with a reflection factor very close to ρ = 0.

For the measurements, the slew rate of the GTLP output stage was varied by means of the edge-rate control input ERC. The measurements were carried out under two different bus conditions: a fully loaded bus (with distributed capacitors) and the bus unloaded (without capacitors). The clock frequencies used were 10 MHz, 50 MHz, and 160 MHz, the last being close to the maximum value of 175 MHz specified in the data sheet.

For the case of a fully loaded bus, the result is a line impedance of about 25 Ω, and a delay time on the line of about 7 ns.

With the bus unloaded, i.e., operated without capacitors connected to it, the line impedance is about 30 Ω, and the delay time on the line reaches a value below 3 ns.

The measurement results presented in Figures 29 through 52 show:

- The LVTTL input signal of the SN74GTLPH1655 that drives the bus line, together with the LVTTL output signal of the SN74GTLPH1655 receiver that is situated at the end of the GTLP bus. For this, the load of the receiver was varied. The diagrams show the curves for $R_L = \infty$ (unloaded output) and for $R_L = 50\ \Omega$.
- Waveforms on the GTLP bus line:
  - GTLP output signal of the SN74GTLPH1655 that drives the bus line, i.e., the signal at the beginning of the line
  - Bus signal in the middle of the GTLP bus
  - Signal at the end of the GTLP bus line, which also is applied to the input of the SN74GTLPH1655 receiver device.

All curves are shown together for the frequencies 10 MHz, 50 MHz, and 160 MHz, and for the two different edge-rate settings (with ERC = V_{CC} and ERC = GND).

For these measurements, care was taken to ensure that the timing relationships between them remained constant. A summary of the measurement results is given in Table 7.

Table 7. Measurement Results on SN74GTLPH1655 Demonstration Board

	SIGNAL	BUS LINE UNLOADED (WITHOUT CAPACITORS)		BUS LINE LOADED (WITH CAPACITORS)	
		SLOW EDGE RATE ERC = V_{CC}	FAST EDGE RATE ERC = GND	SLOW EDGE RATE ERC = V_{CC}	FAST EDGE RATE ERC = GND
f = 10 MHz	I/O LVTTL level	Figure 29	Figure 31	Figure 41	Figure 43
	Beginning, middle, end of GTLP bus	Figure 30	Figure 32	Figure 42	Figure 44
f = 50 MHz	I/O LVTTL level	Figure 33	Figure 35	Figure 45	Figure 47
	Beginning, middle, end of GTLP bus	Figure 34	Figure 36	Figure 46	Figure 48
f =160 MHz	I/O LVTTL level	Figure 37	Figure 39	Figure 49	Figure 51
	Beginning, middle, end of GTLP bus	Figure 38	Figure 40	Figure 50	Figure 52

Measurement Results With an Unloaded Backplane (Z_O = 30 Ω, R_{TT} = 25 Ω)

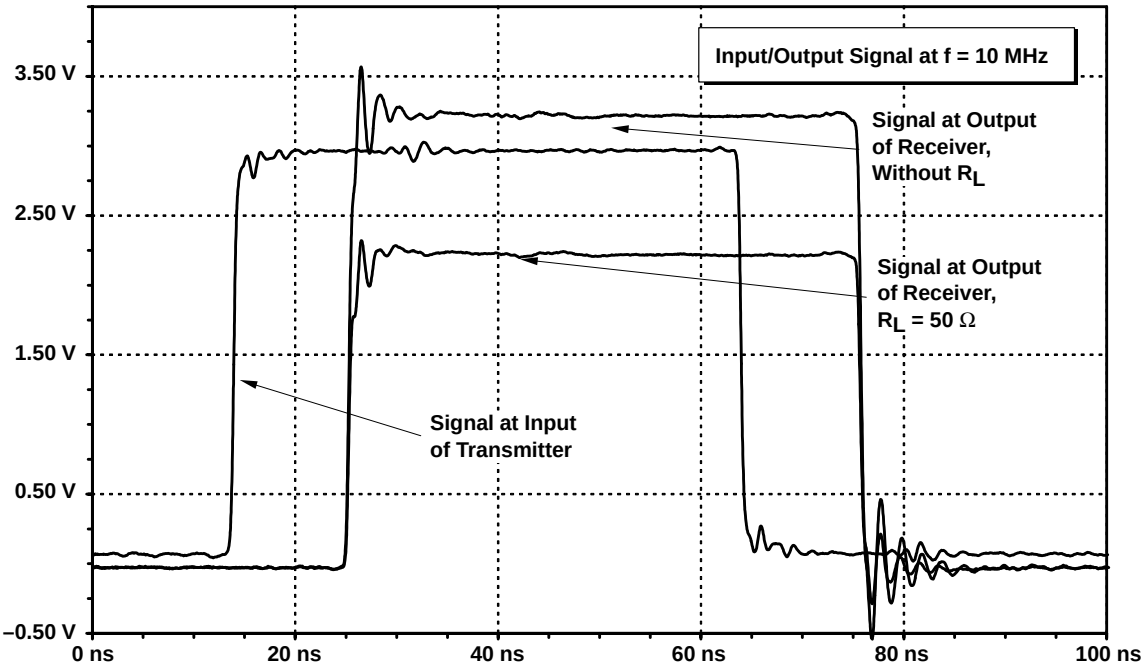

Figure 29. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 10 MHz

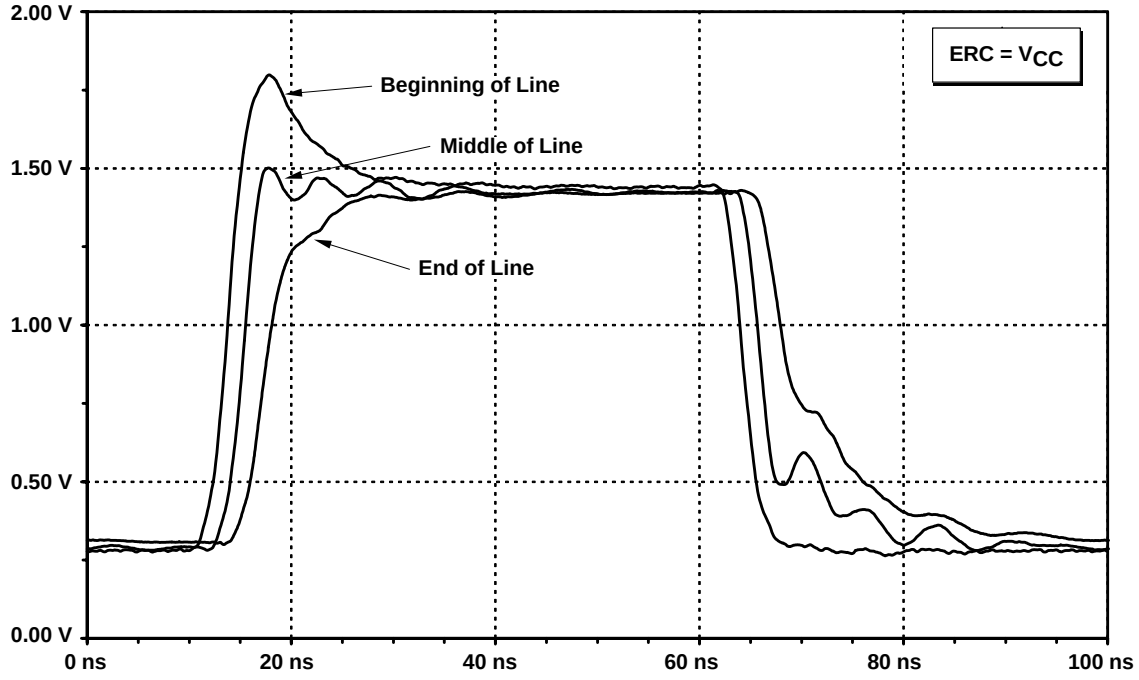

Figure 30. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 10 MHz

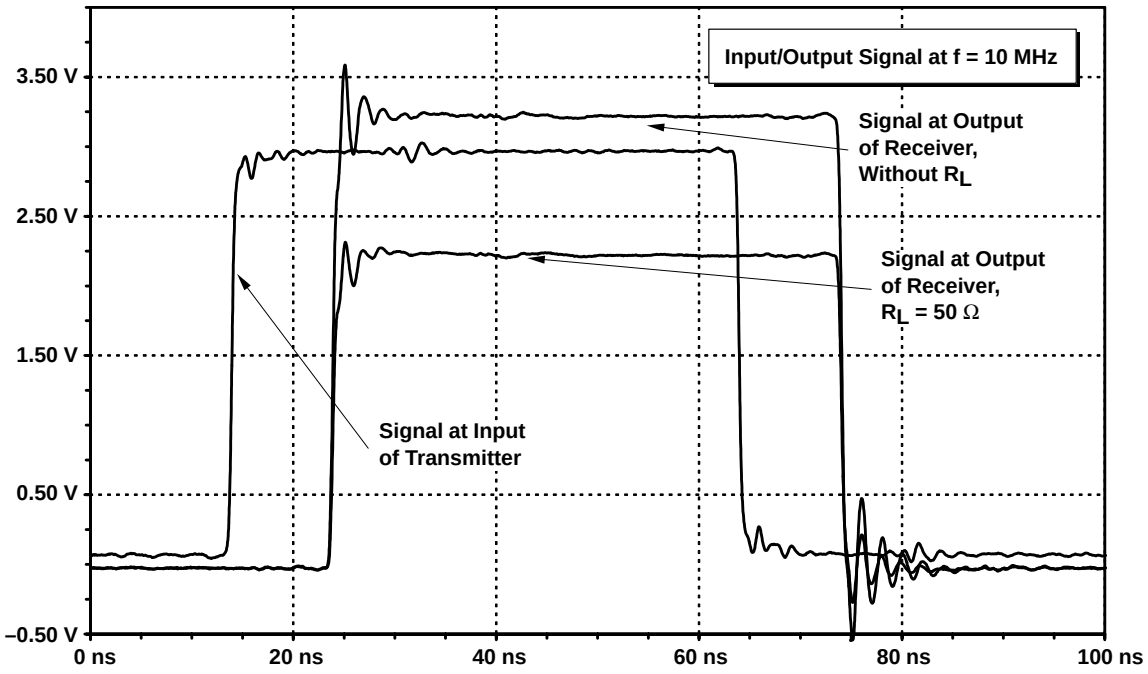

Figure 31. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 10 MHz

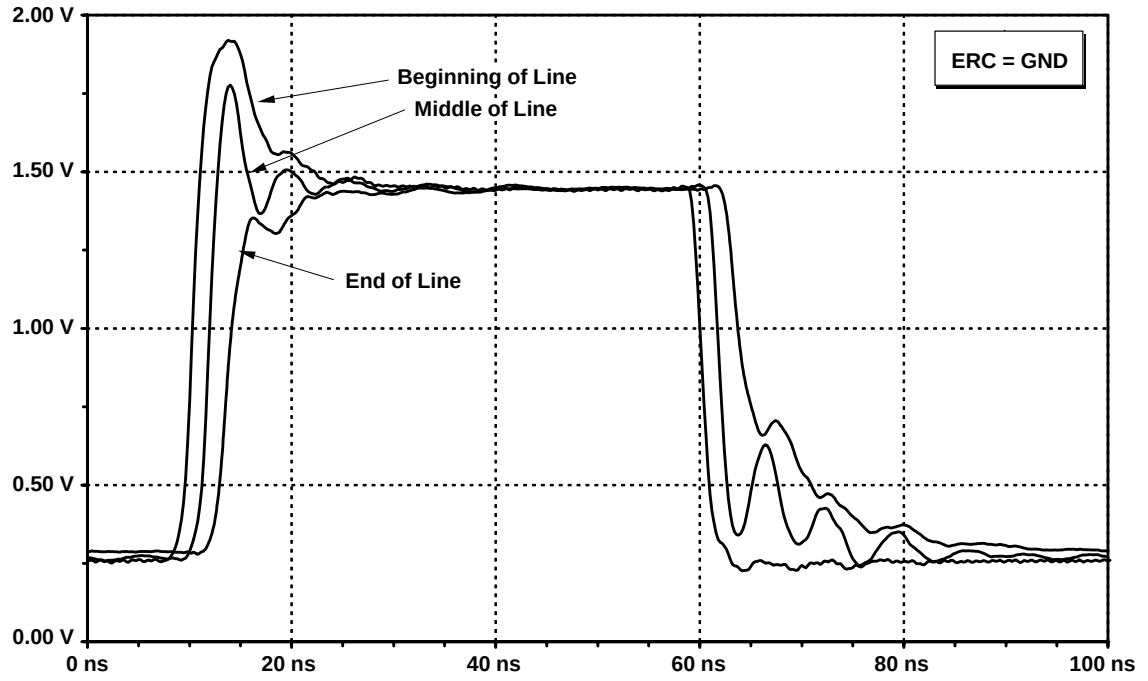

Figure 32. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 10 MHz

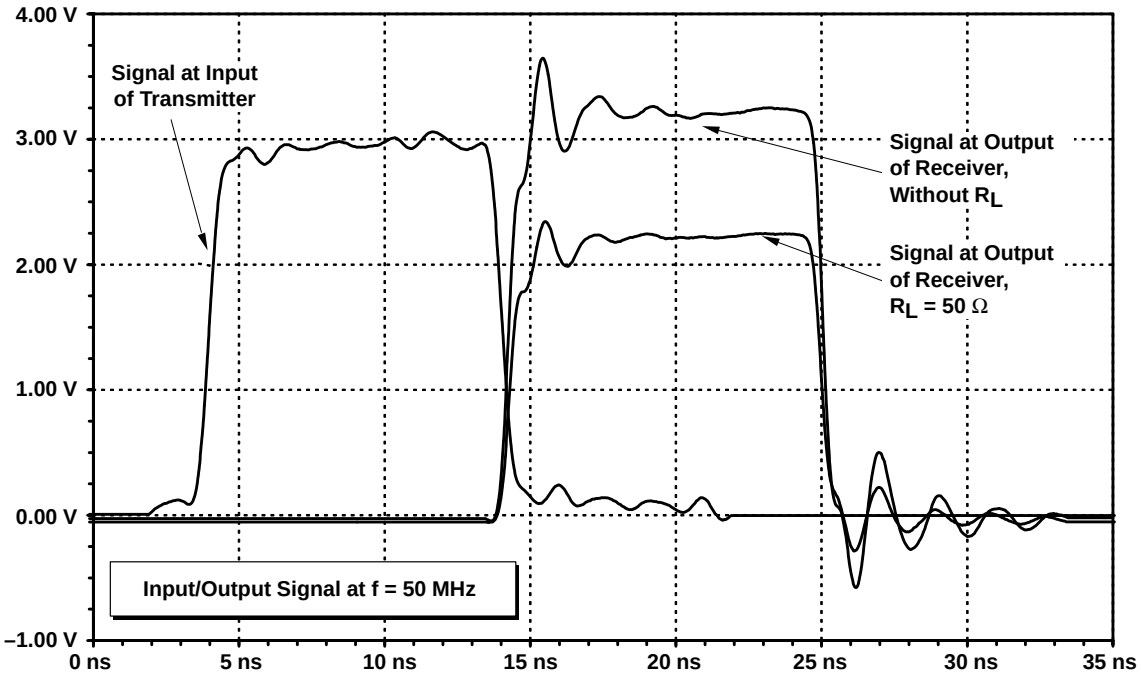

Figure 33. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 50 MHz

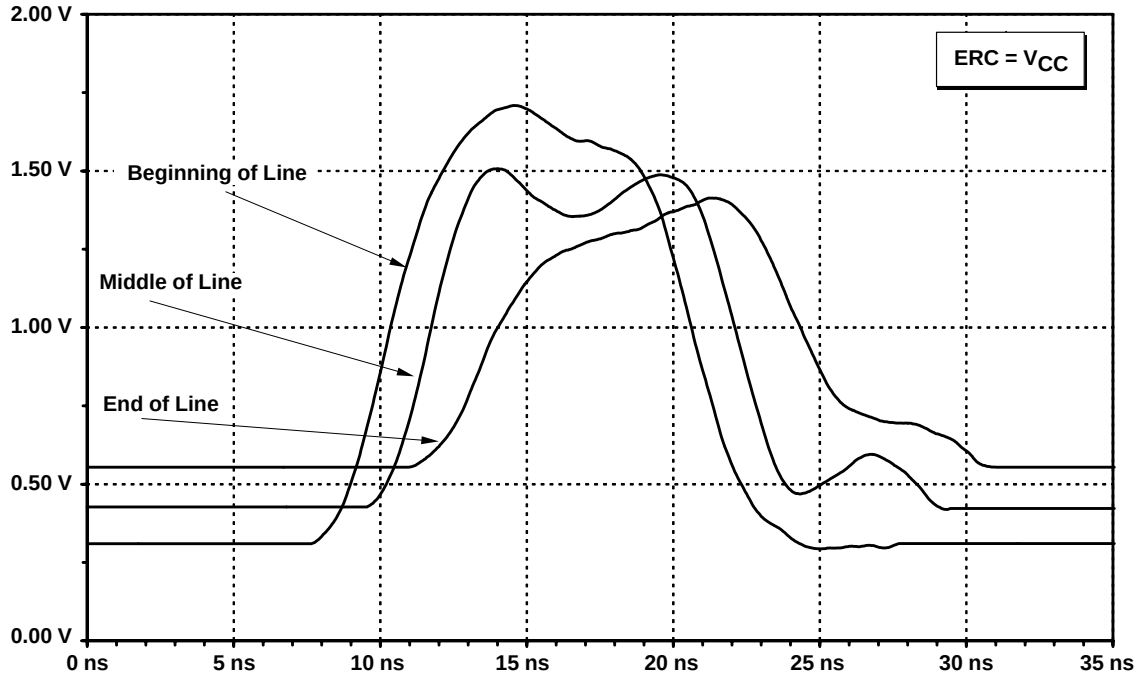

Figure 34. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 50 MHz

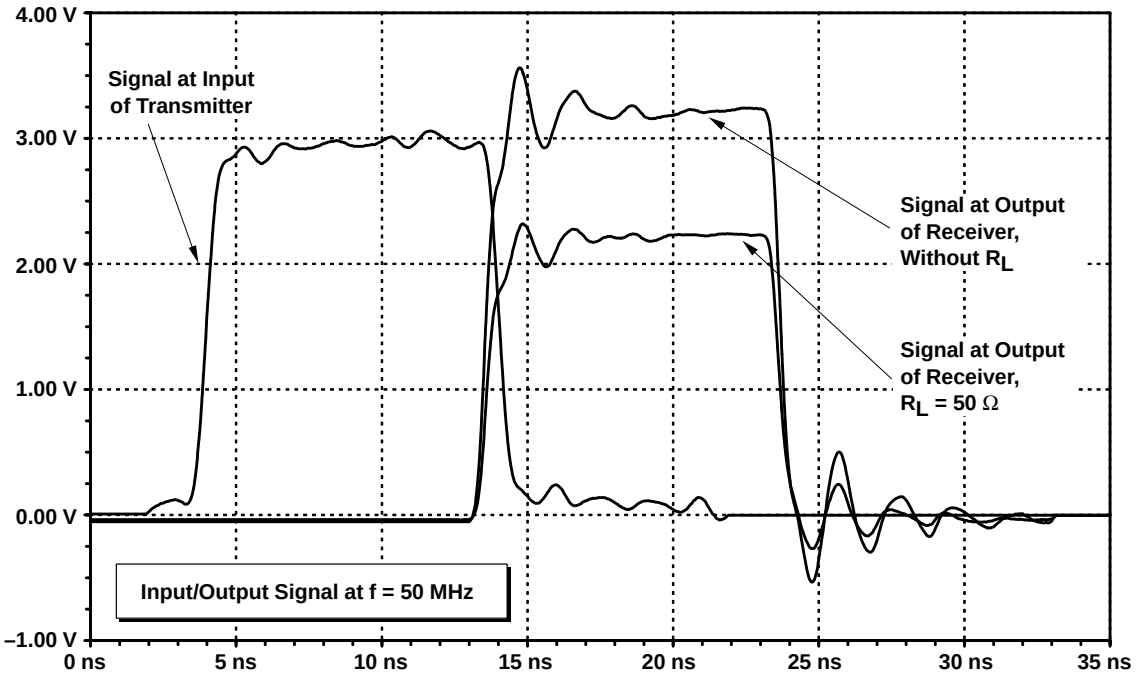

Figure 35. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 50 MHz

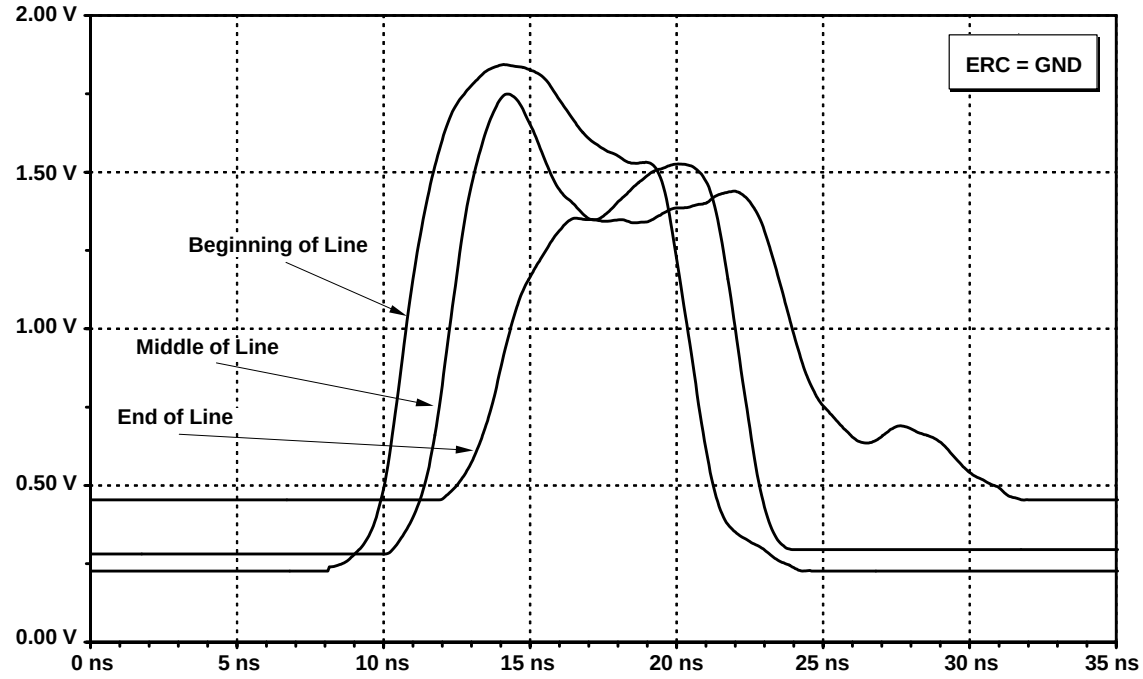

Figure 36. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 50 MHz

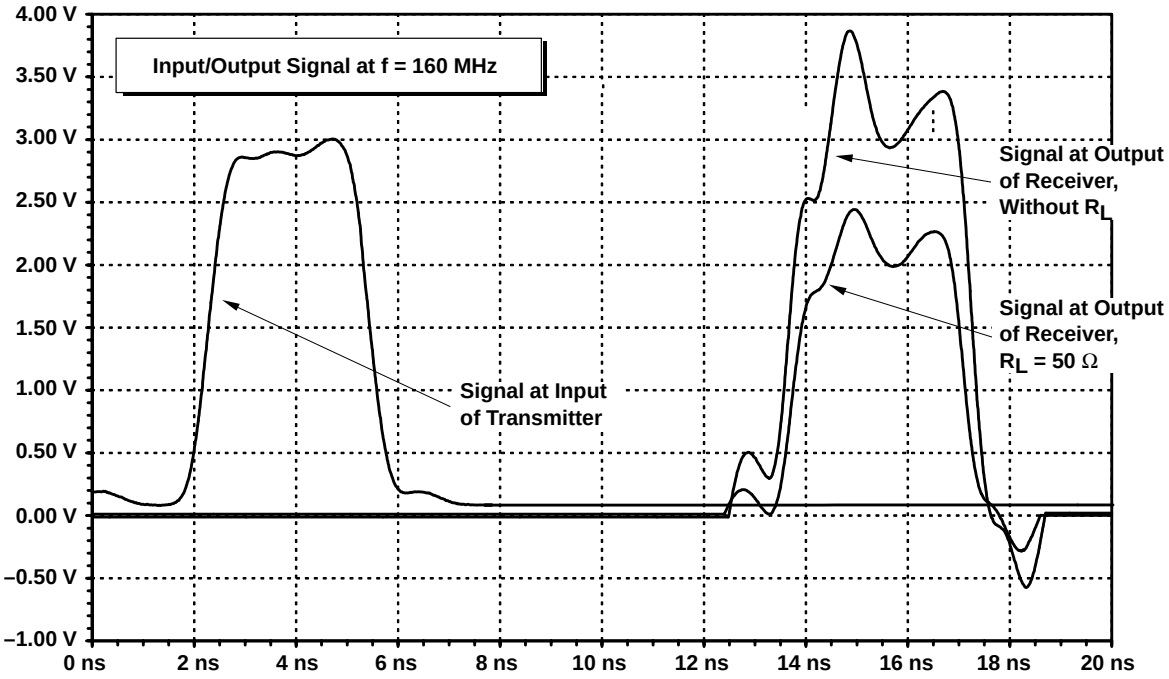

Figure 37. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 160 MHz

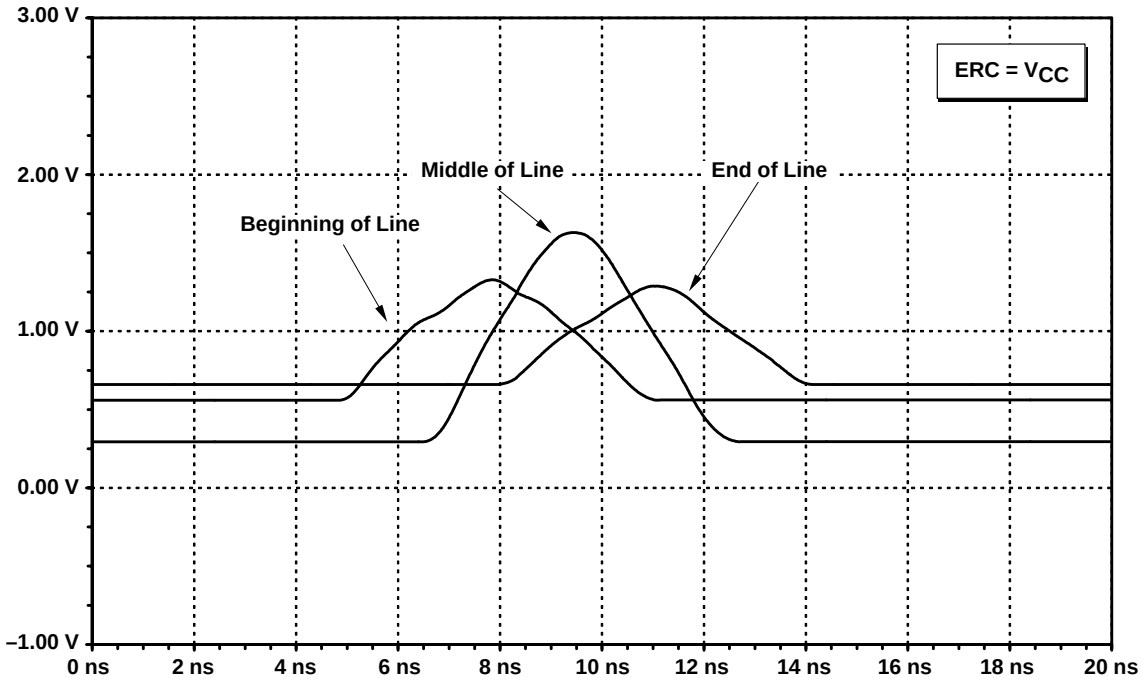

Figure 38. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 160 MHz

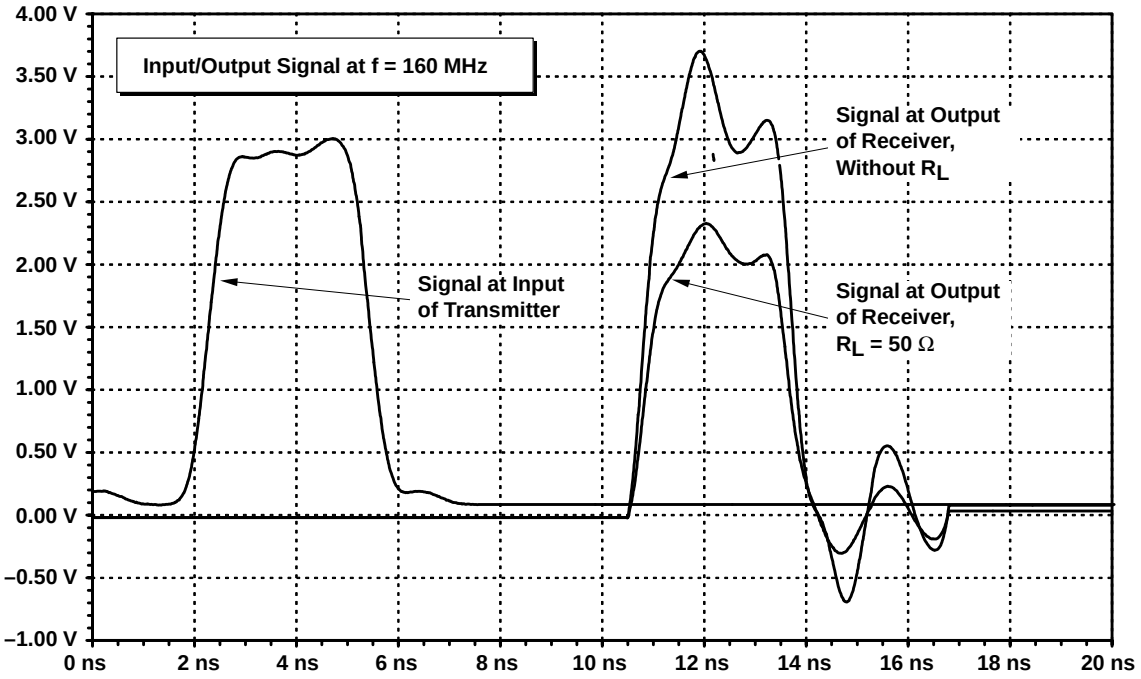

Figure 39. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 160 MHz

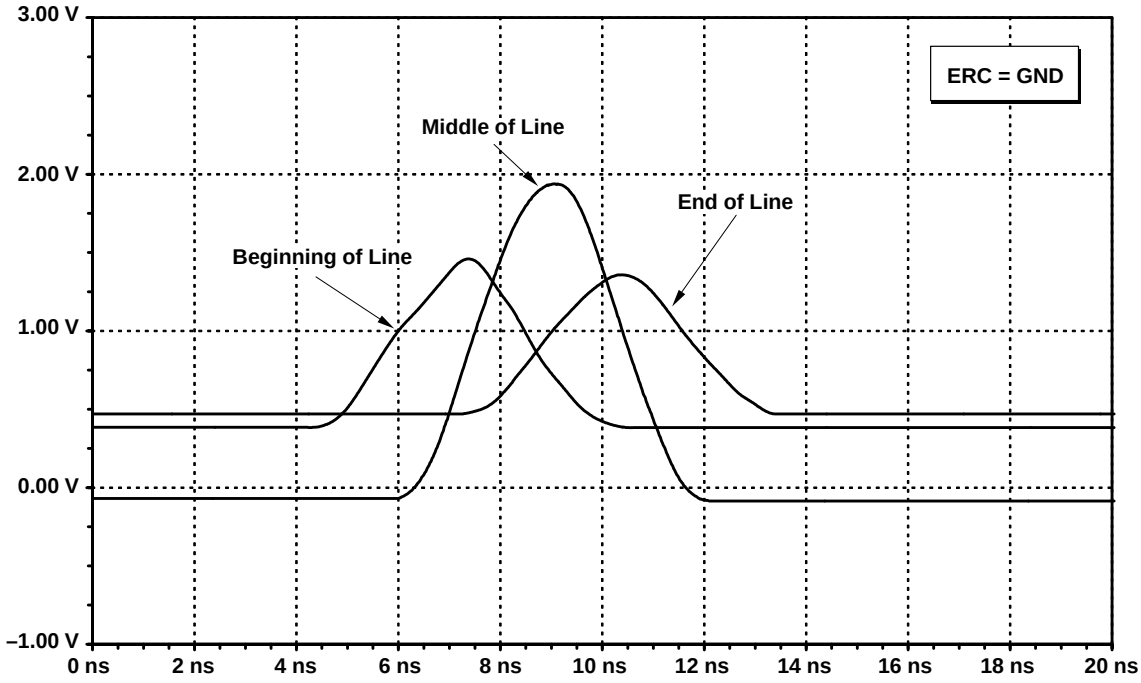

Figure 40. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 160 MHz

Measurement Results With a Loaded Backplane (Z_O = 25 Ω, R_{TT} = 25 Ω)

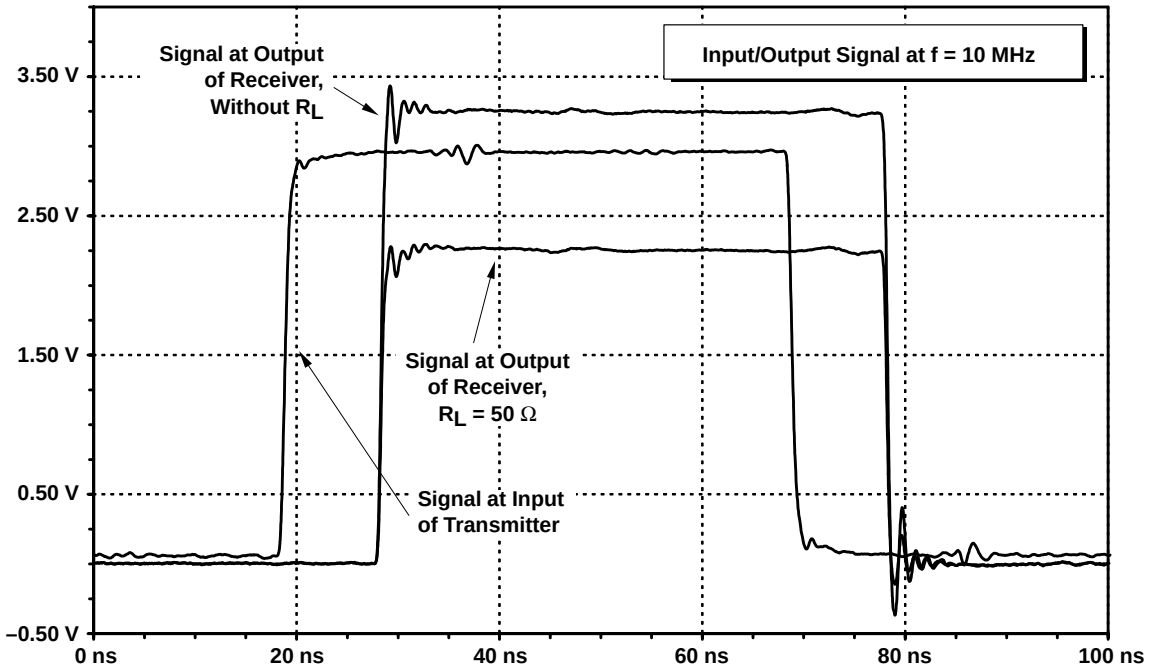

Figure 41. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 10 MHz

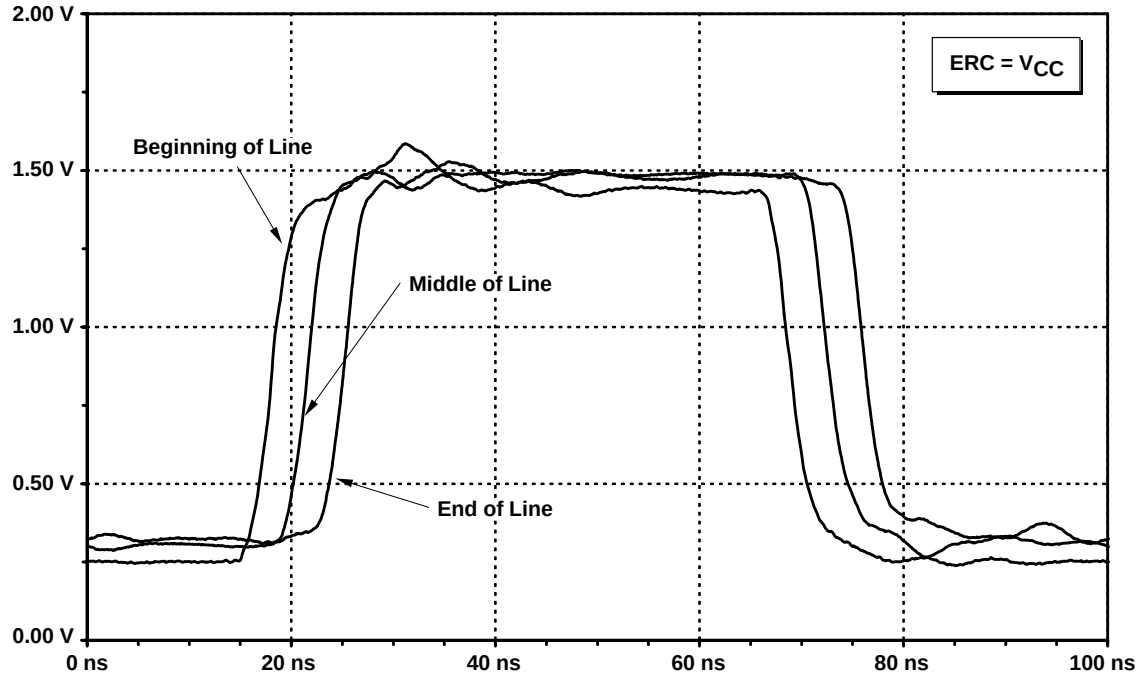

Figure 42. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 10 MHz

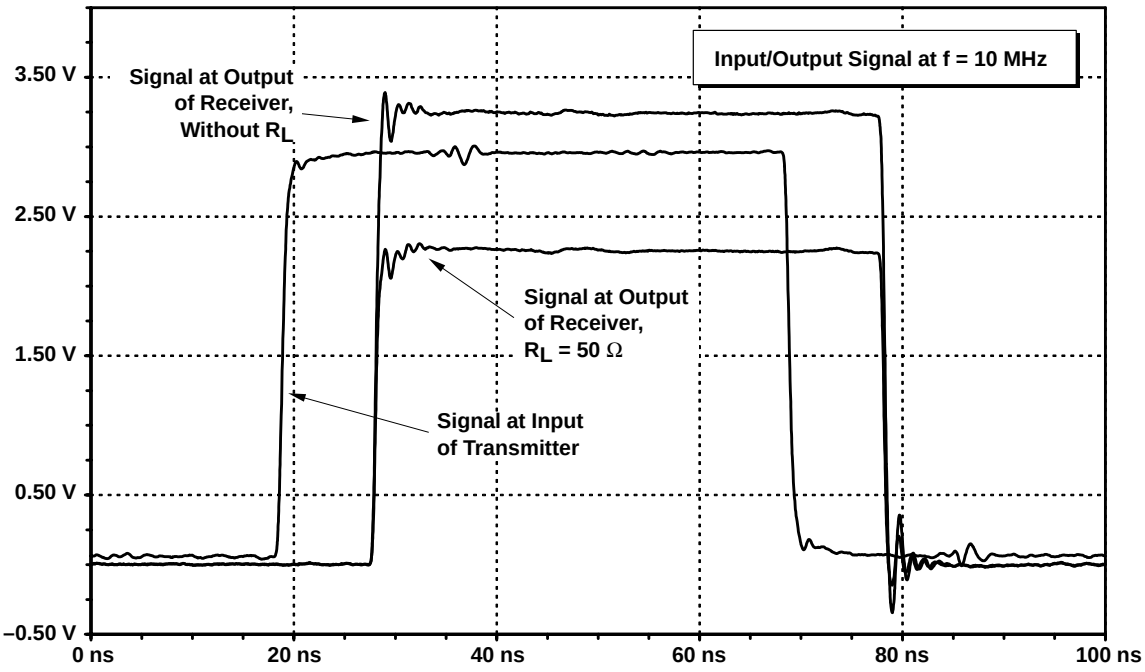

Figure 43. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 10 MHz

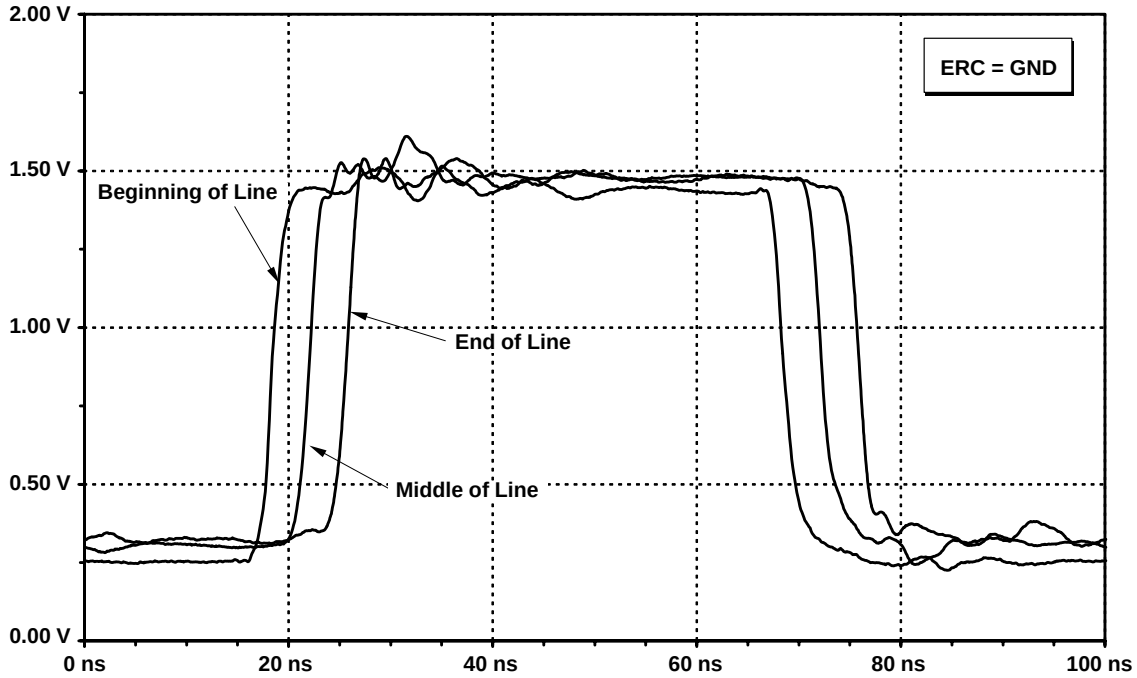

Figure 44. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 10 MHz

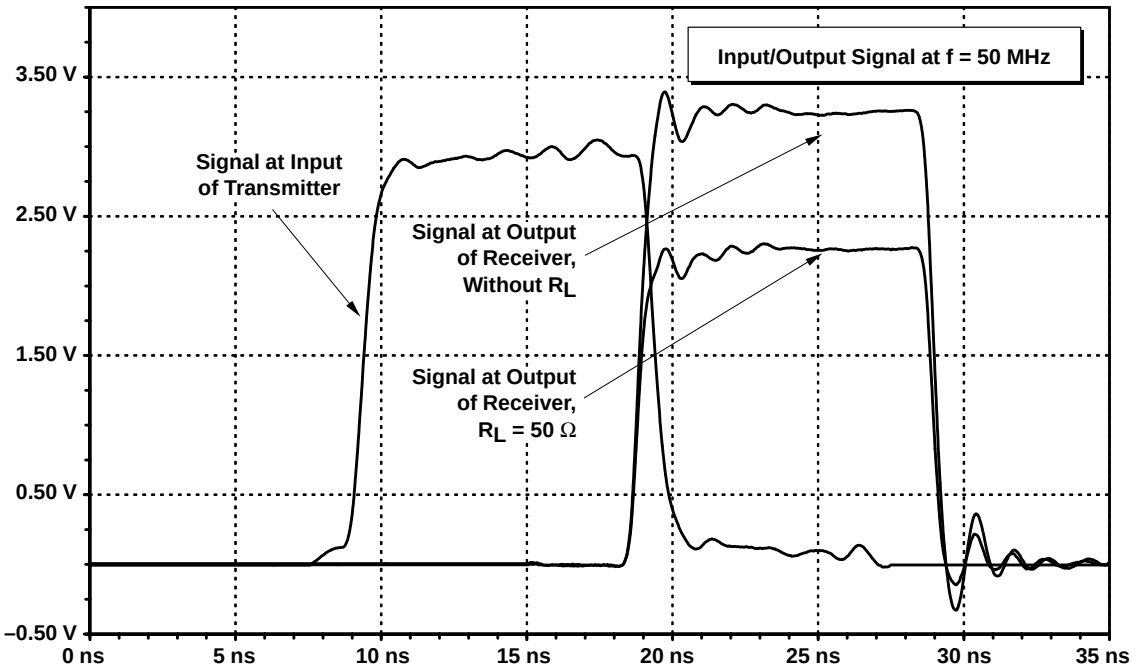

Figure 45. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 50 MHz

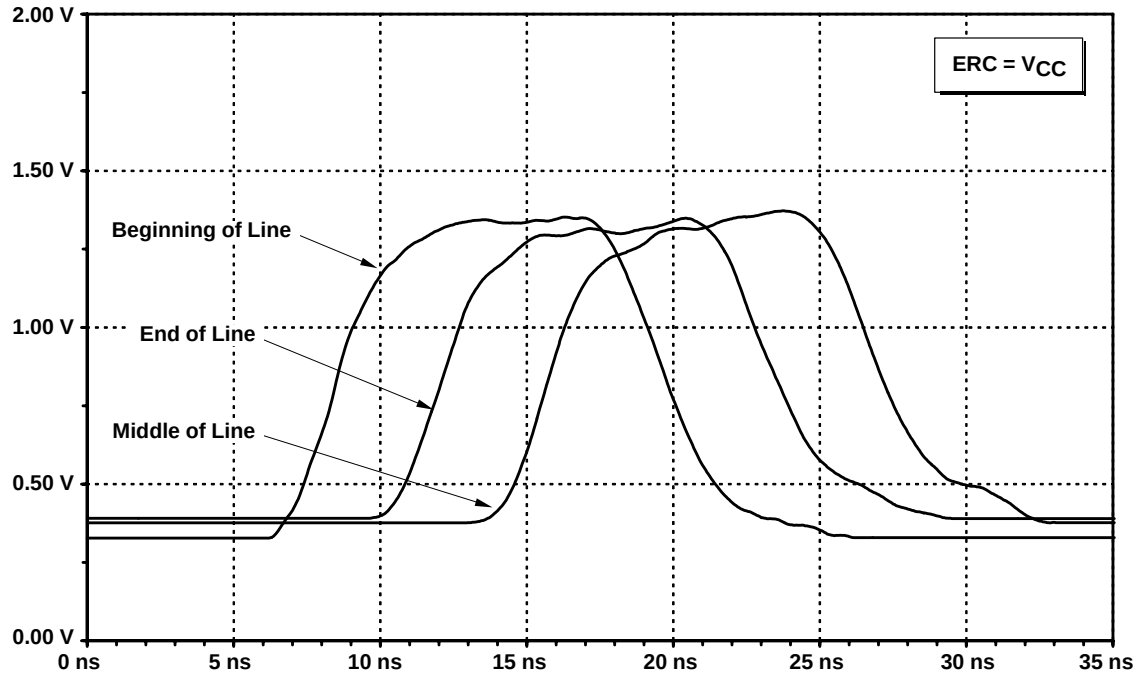

Figure 46. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 50 MHz

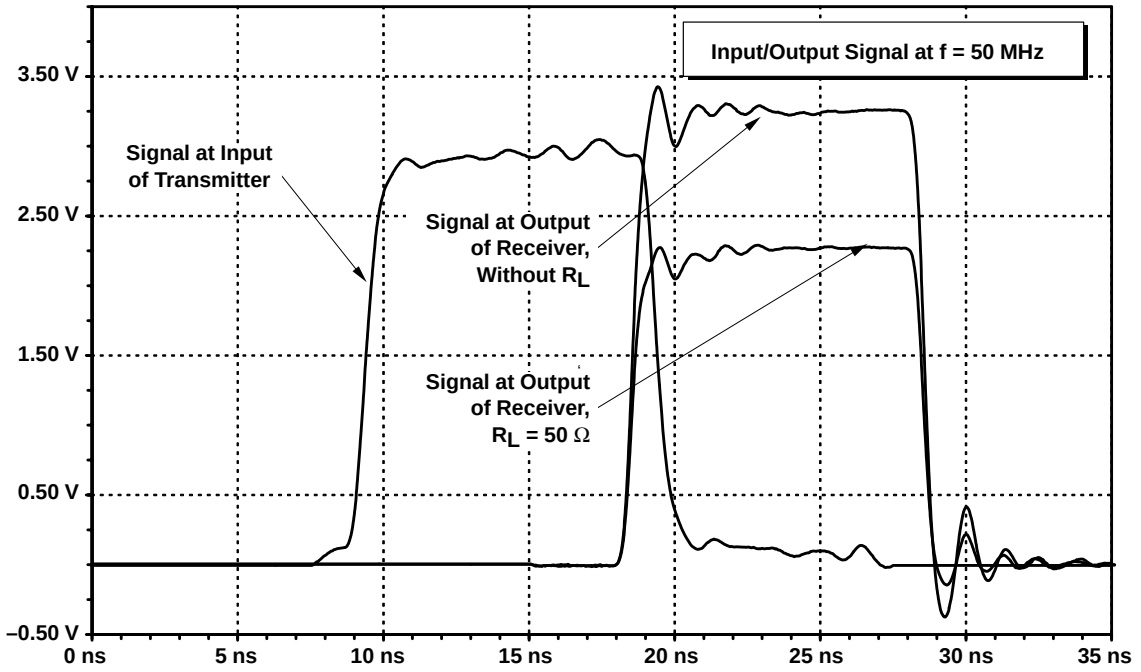

Figure 47. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 50 MHz

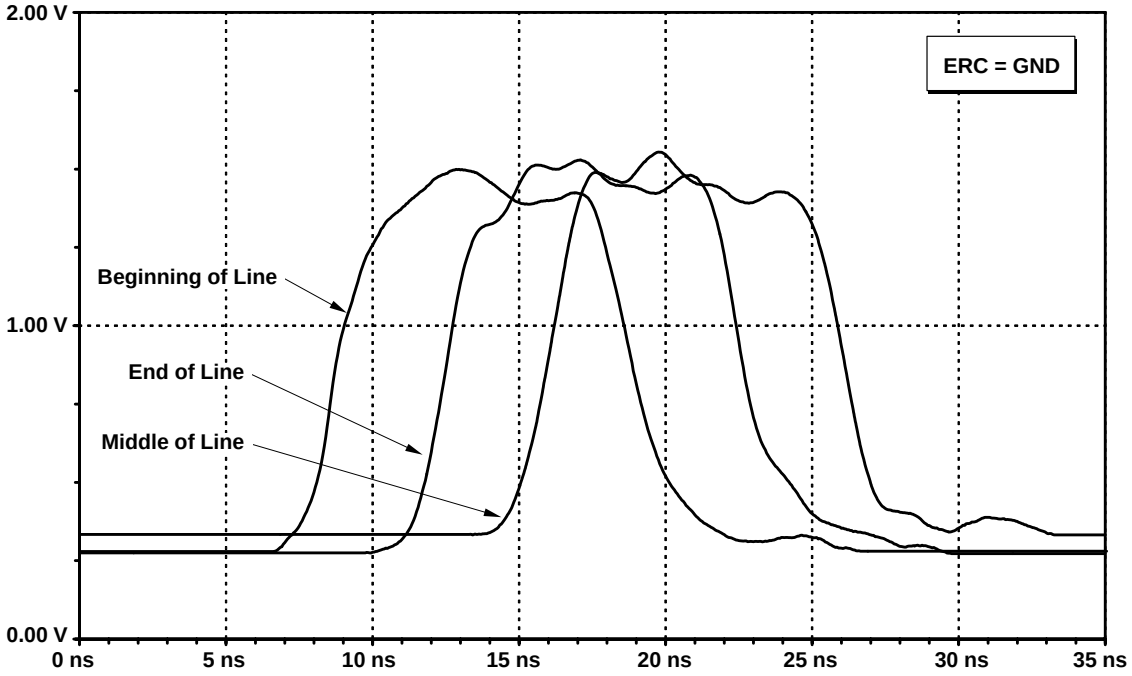

Figure 48. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 50 MHz

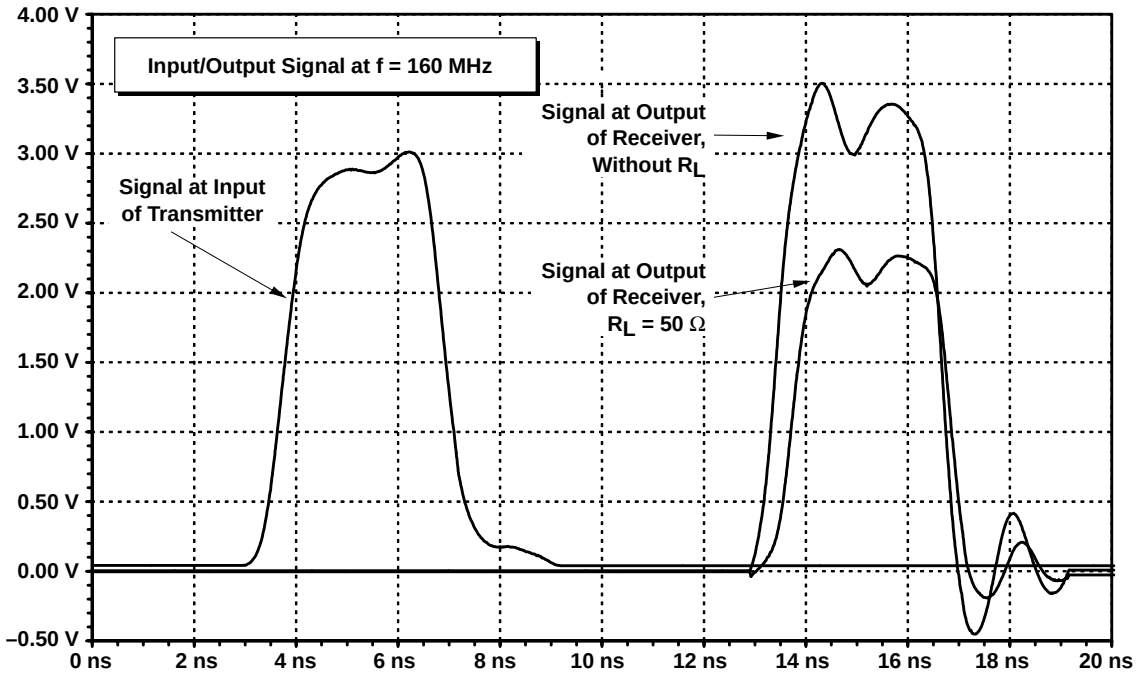

Figure 49. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 160 MHz

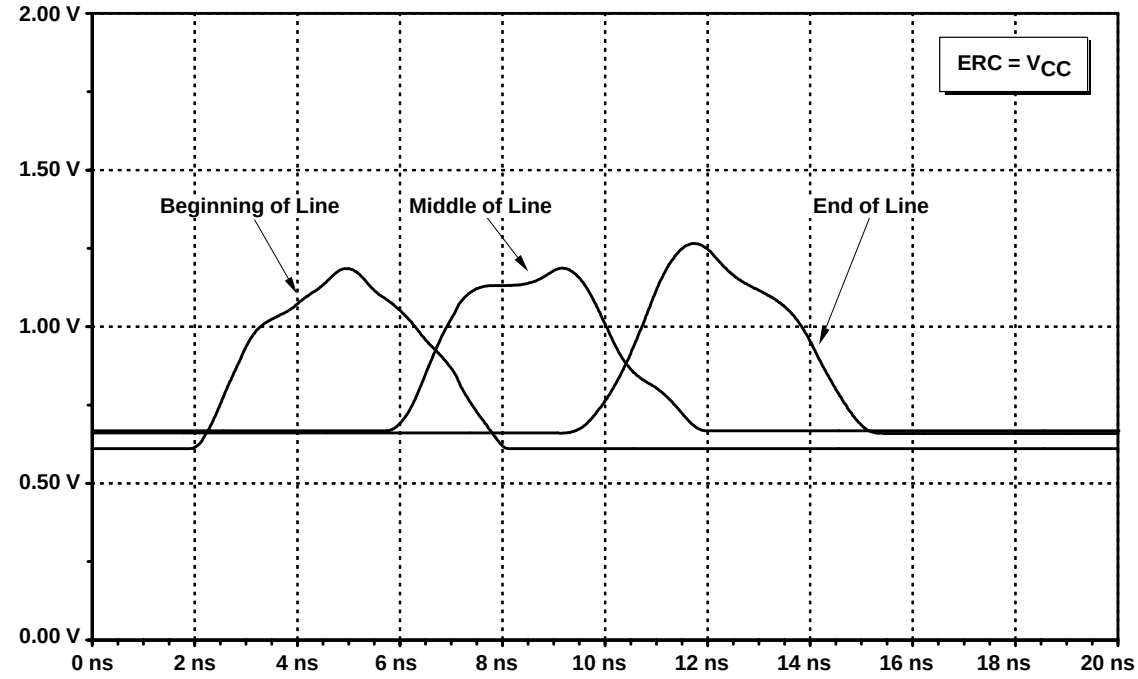

Figure 50. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 160 MHz

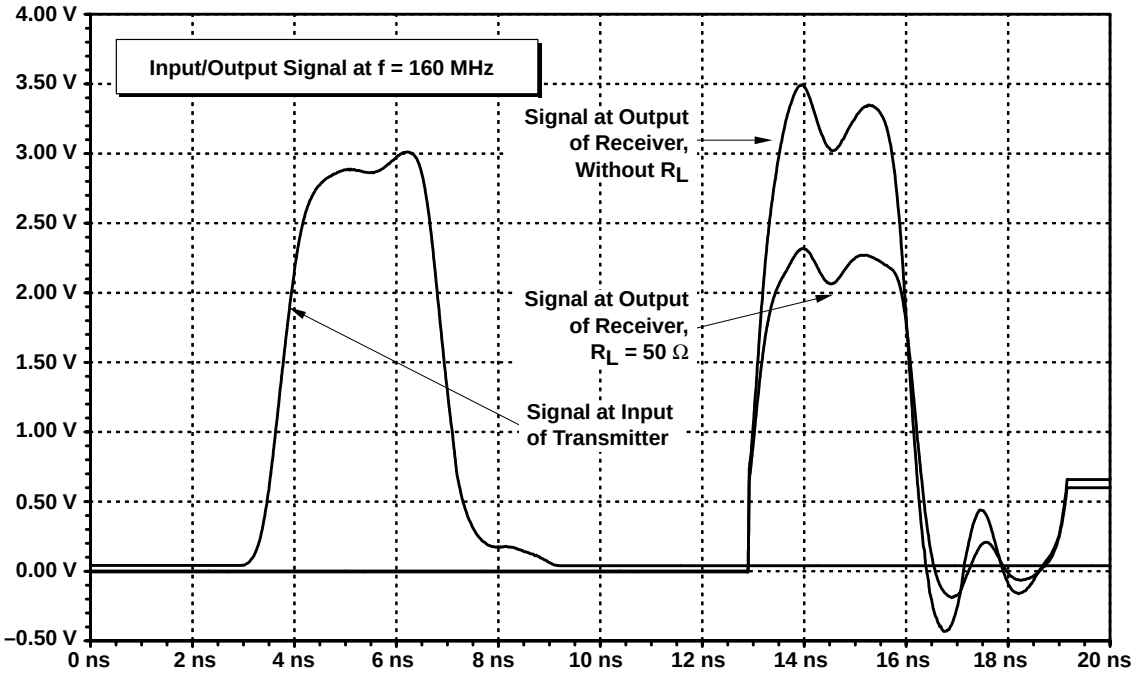

Figure 51. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 160 MHz

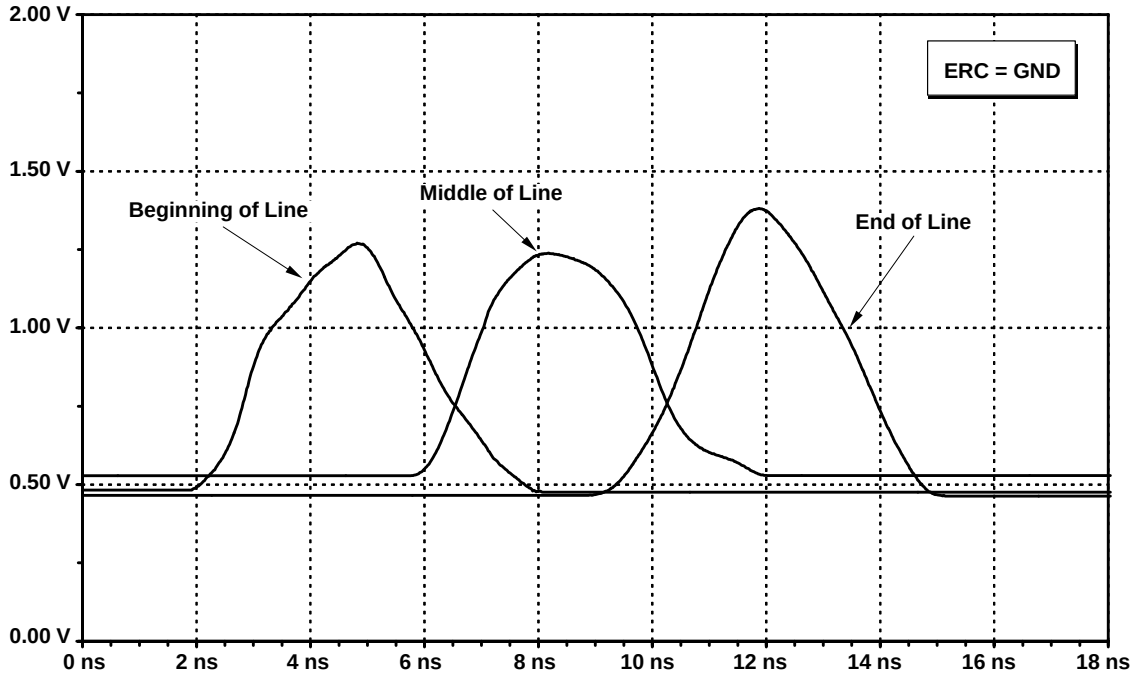

Figure 52. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 160 MHz

Summary

The SN74GTLPH1655 from TI provides engineers who develop fast and complex bus systems with a high-performance bus driver that is particularly suitable for the design of modern low-voltage systems.

Very high signal-propagation speeds are possible, as a result of the increased drive capability of 100 mA, compared with standard GTL circuits (40 mA), and the selectable edge rate. Bus lines with low line impedances of about 22 Ω can be used with the SN74GTLPH1655.

Bus lines with low line impedances of about 22 Ω can be matched using GTLP drivers that have a four-digit identifier, such as the SN74GTLPH1655. The four digits indicate the high drive capability of I_{OL} = 100 mA, while all other GTLP devices have a drive capability of 50 mA.

The four-digit GTLP devices allow optimum termination of low-impedance bus lines, thereby preventing interference and signal distortion that may otherwise occur as a result of line reflections. Reduced signal-voltage amplitude improves signal integrity.

The power-up 3-state and precharge functions provided by the SN74GTLPH1655 and, also, the bus-hold cells at the input of the LVTTL side, allow the design of modern high-speed systems requiring minimum development effort.

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Glossary

BTL	Backplane Transceiver Logic
ERC	Edge-Rate Control
GND	Ground potential
GTL	Gunning Transceiver Logic
GTLP	Gunning Transceiver Logic Plus
I/O	Input/Output
Live insertion	Removal and reinsertion of modules during operation
LVTTL levels	3.3-V logic levels, compatible with TTL logic levels
Partial power down	Switching off parts of a system that is in operation without removing them from the system
Precharge	Charging I/O pins to the threshold voltage
TTL	Transistor-Transistor Logic
V_{CC}	Supply voltage

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