ABT Enables Optimal System Design

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Introduction

As operating frequencies of microprocessors increase, the time allotted for memory access, arithmetic computation, or similar operations decreases. With this in mind, a new series of Advanced Bus-Interface Logic (ABIL) products developed with Texas Instruments (TI) submicron Advanced BiCMOS Technology (ABT) process assumes a prominent role as the key high-performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide system designers a bus-interface solution combining high-drive capability, low power consumption, signal integrity, and propagation delays small enough to appear transparent with respect to overall system performance. Fine-pitch package options simplify layout, reduce required board space, and decrease overall system costs. Novel circuit-design techniques add value over competitive solutions.

Trends Important for Today's System Designer

Modern system designers face many complex challenges in meeting their design goals. The trends toward (need for) faster cycle times, lower power consumption, smaller footprints, greater reliability, and lower total system cost combine to put ever-increasing pressure on today's system designer.

The need for faster cycle time traditionally has been addressed by the microprocessor manufacturer. Clock and microprocessor frequencies have increased steadily with each succeeding product generation. The most advanced RISC processors in development are touting frequencies of about 200 MHz. For production systems, it is not unusual for processors to run on the order of 50 MHz and above. Increasing clock and microprocessor frequencies are now beginning to put pressure on surrounding memory and logic to make greater contributions in reducing overall system cycle times and improving overall system performance.

Higher-performance systems require the designer to focus on total system power requirements. Faster systems traditionally require more power, which often means more costly solutions. Power costs money to supply, and heat buildup due to this power costs money to remove. Also, excess power consumption adversely affects reliability due to the increase in the junction temperature of the silicon components. Lower-power devices reduce requirements for larger power supplies and high-cost cooling techniques, and could lead to smaller system packaging.

Occurring in parallel with demands for increased system performance and reduced system power consumption is demand to house systems in smaller cases, boxes, chassis, and cabinets. This miniaturization requires that each system component be optimally laid out in silicon, packaged, and mounted on the printed-circuit board (PCB).

Speed, power, size, cost, and reliability are all parameters by which system and end-equipment success are measured. Semiconductor manufacturers must be sensitive to these parameters and be able to provide well-defined and well-designed products to meet these needs.

Advanced Bus-Interface Logic (ABIL) as the System Bus Interface

Semiconductor vendors are required by system design houses to provide new products that are faster, consume less power, exist in smaller packages, and present a lower relative cost than their predecessors. Since the early 1970s, many different logic-product technologies have attempted to meet these demands.

Early logic-product technologies often forced the system designer to make tradeoffs. As shown in Figure 1, speed and power were the most typical design goals traded off. Solutions such as Schottky or HCMOS, respectively, offered high speed at the expense of low power or low power at the expense of high speed. In a typical system application, this logic technology is used between only a few system blocks, such as a simple 8-MHz processor, a slow 256K DRAM, and a local TTL bus. Their functional role was little more than small-scale integration (SSI) or medium-scale integration (MSI). Despite these shortcomings, early logic technologies thrived because they were inexpensive and readily available.

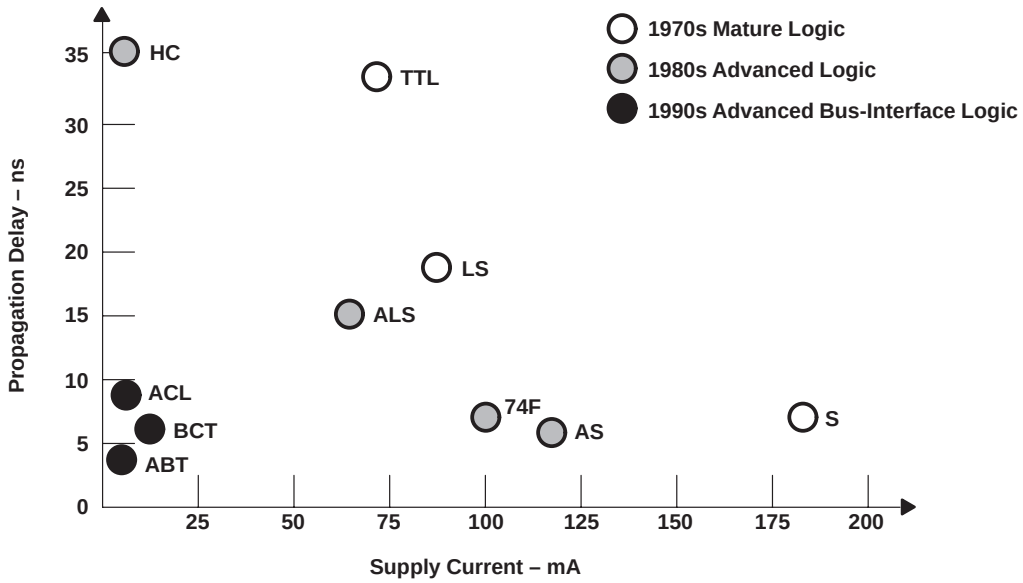


Figure 1. ABT Assumes Optimal Position

Cycle-time requirements for interface logic vary as a function of microprocessor and clock speed. In an 8-MHz system, the total system cycle available for completion of all operations is 250 ns. This can be roughly budgeted into 160 ns for the memory access, 45 ns for processor setup, and 45 ns for the interface logic (including signal propagation across PCB traces). With 45 ns available for interface, a forgiving, low-performance technology such as low-power Schottky or HCMOS can be utilized.

The situation changes dramatically when system speeds increase to 45 or 50 MHz. At 45 MHz, only 44 ns of total cycle time is available to complete all operations. Now, more expensive memories are needed with access times in the 20-ns range. Microprocessor setups can only be 8 ns. This leaves only 16 ns for interface and signal-trace propagation delay. The interface cycle time is a much higher percentage of the total system cycle time at 45 MHz than at 8 MHz.

As cycle-time requirements shrink, each nanosecond becomes critical in meeting the total system budget. The system designer has the option of using higher-performance memories, processors, or interface logic in squeezing additional nanoseconds out of the system delay. There is great demand for using interfacing logic to meet these budget needs because typically it is much less expensive for the designer to use than higher-performance memories or processors.

In light of decreasing total system cycle-time requirements, early logic technologies gave way to faster technologies. Significant gains made since the Schottky and HCMOS days result in products that no longer force the system designer into a tradeoff box. New-product development in the area of complex memories, processors, and ASICs has led the way for an equal, if not greater, acceleration in new-product development for advanced digital-logic products.

This development has propelled logic up from the ranks of *glue* status, used to fill in design gaps around the other major system blocks, to its new position as the system bus interface. ABIL products are now responsible for controlling the signals between the backplane buses and the other major system design blocks. They have become a major system design block in their own right, exerting significant influence over the performance of the final design.

In a modern-day system, ABIL products are likely to connect many major system design blocks, including application-specific parallel processors, 4M DRAMs, fast-cache SRAMs, and complex ASIC gate arrays/standard cells. The task of this new breed of advanced logic is to effectively transceive the address, data, and control signals of these integrated-circuit elements to and from heavily loaded TTL/CMOS/BTL system backplanes.

A wide variety of industry-standard and proprietary backplane specifications add to the difficulty of the task. At the low end of the scale, exhibiting data-transfer rates in the range of 10 to 20 Mbytes/s, are the PC-, AT-, and EISA-type buses. For midrange server and graphics-workstation applications, the 50- to 100-Mbytes/s data-transfer-rate range of Multibus II and microchannel-type buses is typical. High-end server and mainframe computer applications require the ≥ 100-Mbytes/s data-transfer rates of Futurebus+-type buses. Transceivers connecting to each of these backplanes must provide very high-drive current capability to effectively and reliably migrate signals across. ABIL products from TI uniquely address this need.

Enablers to Continuous New-Product Development

Reduction in minimum process dimension, enhanced value-added circuit design techniques, utilization of fine-pitch packaging, and incorporation of lower-power supply voltages are the most important enablers to continuous new development for logic products.

The minimum process dimension represents the width of the transistor-gate region and gives an indication of the switching speed of the transistor. In general, the smaller the minimum process dimension, the faster the transistors switch. An added advantage of reducing the minimum process dimension is the gain in gate density that can be achieved. A gain in gate density results in increased device functionality without a corresponding increase in silicon die area. Currently, state-of-the-art high-volume-production logic processes consider a 0.8-µm minimum process dimension. However, work is ongoing to prototype more advanced processes characterized by 0.6-, 0.5-, and 0.35-µm minimum process dimensions.

Enhanced value-added circuit-design techniques greatly increase the functionality of a logic device as well as improve its performance. These techniques often eliminate the need for the designer to utilize discrete components such as resistors, capacitors, and diodes because these are built into the silicon device itself. Additionally, optimizations in I/O or core circuitry can positively affect speed and power performance.

An aggressive drive exists to convert classic through-hole package approaches to totally above-board surface-mount approaches. Occurring in parallel is a drive to upgrade existing surface-mount packages with finer pin-to-pin pitches so as to minimize total package area. However, with smaller packages comes increased reliance on thermal-management techniques. The increased difficulty in removing heat from the smaller packages can preclude the use of inexpensive plastic packages. The need for ceramic or other alternatives would act to drive up design costs.

Finally, system designers are beginning to drive the semiconductor industry to move below 5 V as the baseline for power supplies. The migration to lower voltages, such as 3.3 V, enhances the reliability of advanced process technologies exhibiting minimum process dimensions of 0.6 µm or lower. The need for low-voltage memory and processor product interface, lower device-generated noise levels, lower power consumption, and increased battery life for unregulated portable systems accelerate the demand for 3.3-V logic. New 3.3-V logic opportunities will emerge as system designers continue to rely on advanced process technologies.

What Is Advanced BiCMOS Technology (ABT)?

Advanced BiCMOS Technology (ABT) is available today in products from TI to aid designers doing high-performance bus management. It is currently available in many different product options, including 8-bit octal, 16-, 18-, and 20-bit Widebus™, and 32- and 36-bit Widebus+™ versions.

At TI, ABT evolved from an earlier 1.5-µm BiCMOS process. It was designed to provide speeds equivalent to existing advanced bipolar solutions but with 90% less device power. This standard BiCMOS process introduced high-performance, lower-power, bus-interface products to the marketplace two years ahead of the nearest competitor. Since its bus-interface introduction in 1987, TI has utilized BiCMOS and advanced BiCMOS in products such as mixed-signal integrated circuits, high-performance gate arrays, high-speed cache tags, and application-specific processors such as the SuperSPARC™.

ABT employs a submicron 0.8-µm minimum process dimension. It combines elements of both bipolar and CMOS circuit/process technologies onto a single silicon chip. ABT offers the system designer the best combination of high speed, high drive, and low power consumption in the industry. As shown in Figure 1, ABT provides a performance point closer to the origin of the speed/power graph than any other logic technology available. Specifically, ABT is based on a CMOS core-circuit structure with an NPN bipolar output transistor module added. This means adding about four additional masks to the CMOS process. The current single NPN transistor output structure of ABT has been optimized for 5-V operation.

Simplified input and output stages of an ABT transceiver are shown in Figure 2. The inputs are designed to offer TTL-compatible levels with guaranteed switching between a V_{IH} minimum of 2 V and a V_{IL} maximum of 0.8 V. These inputs are implemented with CMOS circuitry; therefore, they offer characteristic high impedance for low leakage and low capacitance for minimal bus loading. The CMOS supply voltage of the input stage is dropped by diode D1 and transistor Q1, centering the threshold around 1.5 V. When inputs are in the low state, Q_r raises the voltage of source Q_p up to the rail, ensuring proper operation of the feedback stage. This stage provides about 100 mV of input hysteresis, increasing noise margins and reducing oscillations.

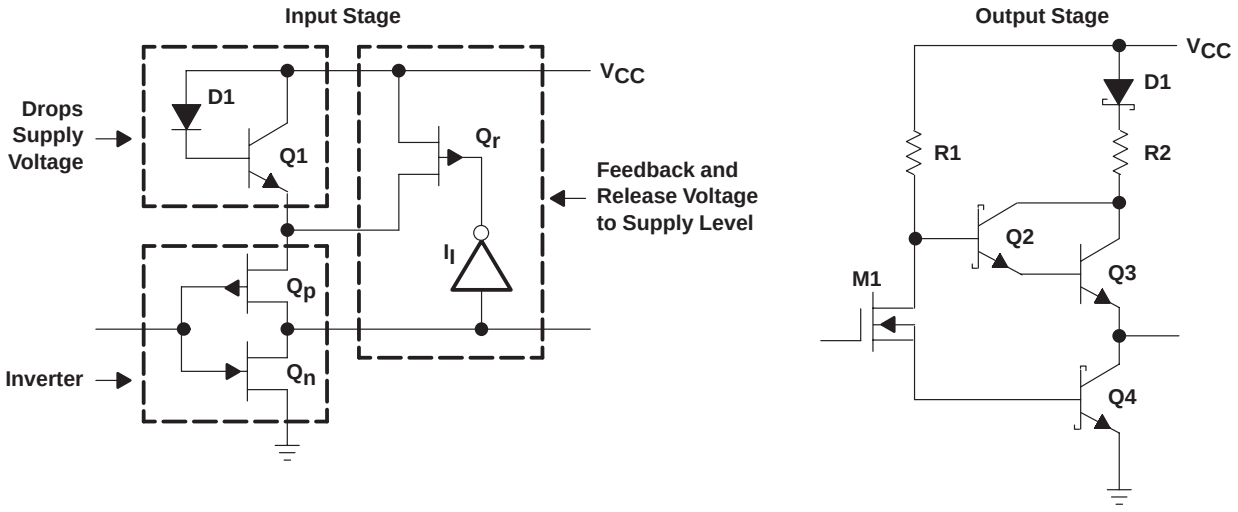


Figure 2. ABT Input/Output Circuit Structure

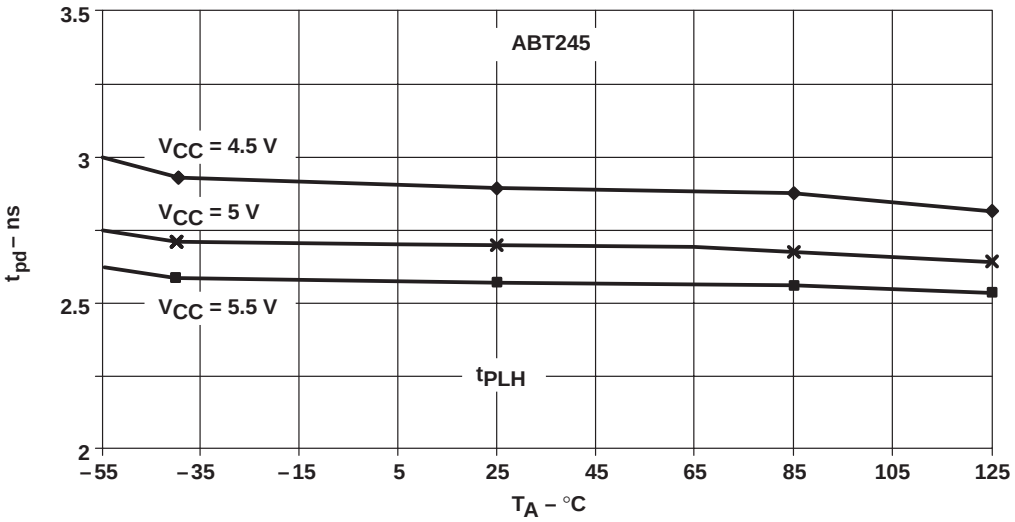
ABT outputs utilize bipolar circuitry to provide the high speed and drive necessary for a bus interface. A major advantage of using bipolar circuitry in the output stage is the reduced voltage swing, which lowers ground noise, improves signal integrity, and reduces dynamic power consumption. In Figure 2, M1 acts as a current switch that drives the outputs low when conducting current from R1 through to the base of Q4. The base of Q2 is pulled low, turning off the upper output. For a low-to-high output transition, M1 turns off and current through R1 charges the base of Q2. As Q2 goes high, the Darlington pair, Q2 and Q3, turns on. With its supply of base current now cut off, Q4 turns off and the output transition switches low to high. R2 limits output current in the high state and D1 is a blocking diode preventing current flow in power-down applications.

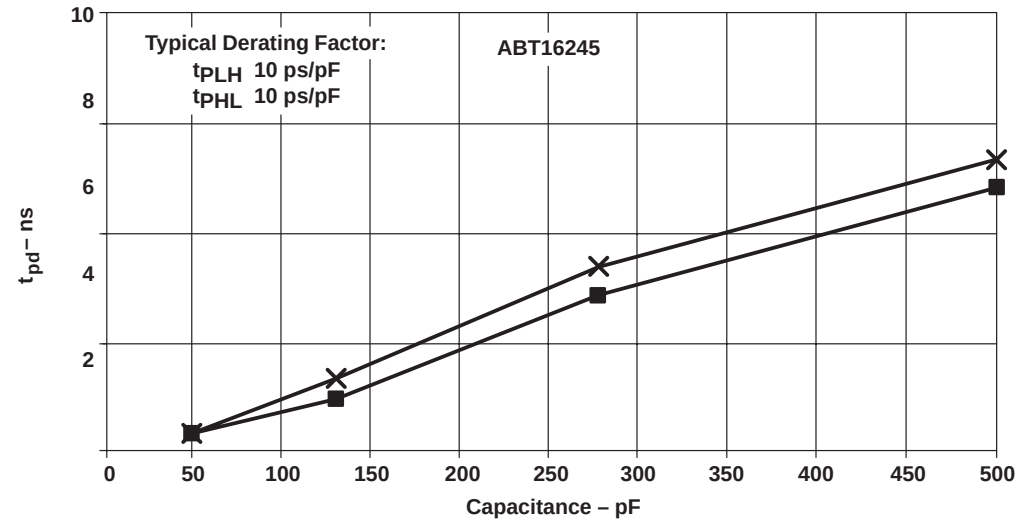
By virtue of its small minimum process geometry, tight metal pitch, and shallow junctions, ABT can provide strong output drive currents (sink currents specified at 64 mA and source currents specified at 32 mA) and low parasitic capacitances. As a result of these enhancements, internal propagation delays are very fast and very well behaved. Figure 3 shows that typical propagation delays are on the order of 2–3 ns across the operating temperature range. This excellent consistency allows ABT to be specified over the industrial temperature range of –40°C to 85°C. Figure 3 also shows that ABT performance is very well behaved across capacitive load and multiple-output switching conditions.

Maximum propagation delays for ABT are as low as 4–5 ns, depending on the device type and propagation path. Table 1 compares the data sheet maximums of several ABT 16-bit Widebus™ transceiver devices with competing FCTB/C CMOS and 74F/ALS bipolar solutions. It is clear from both Figure 3 and Table 1 that ABT is the system designer's best choice for bus-interface applications that require consistent speed performance for many different conditions.

From a power (current) consumption standpoint, the use of bipolar in the output stage is advantageous for two reasons. First, the voltage swing is less than that of a CMOS output. The power consumed when charging or discharging internal circuit capacitances and the external load capacitance is reduced. Second, the bipolar transistors are capable of turning off more efficiently than CMOS transistors. The wasteful flow of current from V_{CC} to GND is reduced. Although bipolar does tend to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or CMOS. This is because the dynamic power component makes up the majority of a device's overall power consumption.

The ABT maximum high-impedance supply currents (I_{CCZ}) range from about 50 µA for 8-bit octals to about 2–3 mA for 16-bit Widebus™ products. Maximum dynamic supply currents (I_{CCL}) range from about 30 mA for 8-bit octals to about 34 mA for 16-bit Widebus™ products. Power on demand, an enhanced circuit design improvement to the bipolar output stage on new ABT product families, reduces dynamic current consumption levels by up to 50%. High-impedance and dynamic supply-current goals for the new 32-/36-bit Widebus+™ family are 500 µA and 60 mA, respectively.





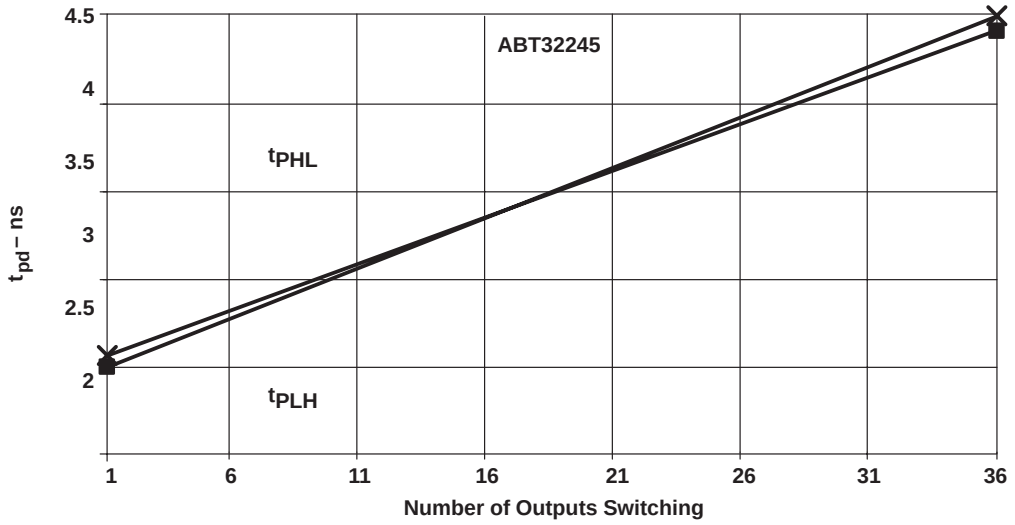
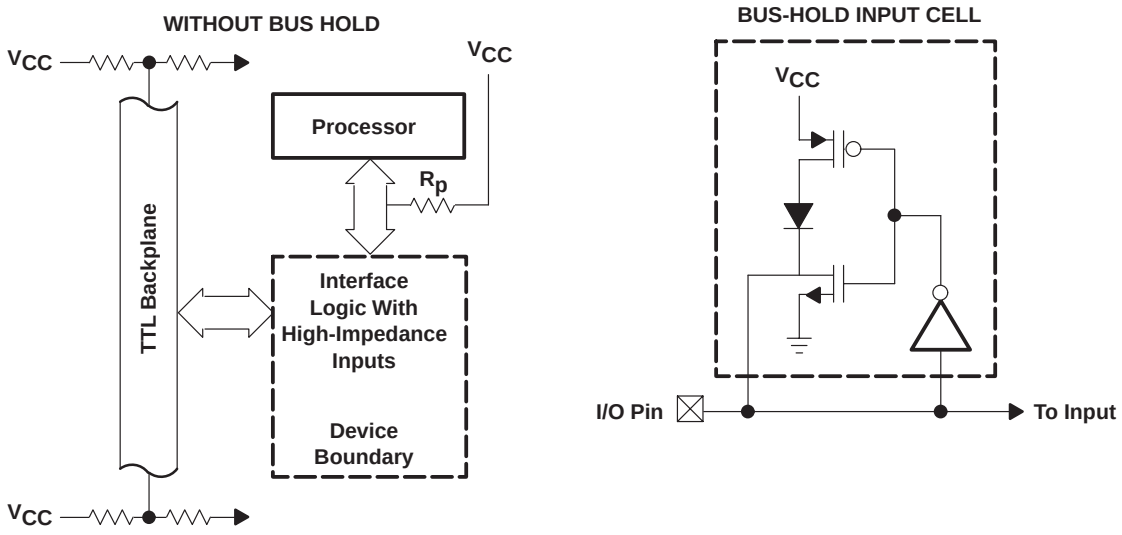


Figure 3. ABT Process Provides Consistency

Table 1. ABT Is the Speed Benchmark

REGISTERED TRANSCEIVER WITH CLKEN	ABT16952 (ns)	29FCT52C (ns)	F2952 (ns)
t_{pd} CLK to A/B	4.5	6.3	9
$t_{pd(en)}$ $\overline{OE}$ to A/B	6	7	10
$t_{pd(dis)}$ $\overline{OE}$ to A/B	5.5	6.5	9
TRANSCEIVER WITH PARITY	**ABT16657 (ns)**	**ABT657 (ns)**	**F657 (ns)**
t_{pd} A to B	4.3	5.5	8
t_{pd} A to PARITY	6.7	11.3	16
t_{pd} B to $\overline{ERR}$	6.7	15.7	22.5
REGISTERED TRANSCEIVER WITH PARITY	**ABT16833 (ns)**	**FCT833B (ns)**	**ALS29833 (ns)**
t_{pd} A to B	4.3	7	10
t_{pd} A to PARITY	6.7	10.5	15
t_{pd} CLK to $\overline{ERR}$	4.6	15	16

Bus hold, as shown in Figure 4, is another example of an enhanced, value-added circuit design technique available on new ABT product families. The bus-hold cell provides for a small holding current of 100 μA to be delivered to I/O pins configured as inputs left unused or floating. This current latches the last known input state to a valid logic level. Floating input conditions are common to CMOS backplanes or device bus-interface situations where driving entities are periodically required to be in 3 state. Bus-hold cells eliminate passive pullup (to V_{CC}) or pulldown (to GND) termination resistors necessary to prevent application problems or oscillations. External provision for these resistors by the system designer consumes board area, increases bus capacitance, contributes to bus loading, and lowers system performance. The bus-hold feature is particularly effective when offered on products with a lot of I/O capability such as 32-/36-bit Widebus+™ devices.



- **Holds the last known state of the input**
- **Provides for ±100 μA of holding current at 0.8 V and 2 V**
- **Bus-hold current does not load down the driving output at valid logic levels**
- **Negligible impact to input/output capacitance (0.5 pF)**
- **Eliminates the need for external resistors on unused or floating input/output pins**

Figure 4. Bus-Hold Circuit and Benefits

Fine-Pitch Packaging Shrinks ABT Device Size

As the push for smaller system sizes becomes intense, the system designer will require the logic manufacturer to house high-performance silicon in increasingly smaller packages. Most notably, the system designer has been leveraging the advantages of plastic-leaded chip carriers (PLCCs) and small-outline integrated circuits (SOICs).

Both PLCC and SOIC packages provide a gull-wing lead profile. Both utilize 1.27-mm pin-to-pin pitch spacing. The reduced pitch offers a major space improvement over bulky plastic dual-in-line (PDIP) through-hole packages. The major difference between PLCC and SOIC is philosophical. The PLCC has pins on all four sides (arranged either in square or rectangular configuration) while the SOIC has pins on only two sides (arranged in flow-through configuration).

In spite of the advantages of PLCC and SOIC, system designers are beginning to specify surface-mount packages with finer pitch values to keep their end equipments competitive in the marketplace or to avoid falling behind more aggressive rivals. Such fine-pitch versions available in volume today offer improvements in the pin-to-pin pitch down to 0.635 mm. More advanced fine-pitch alternatives exhibiting characteristic pitches of 0.5, 0.4, and 0.3 mm are on the horizon.

The plastic quad flat package (PQFP) is a fine-pitch version of the PLCC package. It offers a 0.635-mm pitch and is widely used for microprocessors, ASICs, or other custom devices. The 44-pin PQFP is the smallest used in volume, while the largest versions provide over 200-pin capability. However, for the system designer using ABIL products, it is advantageous to combine the fine-pitch capability of the PQFP with the two-sided dual-in-line design of the SOIC.

SOICs have evolved in two distinct paths to meet this need. The first path considers reducing the surface area and pin pitch of the package while keeping the pin count and bit density constant. The second path considers increasing the bit density of the package by increasing pin count and reducing pin pitch. Figure 5 clearly shows both of these migratory paths starting from the standard octal SOIC package in the upper left corner.

Package size reductions are shown from top to bottom in Figure 5, with each succeeding reduction occupying a new row at constant bit density and pin count. Bit-density and pin-count increases are shown horizontally across Figure 5.

There are five new fine-pitch packages represented in Figure 5. Four of these offer a density-upgrade path for the SOIC. The fifth is a new package offering a density upgrade for the PQFP. All of these packages were developed and standardized exclusively for high-performance ABIL ABT products by TI.

The shrink small-outline package (SSOP) is available in two worldwide standard form factors. The first, approved by the Joint Electronic Device Engineering Council (JEDEC), allows for 16-, 18-, or 20-bit I/O functions in a package roughly the same size as the octal SOIC. The pin pitch for the JEDEC SSOP is 0.635 mm. The JEDEC SSOP is available in a 48-pin version for the basic 16-bit driver and transceiver functions and in a 56-pin version for complex 16- to 20-bit transceiver functions. The very popular ABT Widebus™ family uses the JEDEC-approved SSOP.

The second form factor, approved by the Electronics Industry Association of Japan (EIAJ), allows for 8- and 9-bit I/O functions in a package about 40% of the size of the octal SOIC. The pin pitch for the EIAJ SSOP is 0.65 mm. The EIAJ SSOP is available in a 20-pin version for basic ABT 8-bit driver and transceiver functions and in a 24-pin version for complex ABT 8- and 9-bit transceiver functions.

The bottom row of Figure 5 represents the third form-factor upgrade to the SOIC available from TI. The thin shrink small-outline package (TSSOP) is EIAJ approved and offers a reduced thickness (height) specification of 1.1 mm. The pin pitch of the EIAJ TSSOP is 0.65 mm (the body width is 4.4 mm). The TSSOP is compatible with Type I and Type II card physical requirements of the Personal Computer Memory Card International Association (PCMCIA). TSSOP offers the smallest package size available for 20- and 24-pin drivers and transceivers. For denser memory arrays, TSSOP facilitates front and back side mount in under 3.3-mm thickness specified by PCMCIA if card thicknesses are kept under 1 mm.

For wide-word applications with extreme space and height restrictions, TI offers Widebus™ devices in a new package called the Shrink Widebus™. Available in 48- and 56-pin versions, this new package has a 1.1-mm maximum height, a 6.1-mm body width, and a 0.5-mm lead pitch. The Shrink Widebus™ package, developed by TI, is registered with the EIAJ, meets the requirements of the PCMCIA, and occupies 40% less board area than the standard JEDEC SSOP.

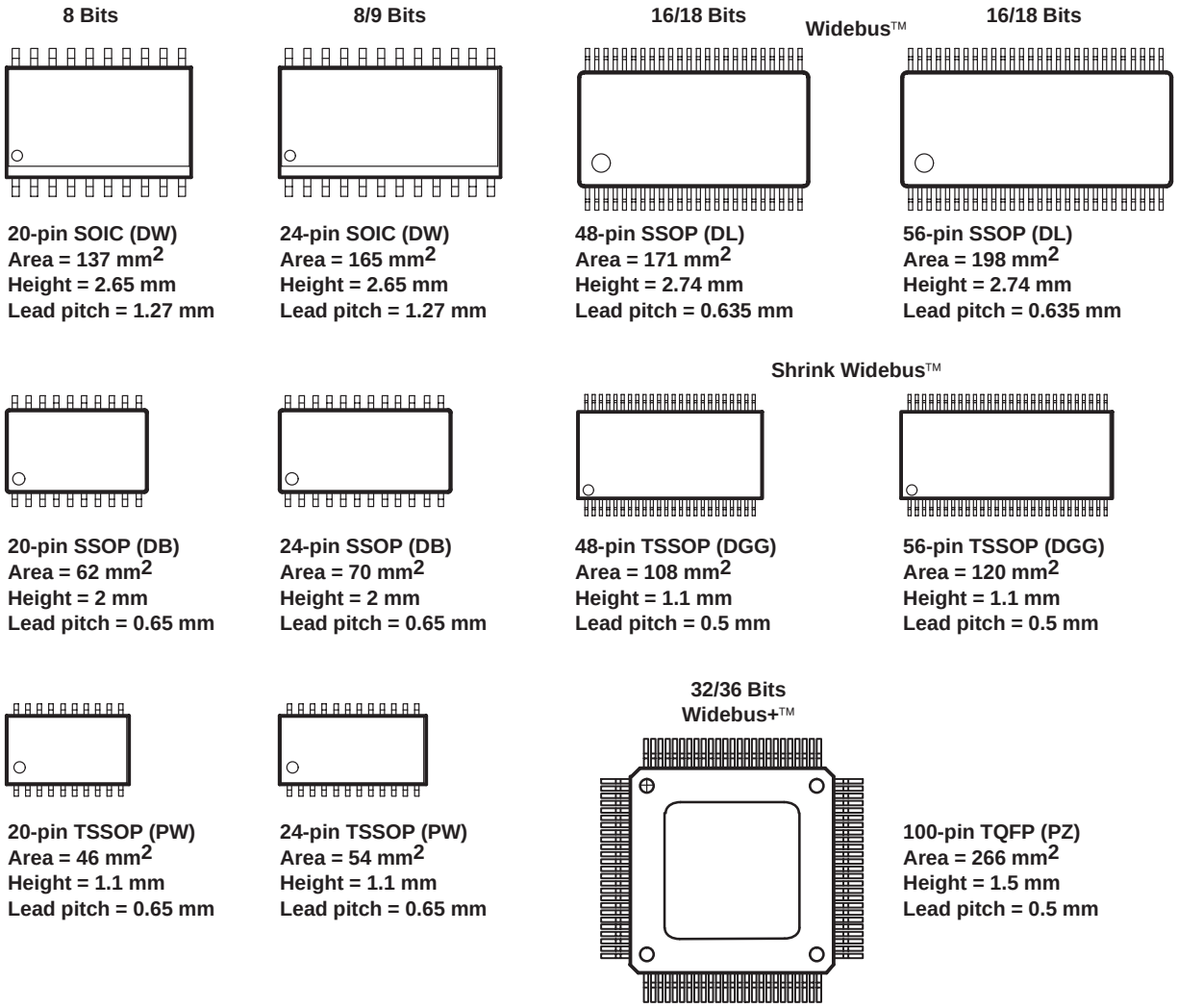


Figure 5. Fine-Pitch Package Options for ABT

The EIAJ thin quad flat package (TQFP) provides the density upgrade path for the PQFP. This 100-pin package allows single-chip 32- and 36-bit I/O solutions in over 50% less area than with octal SOIC connections. The pin pitch for the EIAJ TQFP is 0.5 mm, which is the smallest in production today. The reduced pitch of the TQFP offers a 35% area reduction over 100-pin PQFP solutions. The new 32- and 36-bit ABT Widebus+™ family, announced at the BUSCON '92 West trade show in Long Beach, California, uses the 100-pin TQFP.

All of the fine-pitch package options are superior for space-saving applications. The JEDEC SSOP and EIAJ TQFP are superior in several other areas as well. The JEDEC SSOP incorporates a flow-through architecture where input and output pins each have their own dedicated side of the package. Flow-through pinouts offer the system designer a very easy route path for signal traces.

A standard SOIC octal package can afford only one GND pin for every eight I/Os. This ratio improves to 2:1 and 3:1 for JEDEC SSOP and EIAJ TQFP, respectively. Both the JEDEC SSOP and the EIAJ TQFP provide multiple V_{CC} and GND pins distributed along the sides. The larger number of GND pins and distribution of these pins results in less noise and allows for less propagation delay than octal functions. As a result, ABT octals, ABT Widebus™, and ABT Widebus+™, all typically exhibit less than 1 V of noise, even though the maximum number of switched outputs increases from 8 bits to 18 bits to 36 bits with each respective family.

As package area decreases, the thermal impedance of the package to the ambient environment increases. Thermal impedance represents the ability of a package to dissipate heat. The higher the thermal impedance, the more difficulty the package has in dissipating heat. The higher thermal impedances of fine-pitch packages require additional attention and care from the system designer. Proper thermal management techniques as well as proper power dissipation guidelines must be used to ensure operation. Fortunately, the low power of ABIL ABT products is more conducive to a fine-pitch packaging approach than competitive CMOS solutions.

ABT Products Provide End-Equipment-Specific Solutions

Combining previously discussed state-of-the-art elements of the ABT process with its numerous advanced fine-pitch package options and enhanced circuit-design features yields a very impressive portfolio of new products. These new products effectively serve the distinct needs of the workstation, personal and portable computer, and telecom end-equipment markets.

Table 2 categorizes the entire ABIL product spectrum built with the ABT process technology. These families offer features and benefits dedicated to specific markets and industry standards. Figure 6 shows the relationships of these features and benefits.

Table 2. ABT Products and Features

NAME	EXAMPLE PART NUMBER	KEY FEATURES	NO. OF BITS	PACKAGES	MAX PROP DELAY (ns)	I_{CCZ} (mA)	I_{OL} (mA)	I_{OH} (mA)	TARGET APPLICATIONS
ABT	SN74ABT245A	0.8-µm process, –40°C/85°C	8, 9, 10	DIP, SOIC, SSOP (EIAJ), TSSOP	3.6	0.25	64	32	High-speed bus interface, PC, EWS, telecom
ABT Widebus™	SN74ABT16245A	Flow-through pinouts, low noise	16, 18, 20	SSOP (JEDEC), TSSOP	4.0	0.19	64	32	Higher performance, space-conscious applications
ABT Widebus+™	SN74ABT32245	Bus-hold cell, power on demand	32, 36	TQFP (EIAJ)	5.2	2	64	32	Single-chip 32-bit interface
IWS Drivers	SN74ABT25245	Enhanced output drivers	8	DIP, SOIC	4.3	0.5	188	96	25-Ω incident-wave switching
Memory Drivers	SN74ABT2245	Series output-damping resistors	8, 10, 11, 12, 16	DIP, SOIC, SSOP (EIAJ), SSOP (JEDEC)	4.5	0.25	12	12	Low noise, high-reliability driving, memory interface
Futurebus+	SN74FB2031	BTL port, 2-ns minimum edge rate	8, 9, 18	PQFP, SSOP (JEDEC), TQFP (EIAJ)	7.6	10	100	3	IEEE 896.1 backplane interface
BTL Drivers	SN74FB2033A	BTL-TTL-level translation	8, 9	PQFP, SSOP (JEDEC)	6.1	10	100	3	IEEE 1194.1 backplane interface
SCOPE™	SN74ABT8245	Testability, built-in self-test	8, 16, 18	DIP, SOIC, SSOP (EIAJ), SSOP (JEDEC), TQFP (EIAJ)	4.7	0.05	64	32	IEEE 1149.1 backplane interface
LVT	SN74LVT245B	3.3-V V_{CC}, mixed mode, bus hold	8	SOIC, SSOP, TSSOP	4	0.19	64	32	Battery portables, notebook computers, POS terminals
LVT Widebus™	SN74LVT16245A	3.3-V V_{CC}, mixed mode, bus hold, power on demand	16, 18	SSOP (JEDEC), TSSOP	4.1	0.19	64	32	Workstations, portable computers

For high-performance engineering workstation and server markets, the ABT Widebus™ and Widebus+™ families provide the highest integration and performance. They are necessary to connect the most demanding CISC/RISC microprocessors to the most heavily loaded, high-frequency backplanes.

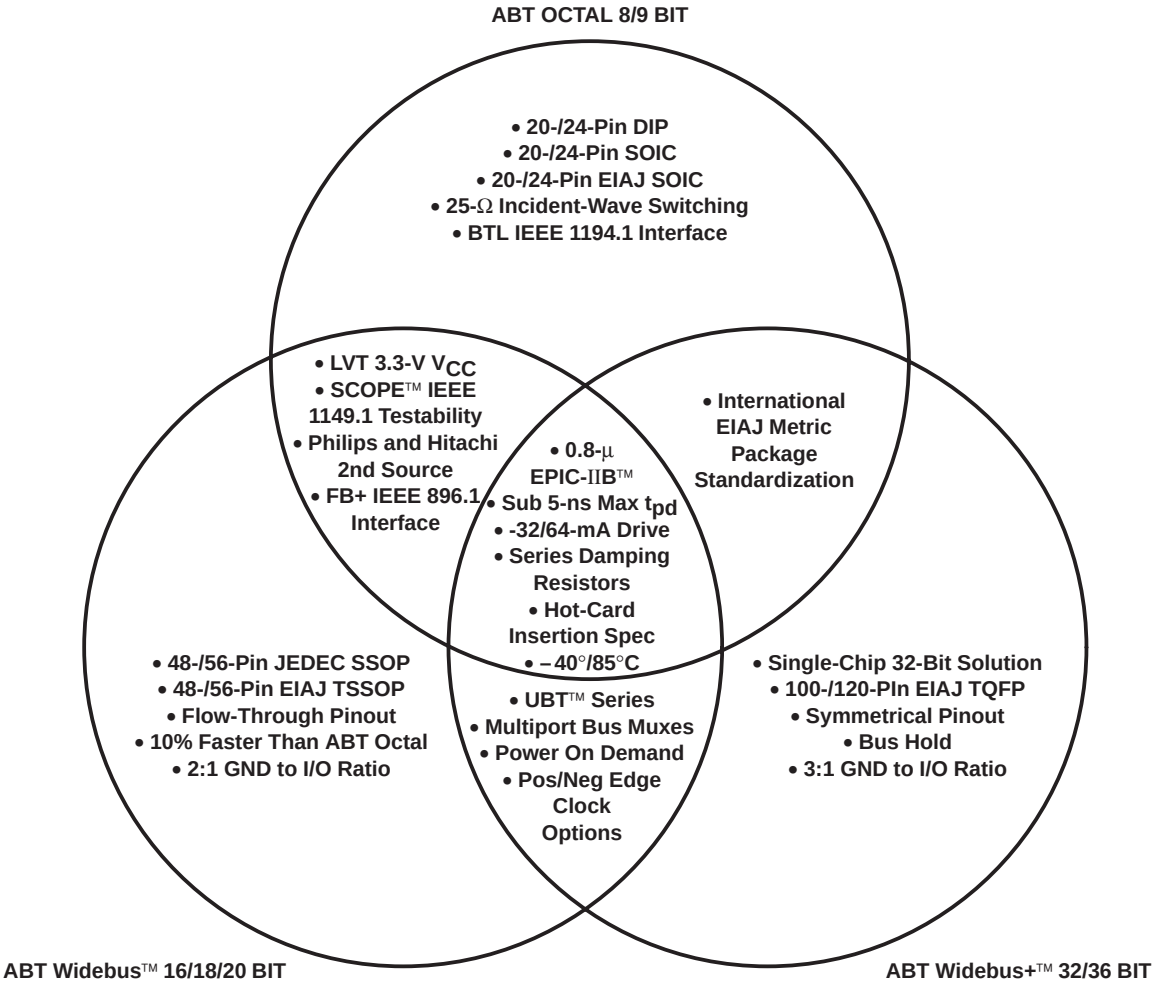


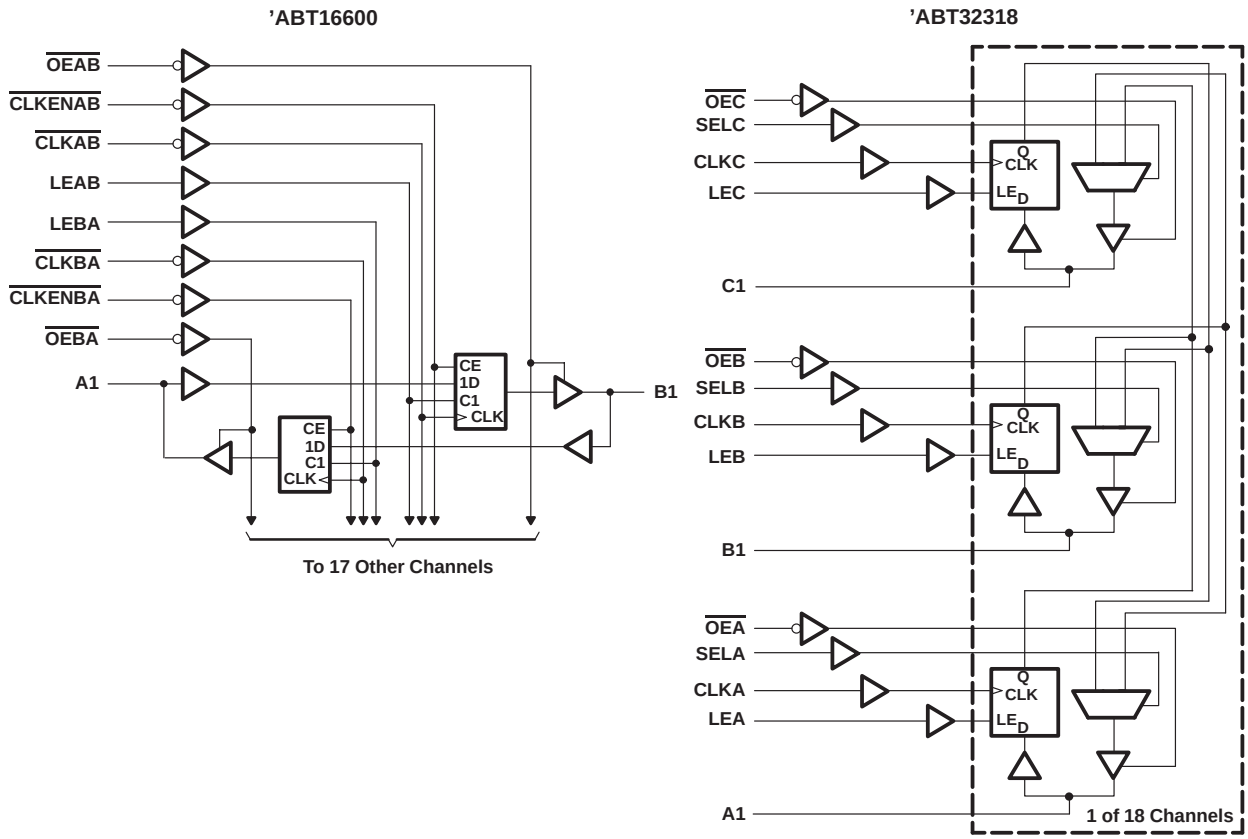
Figure 6. ABT Products and Features

The Universal Bus Transceiver (UBT™) is unique in the industry because it can be operated in several distinct bus-interface modes. Each package contains D-type latches and flip-flops. Flexible control-logic options provide for output-enable, latch-enable, clock, and clock-enable combinations.

UBT™s can be configured as transparent, data-flow-through transceivers (like the dedicated ’245 function), latch-enabled transceivers (like the dedicated ’543 function), clocked registered transceivers (like the dedicated ’646 function), and clock-enabled registered transceivers (like the dedicated ’952 function). Workstation designers can minimize inventory and procurement requirements, costs, and overhead with UBT™ flexibility. Designed specifically for workstation bus-interface applications, the UBT™ is perfect as an interface to the many different microprocessor architectures and system backplane specifications available.

Figure 7 details the current UBT™ portfolio from TI and includes block diagrams for two devices in the series. The ’ABT16600 is an 18-bit UBT™ packaged in the 56-pin SSOP package. It can be configured in each of four different data-flow modes between its A port and B port.

The ’ABT32318 is an 18-bit multiplexed UBT™ that can be configured in each of three different data-flow modes between its A port, B port, and C port. This UBT™ allows the system designer multiple combinations for real-time and stored data exchanges between the three ports. It is particularly useful for multibus communication, multiway interleaving memory applications, and high-performance, multiplexed-address and data-bus interface.



SERIES	NO. OF BITS	NO. OF PORTS	PACKAGE	NO. OF PINS	PARTITIONING	CONTROL LOGIC			
						OE	LE	CLK	CLKEN
16500/1	18	2	SSOP, TSSOP	56	× 18	Yes	Yes	Yes	No
16600/1	18	2	SSOP, TSSOP	56	× 18	Yes	Yes	Yes	Yes
32316	16	3	TQFP	80	× 16	Yes	Yes	Yes	Yes
32318	18	3	TQFP	80	× 18	Yes	Yes	Yes	No
32501	36	2	TQFP	100	× 18	Yes	Yes	Yes	No

Figure 7. UBT™ Portfolio

Several ABT product families directly address upper-end workstation and server equipment. A series of transceivers compliant with the IEEE 896.1 Futurebus+ backplane-interface standard are available. The special Futurebus+ protocols dictate special electrical requirements of the transceivers to ensure proper connection to Futurebus+ backplanes. Each of seven transceivers in the series utilize backplane transceiver logic (BTL) switching levels in accordance with the Futurebus+ standard. Complementing these Futurebus+ transceivers is a series of BTL transceivers compliant with the IEEE 1194.1 standard. Both transceiver series contain a TTL A port along with the BTL B port and can perform TTL-to-BTL and BTL-to-TTL-level translation.

SCOPE™ transceivers and drivers are available in ABT, which are compliant with the IEEE 1149.1 testability standard. For high reliability and fault-tolerant system needs, these devices provide their own internal self-test capabilities. A complete line of SCOPE™ hardware and software system products have been developed by TI.

The personal-computer market is characterized by very short design cycle times and intense pressure to lower costs. The major driving force is the need for workstation-type performance in machines designed for desktop, home, and portable applications. ABT in fine-pitch package options meets these needs nicely.

A new series of low-voltage products definitively addresses the needs of the portable subsegment of this market. The low-voltage technology (LVT) family has been developed with the submicron ABT process and will be available in both 8-bit octal and 16-/18-bit Widebus™ versions. Supply voltage for LVT is specified from 2.7 V to 3.6 V. The LVT 8-bit product uses the TSSOP to facilitate the smallest area for portable applications. The LVT Widebus™ product uses both the JEDEC SSOP and the 48-/56-pin EIAJ Shrink Widebus™ SSOP.

Market requirements for 3.3-V logic products are being driven now by battery laptops and hand-held instruments. Higher-performance desktop PCs and workstations could lag a year behind portables in their demand for 3.3-V logic.

As shown in Figure 8, the 5-V ABT I/O structure has been optimized for use with 3.3-V supply currents. LVT 3.3-V speed performance is equivalent to ABT 5-V speed performance. This special I/O circuitry also allows for a *mixed-mode* 3.3-V to 5-V interface capability. Designers can use the same LVT logic for the core 3.3-V system partition as for the external 5-V backplane interface. This is particularly important as other system elements (microprocessors, ASICs, and memories) migrate to 3.3 V at different rates.

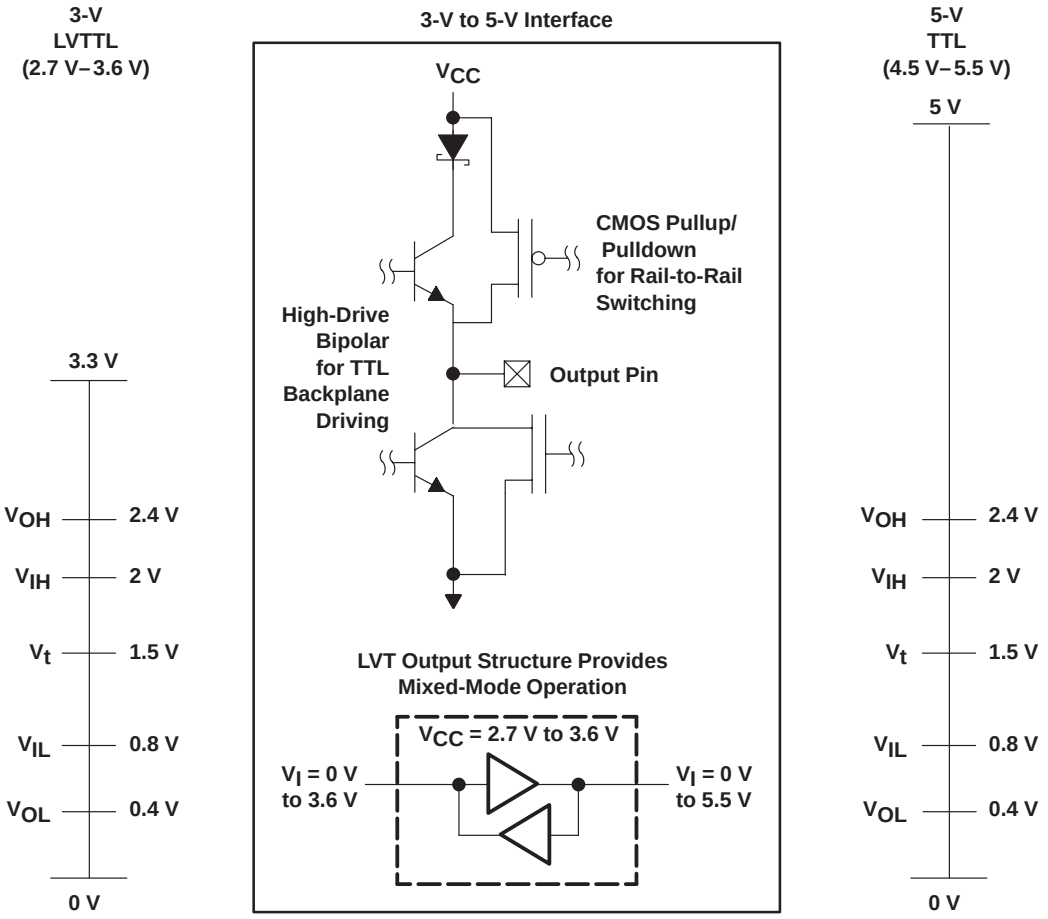


Figure 8. LVT Provides Optimized 3.3-V I/O

LVT I/O circuitry provides multiple output-current ratings for multiple system requirements. LVT devices are specified to drive at rail-to-rail low-voltage CMOS levels and standard 5-V TTL levels. LVT employs bus-hold and power-on-demand circuits increasing reliability, decreasing discrete component count, and minimizing enabled and disabled static power consumption. Maximum I_{CCL}, I_{CCH}, and I_{CCZ} current specifications are 5 mA, 0.1 mA, and 0.1 mA, respectively.

The majority of traditional telecom end equipments can be divided into switching and transmission categories. Switching equipment, such as central offices, cross connects, and branch exchanges, are analogous to large mainframes or supercomputers. ABT octal and Widebus™ product families are targeted for these telecom equipments.

For transmission equipment, such as line cards, bridgers, and routers, products with enhanced data-sheet specifications covering hot-card insertion and power up/down are required. In these applications, a board (card) typically is removed (inserted) from an active (hot) system for upgrade, maintenance, or repair. The additional specifications characterize the device's performance when supply currents change (ramp) rapidly.

It is necessary to know how the device behaves when V_{CC} is 0 V, when V_{CC} is at the rail (5.5 V), and when V_{CC} ramps between these voltages. To address this requirement specifically for telecom transmission applications, ABT transceiver data sheets take into account I_I, I_{OZH}, I_{OZL}, and I_{OZ} current conditions for various V_{CC} ramp rates. Transmission-system designers can then profile ABT device performance in hot-card insertion and power up/down conditions.

Summary

TI provides the system designer with the most advanced products to date, aiding the solution of complex design challenges. Advanced bus-interface logic (ABIL) products processed in submicron advanced BiCMOS technologies (ABT) address specific end-equipment demands of the workstation, personal and portable computer, and telecom markets. Advanced fine-pitch package options, such as SSOP, TSSOP, and TQFP, offer space-saving form factors. Circuit design techniques, such as bus hold and power on demand, add value over competitive solutions.

The evolutionary development of process and package technologies is illustrated in Figure 9. Solid lines indicate process-technology migration for CMOS and BiCMOS. The minimum process dimension is represented on the ordinate in units of microns. The dashed line indicates package-technology migration from PDIP to SOIC to SSOP to TQFP. For the dashed line, the ordinate represents minimum lead pitch in millimeters.

Figure 9 shows some interesting trends. BiCMOS solutions, initially well behind their CMOS cousins in terms of performance, have closed the gap almost completely during the past six years. For 5-V logic applications, ABT offers significant advantages over an equivalent CMOS version, particularly with the advent of thermally enhanced fine-pitch packages like the TQFP.

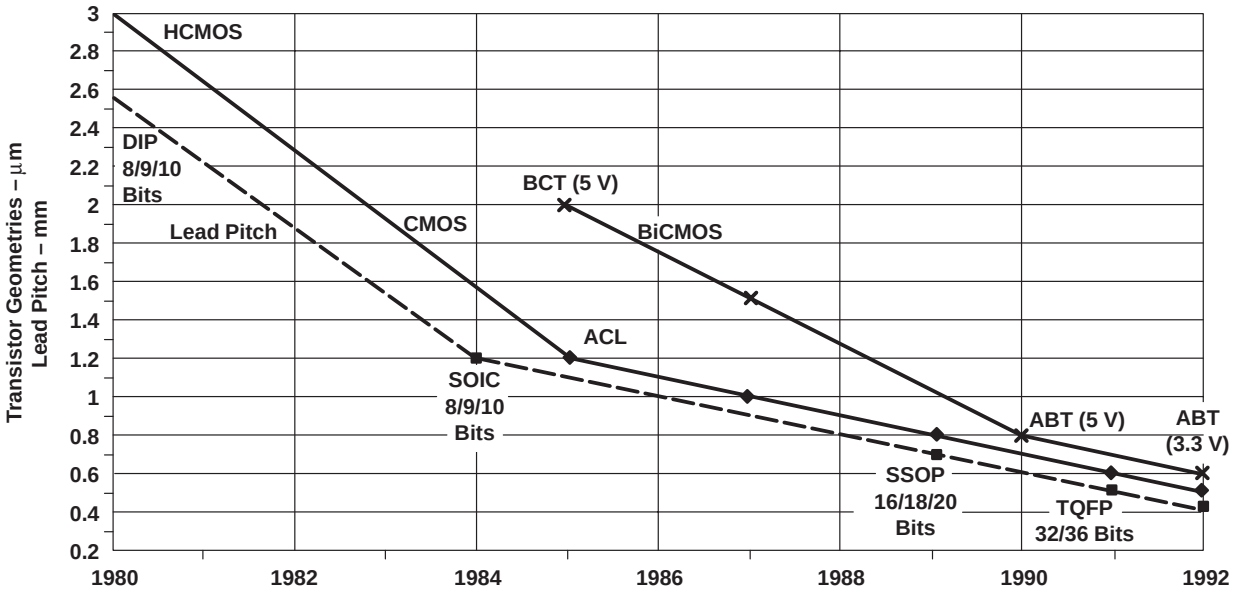


Figure 9. Bus-Interface Evolution

The advanced BiCMOS opportunity is to provide more processing capability and overall throughput at a time when the next-generation CMOS technologies are not quite ready, or where a mixed-technology approach provides a more practical solution. For ABIL products, the high performance and drive capability of ABT are necessary for rack-mount supercomputers, workstations, and telecom switching equipment. However, the low power consumption of ABT is necessary if these end equipments are to migrate to the desktop.

As process geometries drop to 0.6 μm and below, advanced BiCMOS and advanced CMOS will continue to compete in the pursuit of the best low-voltage solutions. Future enhancements to advanced BiCMOS might include extensions to a complementary structure of NPN and PNP transistors to better cope with reduction in power-supply voltages. As supply voltages drop to 2.6 V and below, it appears likely that advanced BiCMOS and advanced CMOS will coexist as viable product technologies, each supporting a dedicated group of customers. Time will tell.