CDCLVP111-SP Evaluation Module (CDCLVP111EVM-CVAL)

This user's guide provides an overview of the evaluation module (EVM) including hardware features to be considered while using this module. This manual is applicable to the CDCLVP111-SP EVM which is synonymous with CDCLVP111EVM-CVAL, the orderable part number. The EVM provides a platform for evaluating the clock buffer under various voltage and bias configurations.

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Trademarks

1 CDCLVP111-SP EVM (CDCLVP111EVM-CVAL)

The CDCLVP111-SP EVM is ideal for evaluating the CDCLVP111-SP. The CDCLVP111-SP is a 1 to 10 LVPECL buffer with selectable input. The evaluation setup is shown in Figure 1. The evaluation setup is essentially a break-out board exposing full functionality of the device with flexible input and output-biasing options.

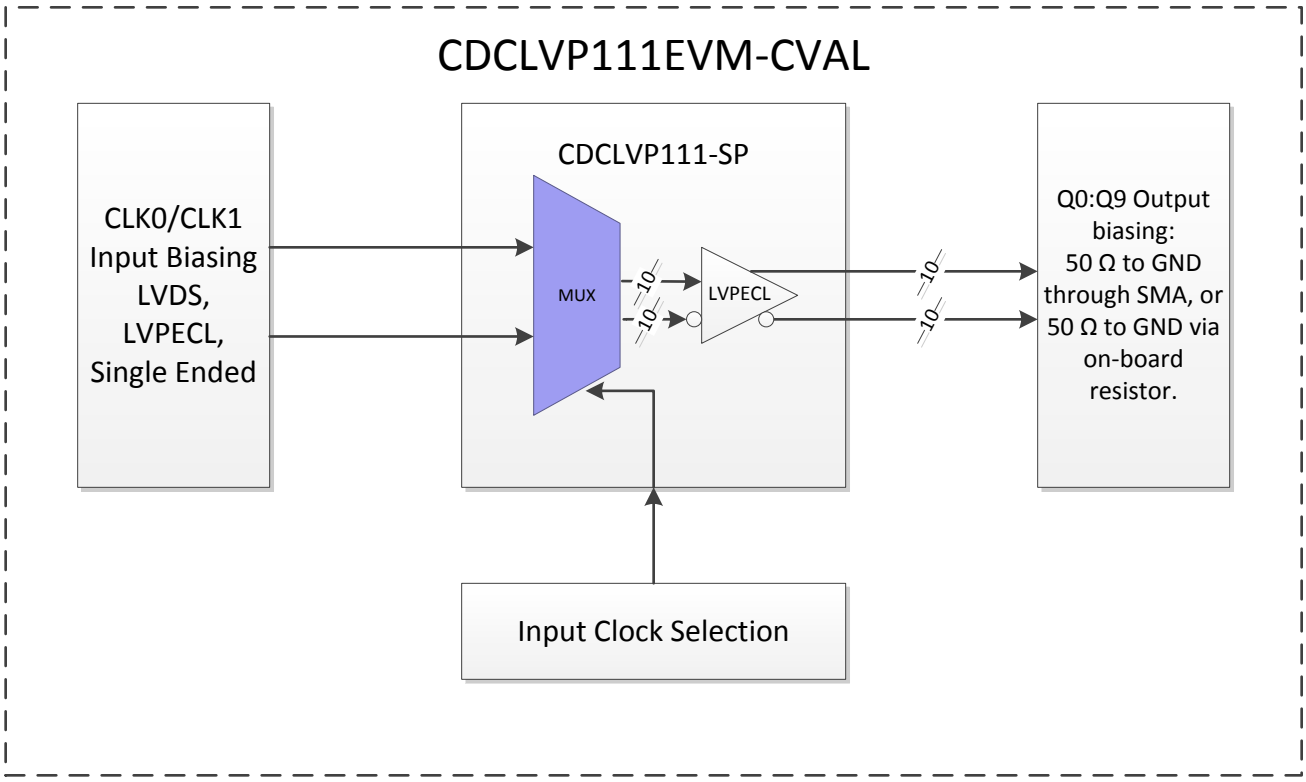

Figure 1. CDCLVP111-SP EVM Block Diagram

2 CDCLVP111-SP Setup and Quick Test

The CDCLVP111-SP EVM is designed to ease lab-based evaluation by utilizing an offset LVPECL bias point set to earth ground. This allows a two power supply setup to easily connect the outputs to standard 50-Ω terminated test equipment. Connecting this way provides the proper termination for LVPECL drivers. The EVM also provides pads near SMA jacks for on-board 50-Ω termination for cases that may desire to utilize high-impedance probes.

2.1 Power Supply Setup

Figure 2 illustrates the necessary power connections for 3.3-V VCC-to-VEE operation.

- With supply 1 disabled, program supply 1 to 3.3 V with 100-mA current limit
- With supply 2 disabled, program supply 2 to 2 V with 100-mA current limit

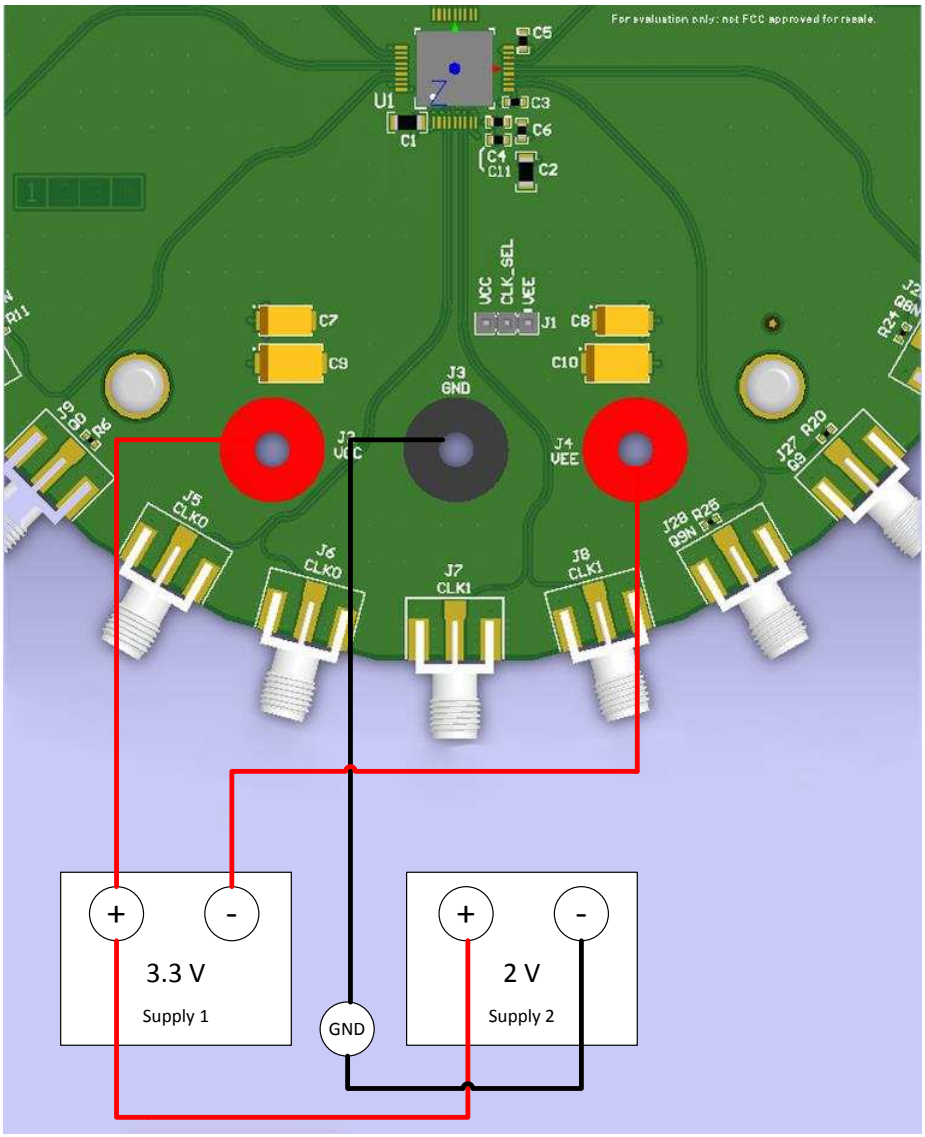

Figure 2. Power Supply Connections

(A) Connect supplies and board with banana cables as shown. This configuration is for nominal 3.3-V testing. To configure other VCC-to-VEE voltages, program supply 1 to the proper range of 2.375 V to 3.8 V. Supply 2 remains fixed with 2-V offset from VCC to earth ground termination.

(B) With the signal generator disabled, program according to Table 1 based on the supply voltage used. Note, that the amplitudes and offsets are based on a single-ended signal.

Table 1. Power Supply Configuration

Voltage	VCC:VEE	VCC-GND	CLK[0:1] amplitude	CLK[0:1] offset
MIN	2.375 V	2 V	500 mV	0.625 V
TYP	3.3 V	2 V	500 mV	–0.3 V
MAX	3.8 V	2 V	500 mV	–0.8 V

(C) This configuration provides a 1 V peak-to-peak differential clock with appropriate offset relative to earth ground (LVPECL termination point).

(D) Connect 1 or more output pairs to a 50-Ω terminated oscilloscope.

(E) Connect signal generator to CLK0 and nCLK0.

(F) Ensure that J1 is open or set between pins 1 and 2. This enables CLK0. Jumper pins 2 and 3 for CLK1 pair.

(G) Enable power supply 1 and 2.

(H) Enable signal generator outputs.

(I) View outputs on oscilloscope screen.

3 CDCLVP111-SP EVM Description

The following sub-sections describe the CDCLVP111-SP EVM in detail.

3.1 CDCLVP111-SP Clock Mux Selection

The EVM provides a three-pin jumper, J1, to select CLK0 or CLK1 pairs.

Table 2. CDCLVP111-SP Jumper Configuration

Reference Designator	# of Pins	Default Config	Pin 1 Silkscreen	Pin 2 Silkscreen	Pin 3 Silkscreen
J1	3	Short pins 1-2	VEE	CLK_SEL	VCC

The CDCLVP111-SP CLK_SEL pin contains a 75-kΩ pulldown to VEE. Leaving J1 without jumper will select the CLK0 pair, the same as if J1 has pins 1 and 2 shorted. Shorting J1 pins 2 and 3 will select CLK1 input pair.

3.2 CDCLVP111-SP EVM Input Biasing

The CDCLVP111-SP EVM was designed to allow implementation of flexible input biasing. By default, the board is configured with two 50-Ω resistors to LVPECL bias level (VCC-2 V, earth ground) for both CLK inputs. This configuration allows for direct use of LVPECL drivers. The termination resistors R1, R2, R4, and R5 are placed on the bottom side of the board in a fly-by configuration.

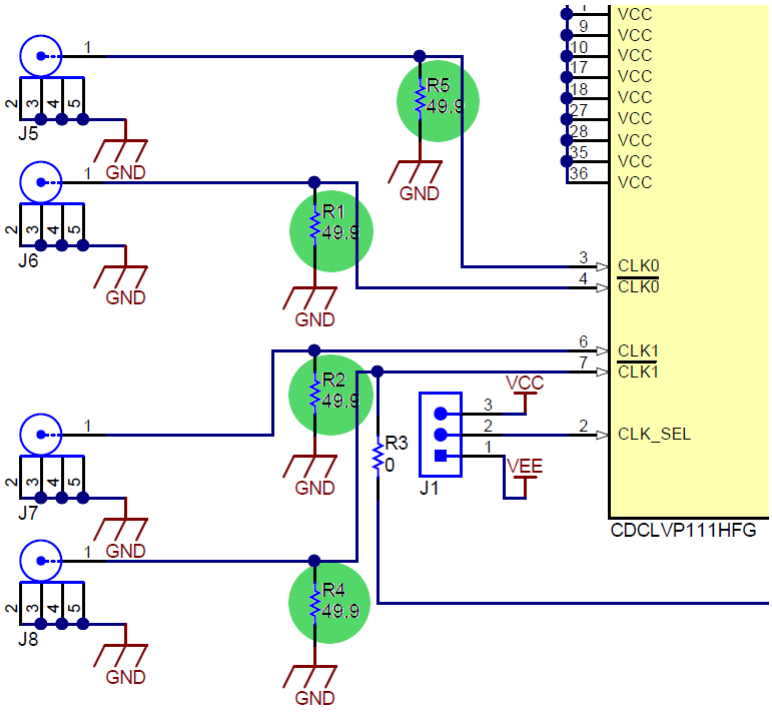

Figure 3. Input Biasing Schematic

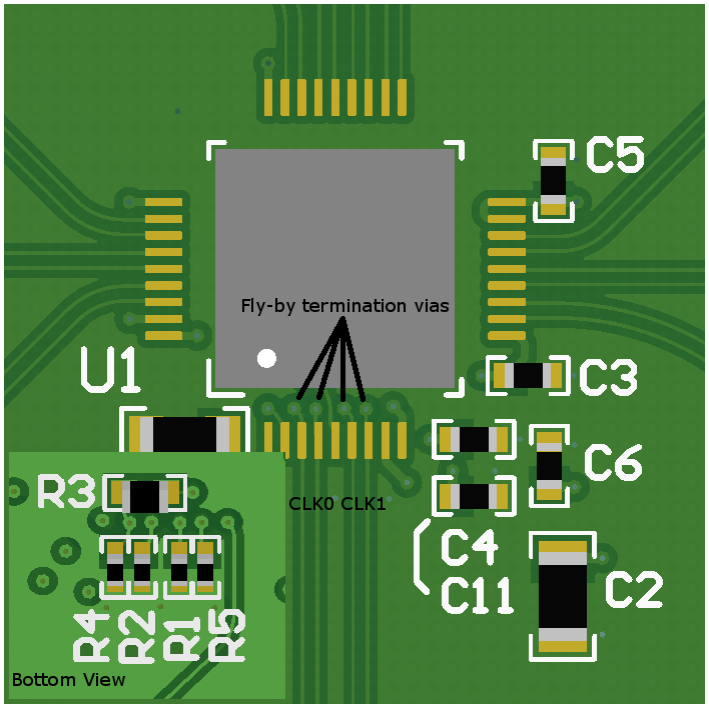

Figure 4. Input Biasing Board View

The board also is designed to allow LVDS termination. This is accomplished by the careful layout of R1, R2, R4 and R5. The pad placements are such that an 0402 100-Ω resistor can be placed between the top pads of R1 and R5 or R2 and R4 to differentially terminate either CLK0 or CLK1 pairs respectively (see Figure 5).

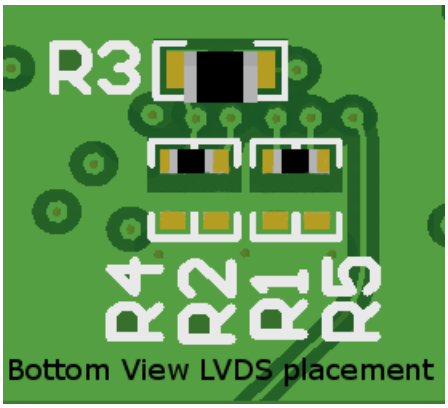

Figure 5. LVDS Termination

The final termination option is to allow single-ended input to drive CLK1. A 0-Ω resistor, R3, can be added to the circuit to connect VBB output to the negative pin of CLK1. Remove resistor R2 and R4. A single-ended signal can now drive CLK1 input on J7.

3.3 CDCLVP111-SP EVM Output Termination

The CDCLVP111-SP EVM is configured with no on-board output termination installed, by default. This allows simple connection to 50-Ω terminated test equipment. There are 0402 pads for 50-Ω termination on board. This allows the connection of a high- impedance or differential probe. Simply install the pair of resistors associated with the output being evaluated. In Figure 6, install R7 and R12 for on-board termination. Leave them unconnected for direct termination to 50-Ω test equipment.

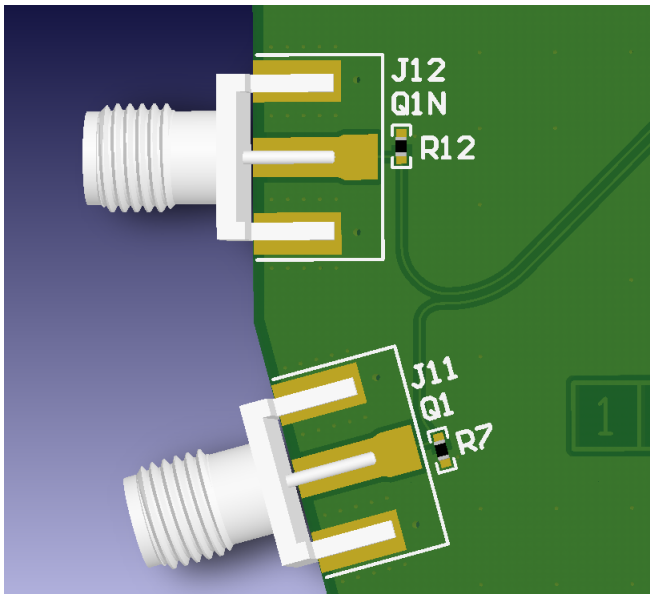

Figure 6. On Board Optional Output Termination

4 CDCLVP111-SP EVM Schematic

Figure 7 illustrates the EVM schematic.

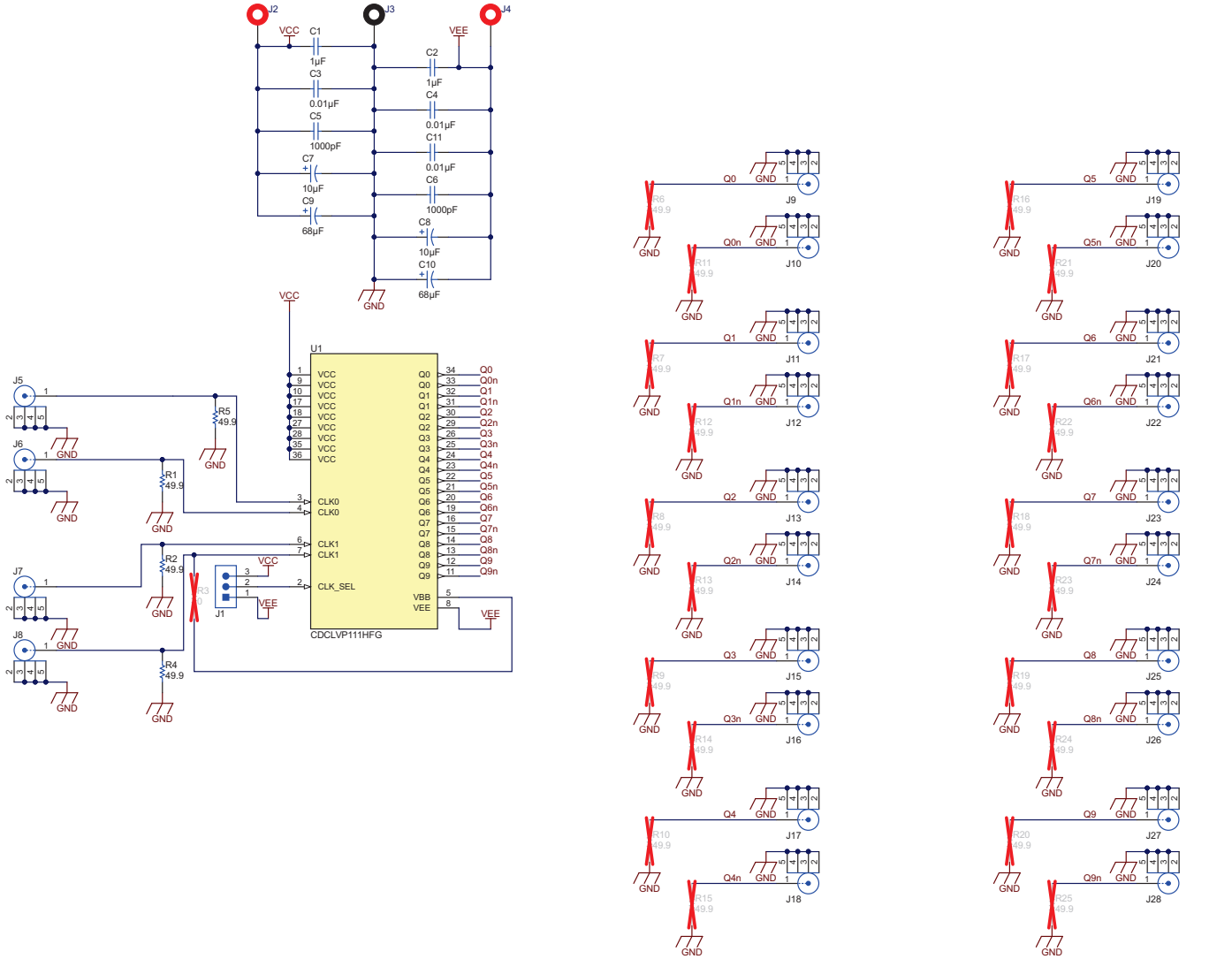

Figure 7. CDCLVP111-SP Schematic

5 CDCLVP111-SP EVM Bill of Materials (BOM)

Table 3 displays the BOM.

Table 3. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		MHR030	Any
C1, C2	2	1uF	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 1206	1206	C3216X7R1E105K085AA	TDK
C3, C4, C11	3	0.01uF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C5, C6	2	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C102K5RACTU	Kemet
C7, C8	2	10uF	CAP, TA, 10 µF, 25 V, +/- 20%, 1.5 ohm, SMD	6032-28	293D106X0025C2TE3	Vishay-Sprague
C9, C10	2	68uF	CAP, TA, 68 µF, 25 V, +/- 10%, 0.2 ohm, SMD	7343-43	T495X686K025ATE200	Kemet
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Header, 2.54 mm, 3x1, Tin, TH	Header, 2.54 mm, 3x1, TH	TSW-103-07-T-S	Samtec
J2, J4	2		BANANA JACK, SOLDER LUG, RED, TH	Red Insulated Banana Jack	SPC15363	Tenma
J3	1		BANANA JACK, SOLDER LUG, BLACK, TH	Black Insulated Banana Jack	SPC15354	Tenma
J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28	24		JACK, SMA, 50 Ohm, Gold, SMT	SMA JACK EDGE MNT, SMT	73251-1150	Molex
R1, R2, R4, R5	4	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America
SH-J1	1		Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
U1	1		CDCLVP111HFG, HFG0036A_Custom_A	HFG0036A_Custom_A	CDCLVP111HFG	Texas Instruments
R3	0	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25	0	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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