Application Report
SCAA094–November 2008

CDCE62005 as Clocking Solution for High-Speed Analog-to-Digital Converters

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ABSTRACT

Texas Instruments has introduced a family of devices well-suited to meet the demands for high-speed analog-to-digital converter (ADC) devices such as the ADS5527, which is capable of sampling up to 210 MSPS. To realize the full potential of these high-performance devices, it is imperative to provide a low phase noise clock source. The CDCE62005 clock synthesizer chip offers a real-world clocking solution to meet these stringent requirements for high-speed ADCs. This application report highlights the limiting agents associated with the clock source that adversely affect the ADC signal-to-noise performance. The performance of the ADS5527 ADC clocked with the CDCE62005 is shown and compared to ideal baseline performance. Additional improvement topologies are presented, along with measured results that show the CDCE62005 can meet or exceed the specifications at high sampling rates, and even at the more demanding high input frequencies.

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1 Introduction

New transceiver architectures and power amplifier (PA) linearization techniques are being investigated with the introduction of low-power, medium-to-high sampling rate, and high input frequency (IF) capability ADCs. For example, digital predistortion requires high sampling rate ADCs to convert the output spectrum of the PA, including the desired signal and the third- and fifth-order intermodulation products, for linearization processing. The bandwidth requirements for a multi-carrier WCDMA PA can be as high as 100 MHz. This condition, in turn, requires high sampling rate ADCs to suitably capture the signal.

For new receiver designs with multi-carrier signals that incorporate cost-saving topologies, there is a need for high IF sampling ADCs. This type of architecture effectively eliminates the need for a second analog miner or analog demodulator that simplifies the receiver architecture. A high IF ADC is necessary to sample the signal at these frequencies with sufficient purity for advanced telecommunication standards.

Texas Instruments offers a series of high IF, high sampling rate ADCs suitable for the wireless infrastructure market. The ADS5527 is an industry-leading, 12-bit, 170-MSPS ADC capable of achieving good SNR performance with high input frequency signals. In order to realize the full potential of these types of devices, it is important that the clock source have low phase noise. This requirement is often overlooked when evaluating and designing with high-end ADCs. Furthermore, although a suitable source may be used for evaluating purposes, finding a board-level solution often proves difficult.

Texas Instruments has introduced a board-level, low phase noise clocking solution for the ADS5527 and other high-speed ADC devices (up to 12 bits) using the CDCE62005 clock synthesizer chip. With proper configuration, the CDCE62005 can be used with high-speed ADCs to achieve ideal performance suitable for direct implementation into printed circuit board (PCB) designs. In addition, the CDCE62005 has the ability to drive five independent outputs that can be independently divided down. This feature allows one clock circuit to provide a clock source for not only a high-performance ADC, but also the other devices on the board that require an independent clock such as digital-to-analog converters (DACs), digital down-converters (DDCs), and digital up-converters (DUCs). Figure 1 illustrates how the CDCE62005 is used with an ADC and other devices in a typical transceiver block diagram.

Figure 2 shows how the CDCE62005 can be used in an ultrasound medical imaging application, with the AFE5805 analog front-end integrated chipset from TI. This device includes a low-noise amplifier (LNA), a voltage-controlled attenuator (VCA), a programmable-gain amplifier (PGA), and an octal 12-bit ADC.

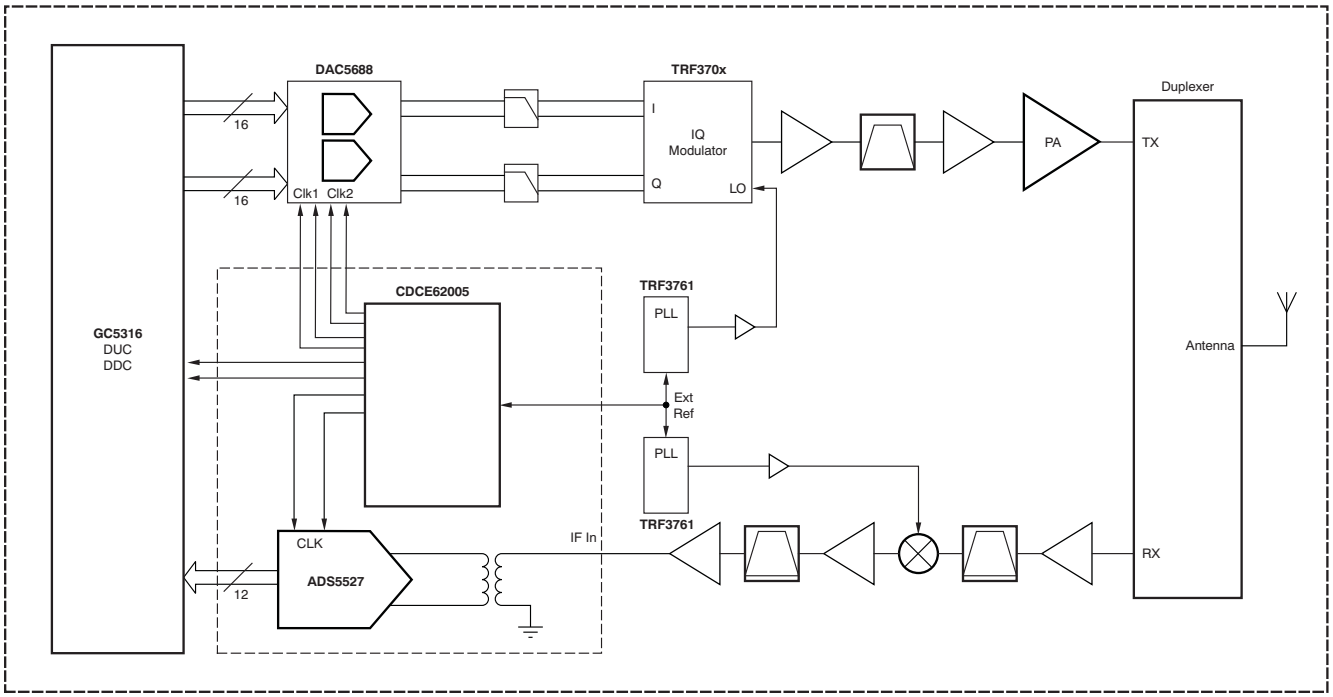

Figure 1. ADS5527 with CDCE62005 Clocking Solution within a Typical Base Station Application

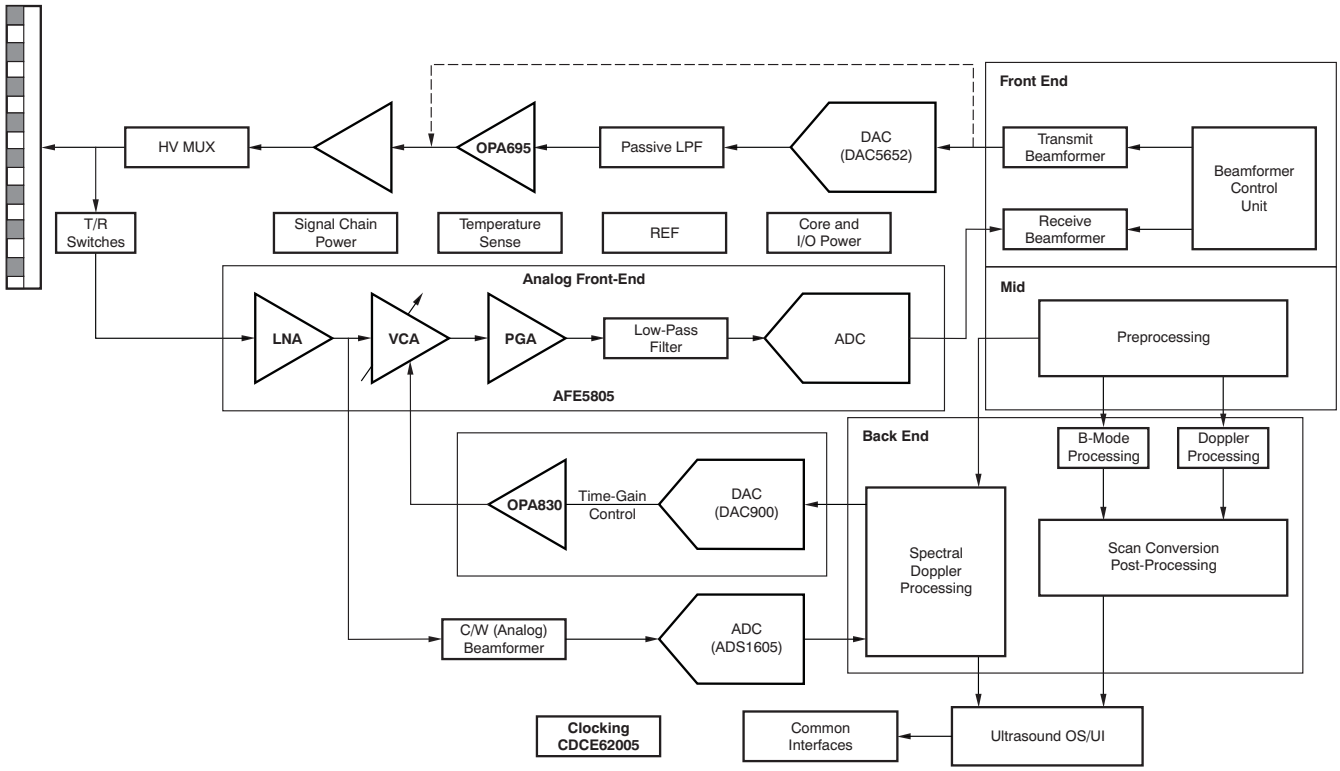

Figure 2. AFE5805 with CDCE62005 Clocking Solution within a Typical Medical Ultrasound Application

2 High IF Sampling Challenges

Clock jitter is defined as the random variation of the clock position compared to its ideal position with respect to time. When the position of the clock varies slightly, it alters the position of the sampling point, which in turn samples the input waveform at an imprecise location. This error manifests itself as a signal-to-noise (SNR) degradation.

The SNR degradation attributed to the jitter of the clock and jitter inherent to the ADC is defined as:

$$SNR_T = -20\log\left[\frac{\frac{V_{FS}}{2}(2\pi f_{IN})10^{\frac{V_{IN}}{2}}t_J}{\sqrt{2}}\right] \quad (1)$$

Where:

- V_{FS} = Full-scale voltage of the ADC
- V_{IN} = Relative input amplitude of the signal compared to Vfs expressed in dBFS
- f_{IN} = Input frequency
- t_J = Total system jitter in seconds

The total system jitter is defined as:

$$t_J = \sqrt{t^2_{ADC} + t^2_{CLK}} \quad (2)$$

Where:

- t_{ADC} = Aperture jitter of the ADC in seconds
- t_{CLK} = Clock jitter in seconds

Note that the SNR degradation as a result of clock jitter is independent of the sampling rate; however, it depends on the input frequency. For much smaller input frequencies (relative to the sampling frequency), SNR degradation occurs because of the quantization noise limitation of the ADC and not from the clock jitter. For a given amount of clock jitter, it can also be seen from the above equations that a higher IF input signal will be more susceptible to SNR degradation. This phenomenon is illustrated in Figure 3.

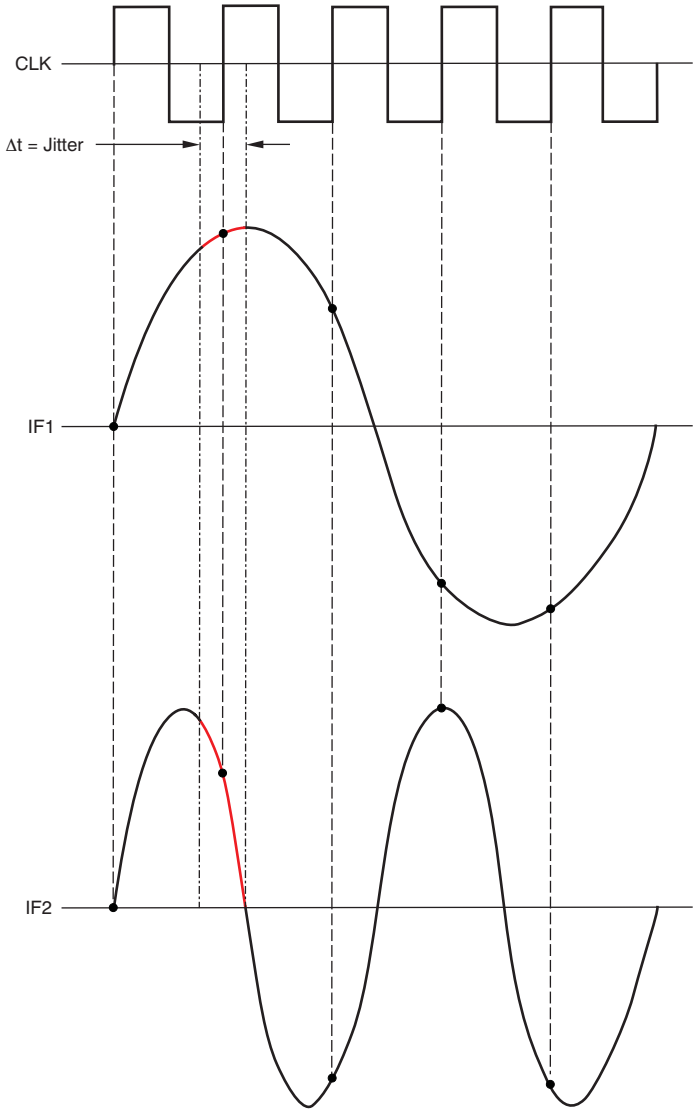

Figure 3. SNR Degradation Caused by Jitter for Different IF Input Signals

Figure 3 depicts two IF input signals at different frequencies. An ideal clock source with a given amount of jitter samples each signal. The ideal sampling point is shown at the dot, but the jitter will alter the exact point where the signal is sampled. The potential points that could be sampled are depicted by the bold red line between the dashes. The error line on the lower frequency signal is smaller than the error line on the higher frequency signal. As a result, the higher IF signal will have higher SNR degradation because of clock jitter. The integration limits (important for the ADC SNR performance) for the jitter of the clock source from its phase noise profile can be obtained from the standards that the system would adhere to.

Figure 4 shows the measured performance versus predicted performance of the ADS5527 at a sampling frequency of 122.88 MSPS.

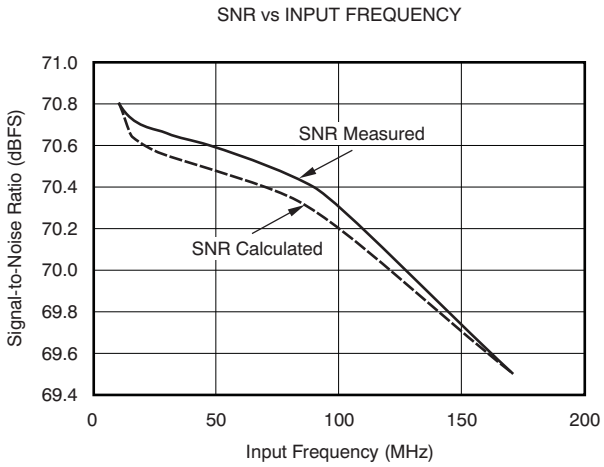

Figure 4. Measured vs Predicted SNR Performance Over Input Frequency

The predicted values closely match with the measured data for the device. As such, these equations can be used to predict performance at any desired input frequency.

3 Effect of Clock Amplitude

With an ideal square-wave clock, the sampling is completed at the zero crossings of the waveform. Furthermore, in some ADC components such as the ADS5527, data are sampled and latched using the up and down cycles of the clock; therefore, it is important for the clock to maintain a 50% duty cycle. Previously, it was shown that jitter affects the sampling position of the input waveform, which degrades SNR performance. Thermal noise from a non-ideal clock also contributes to SNR degradation.

Thermal noise contributes a random amplitude vector to the clock source. With an ideal square-wave clock, the signal would swing instantaneously from one state to the other. In this scenario, slight amplitude variations as a result of noise would have no effect on the transition sampling point. In practical terms, however, even with a good square-wave clock, the transition from one state to the other is not instantaneous. There is a finite time during which the transition occurs. Noise on the waveform alters the signal such that the crossover points occur slightly off the ideal position. This offset causes a small error in the sampling point that degrades SNR. Figure 5 illustrates an enlarged view of the transition slope of the clock around the crossover point with added random noise. The noise component, Δn, raises the signal to the crossover point that yields a small error Δt.

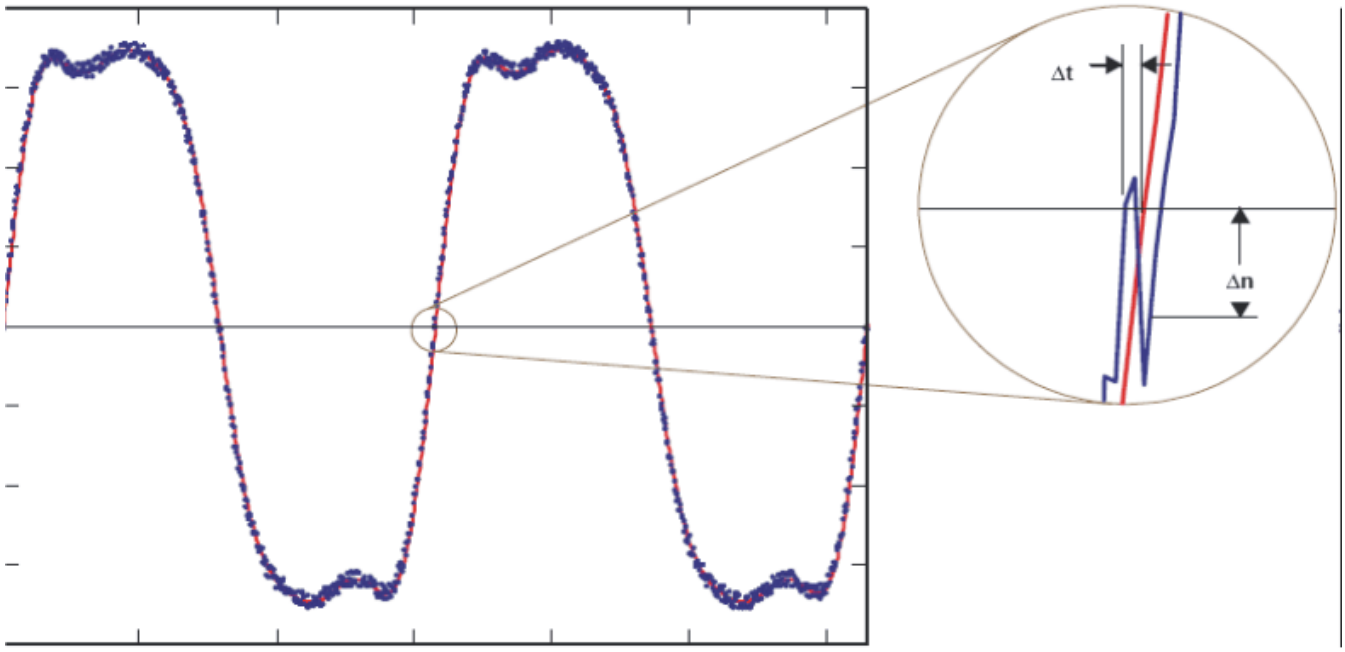

Figure 5. Sampling Error Caused by Thermal Noise Component

One way to minimize the impact of thermal noise degradation is to make the transition slope steeper. In other words, by increasing the transition slope of the clock signal, the signal more closely approximates the ideal square wave clock. Conversely, a less inclined transition slope is more susceptible to SNR degradation as a result of thermal noise. Figure 6 illustrates two clock signal transition slopes, each subjected with the same thermal noise profile. The noise component is equal for both transition slopes; but the resultant timing error, Δt, is larger for the shallower slope. For this reason, it is desirable to keep the transition slopes as steep as possible in order to minimize the effects of thermal noise.

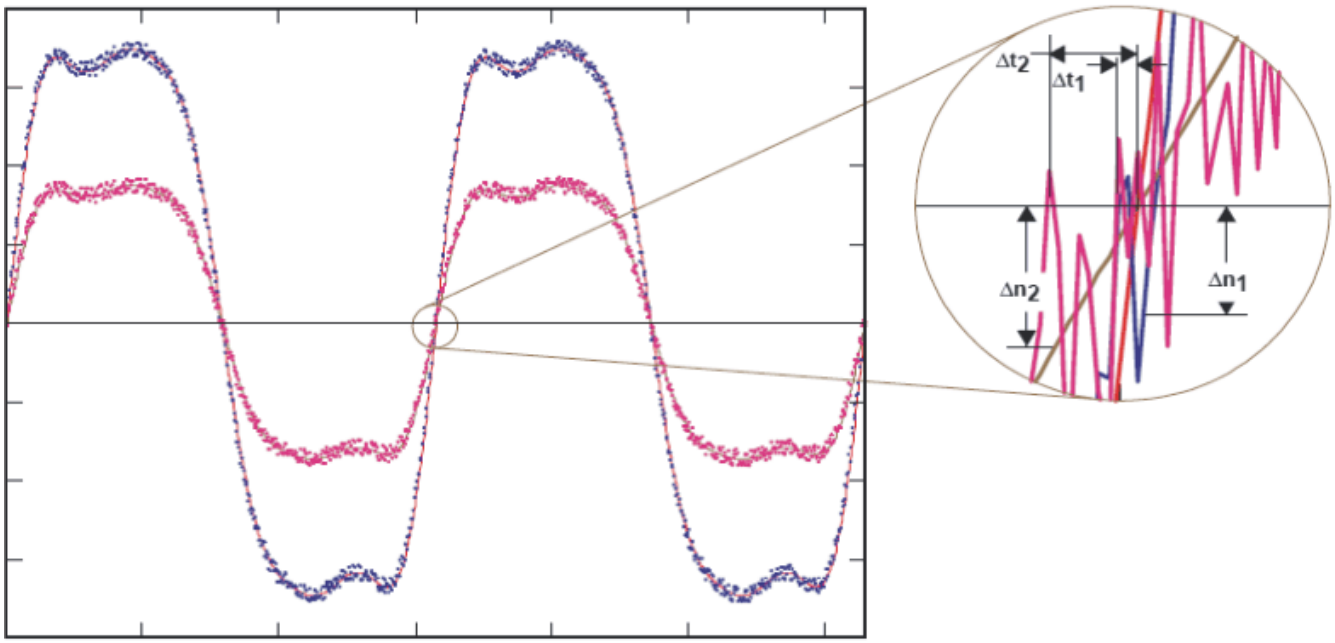

Figure 6. Thermal Noise Effect for Different Slope Clock Signals

For very high IF input frequencies, the thermal noise component of the clock can be further minimized by including a band-pass filter at the clock input, centered at the clock frequency of choice. Any suitable band-pass filter topology will suffice, such as an L-C filter, a SAW filter, or a crystal filter. Because the clock frequency is only a single tone, the most narrow bandwidth filter produces the best results.

The inclusion of a band-pass filter around the clock minimizes noise outside the filter bandwidth, but it also affects the transition slope of the clock signal. A square-wave clock signal consists of a fundamental tone and a series of higher-order harmonics. By inserting the narrow band-pass filter, the higher harmonics of the clock signal are eliminated. The result is a pure fundamental tone in the frequency domain or a pure sine wave in the time domain. Though the filter effectively minimizes the noise components, it also inadvertently reduces the transition slope of the clock signal, because the transition of a sine-wave is shallower than that of a square wave. As shown previously, this shallower transition becomes more susceptible to noise contributions. The band-pass filter not only removes the harmonics of the clock signal (resulting in a sine-wave output signal), it also introduces 2 dB to 6 dB of insertion loss. This insertion loss further reduces the amplitude of the clock signal and reduces the transition slope of the signal. In order to maintain sharp transitions, the amplitude of the sine-wave signal must be increased.

Figure 7 illustrates how the error from thermal noise is minimized as a result of a higher amplitude sine-wave signal, because it effectively increases the transition slope of the signal. A transformer can be inserted after the band-pass filter to amplify the signal in order to keep the transition slope as sharp as possible.

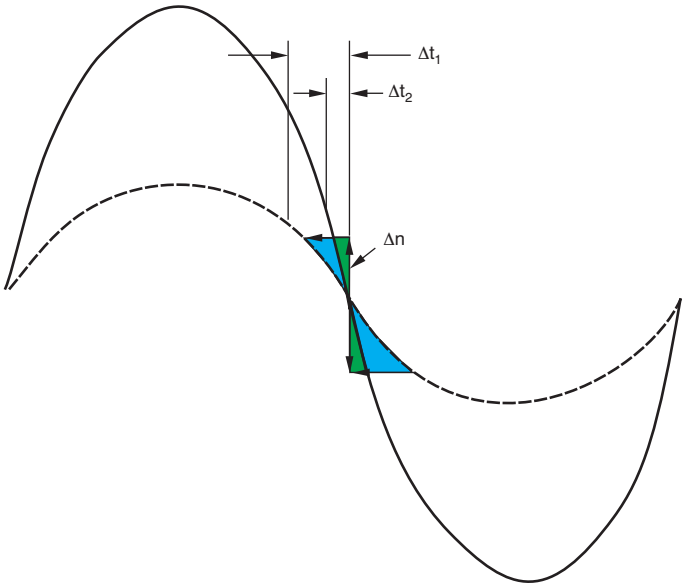

Figure 7. Thermal Noise Effect for Different Amplitude Sinusoids

4 CDCE62005 Clocking Solution

The CDCE62005 is a high-performance, low jitter differential/single-ended clock driver and clock distribution chip. It has five independently-controlled outputs, which be set to any combination of up to five differential (LVPECL or LVDS) outputs or 10 single-ended (LVMCOS) outputs that are suitable for clocking high performance ADCs such as the ADS5527. Additionaaly, this chip is able to satisfy other clocking requirements on the board as well. The CDCE72010 offers a real-word clocking solution for these applications, and can synchronize the clock output to a supplied board reference frequency.

5 CDCE62005 Interface to ADC

For low IF input frequencies to an ADC, the CDCE62005 output can be configured as a high swing LVPECL signal (which provides a 10% increase in amplitude compared to standard LVPECL) and interfaced to the ADC as shown in Figure 8. The high swing LVPECL outputs must be properly terminated; for the optimal clock signal, it is important to properly terminate the clock lines close to the ADC device to minimize reflections. Using the differential output is ideal in this case, because it minimizes the susceptibility of outside noise coupling on the line. Loop filter components for the CDCE62005 are contingent on the frequency of the VCXO and the internal PLL structure. Optionally, a simple first- or second-order LC filter can be designed at the clock outputs to minimize the impact of the reference clock spurs on the ADC SNR.

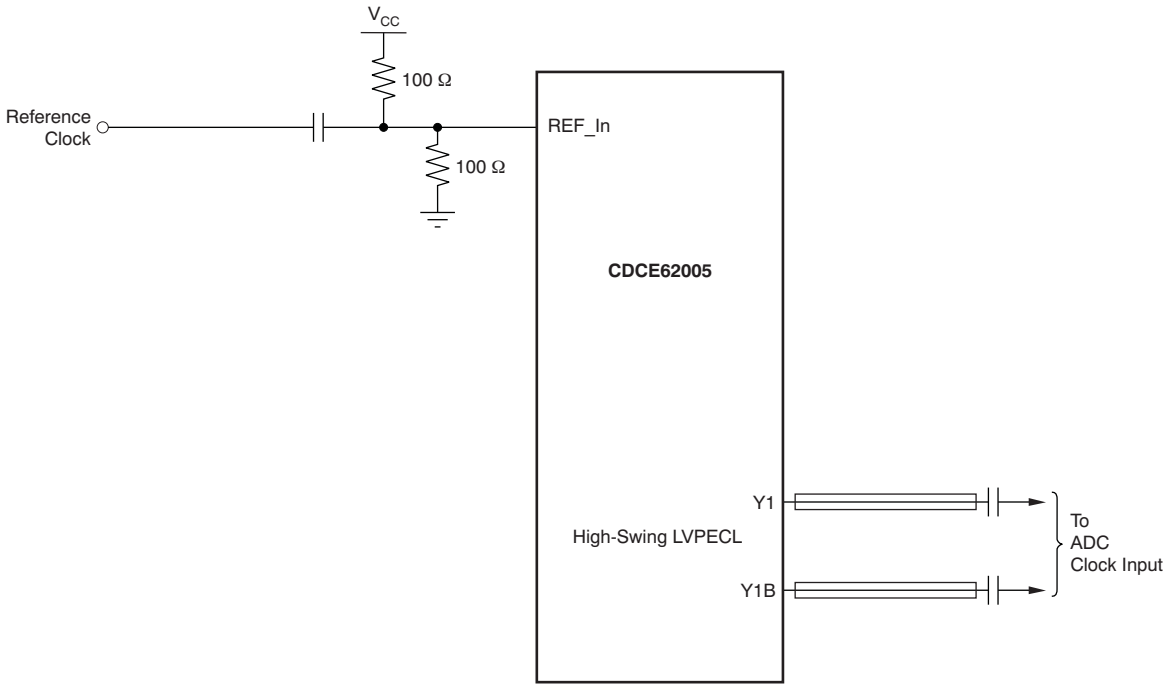

Figure 8. CDCE62005 Interface to ADCs for Low IF Input Frequencies

For medium to high IF input frequencies to the ADC, the CDCE62005 output can be configured as an LVCMOS signal and interfaced to the ADC as shown in Figure 9. The crystal filter is used to remove excessive noise from the clock signal; as a result of its high insertion loss, an LVCMOS clock is recommended for larger filtered clock amplitudes. The 4:1 transformer after the crystal filter then converts the single-ended signal to a differential signal and also boosts the amplitude. The crystal filter works best for matched 50-Ω loads; thus, care should be taken to match the lines to 50 Ω.

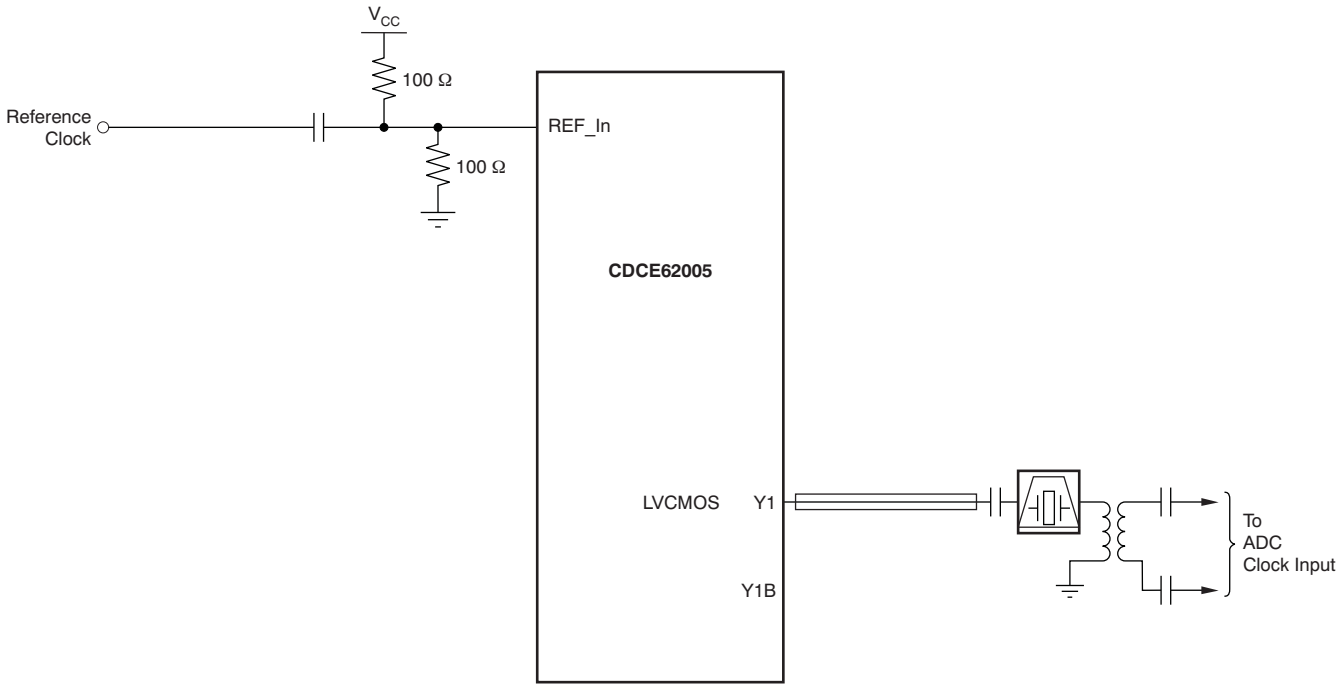

Figure 9. CDCE62005 Interface to ADCs for High IF Input Frequencies

6 CDCE62005 Clock Source for the ADS5527

To illustrate the performance of the CDCE62005 clocking solution, the device is used to supply the clock signal to the ADS5527. The data are compared to the baseline performance using an extremely good phase-noise generator with a crystal band-pass filter. Figure 10 shows the test setup.

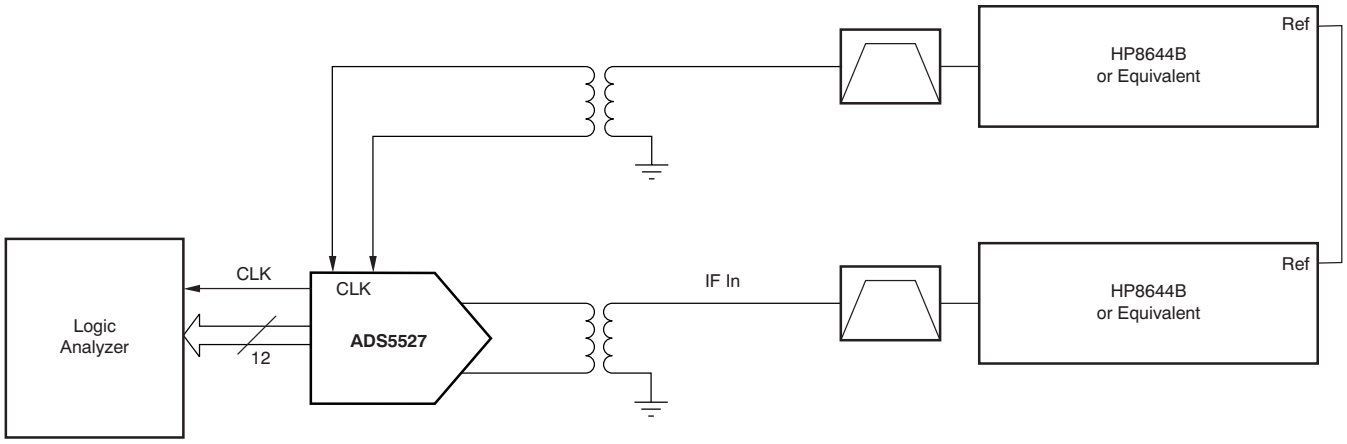

Figure 10. ADC Evaluation Test Setup (Baseline)

The measured performance of the device over frequency with a near-ideal clock source is compared to the performance using the CDCE62005 as a clock source. The block diagram of the ADC test setup incorporating the CDCE62005 is shown in Figure 11.

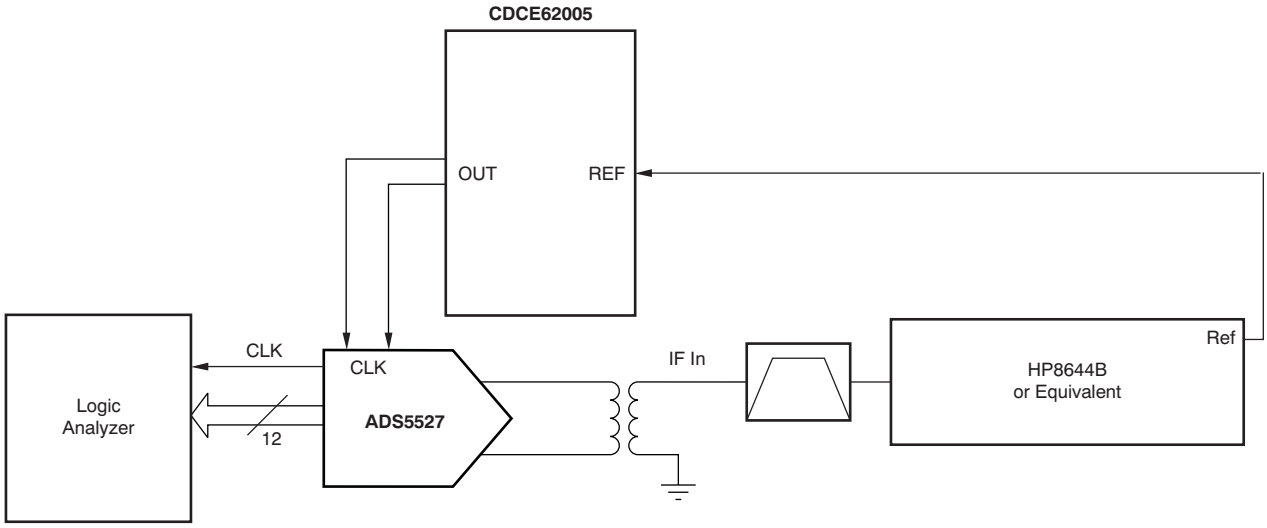

Figure 11. ADC Evaluation Test Setup with the CDCE62005 Clock Source

Measured results for the ADC SNR and SFDR (spurious free dynamic range) are shown in Table 1.

Table 1. SNR and SFDR Measurements on ADS5527

Freq (MHz)	SNR (dBFS)		SFDR (dBc)	
	Baseline	CDCE62005	Baseline	CDCE72010
5	70.9	70.6	86	85
10	70.8	70.4	86	84
20	70.7	68.7	85	83
30	70.6	66	85	81

SNR results are shown versus frequency in Figure 12, and the spectral plot of the performance at 5 MHz is displayed in Figure 13.

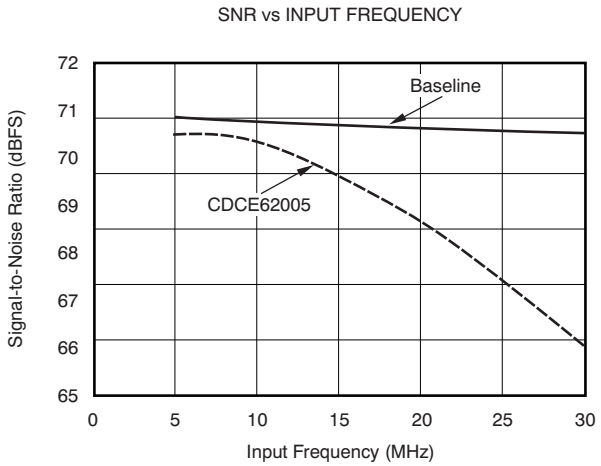

Figure 12. SNR Performance vs IF Input Frequency

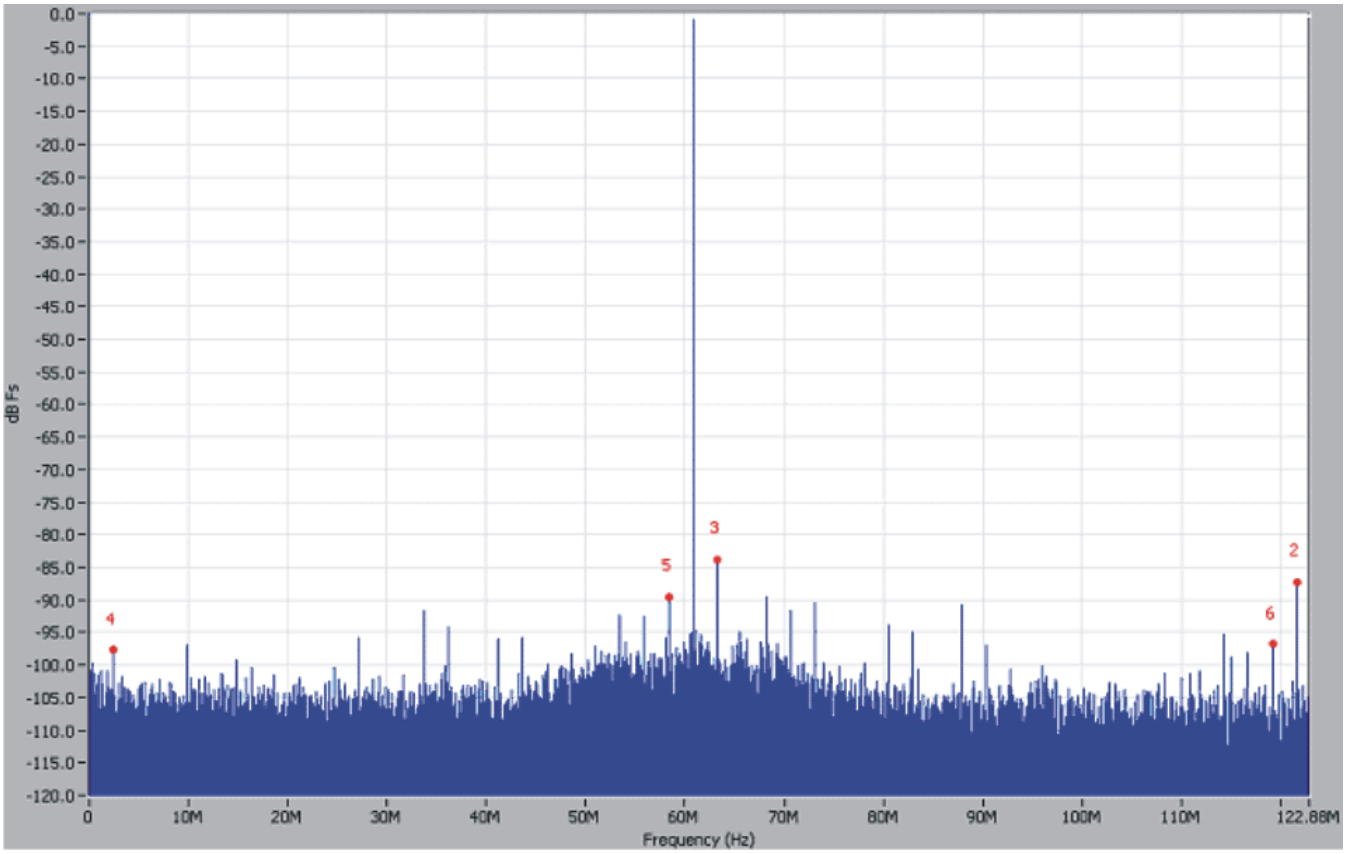

Figure 13. Spectral Performance with the CDCE62005 Clock Source at 5-MHz IF Input

For low IF frequencies, the CDCE62005 provides a suitable clock source to achieve SNR values close to the baseline performance. As expected from the analysis in Section 2, the desired performance degrades at higher IF frequencies. Because the jitter associated with the CDCE62005 is not quite as good, the SNR degradation is more severe when operating at higher IF frequencies. The SFDR performance is mostly similar to the baseline case and degrades marginally for higher IF frequencies.

7 Performance Improvements

7.1 Improved Jitter

One method to achieve performance improvement is to use a lower phase noise (or lower jitter) oscillator source for the reference input to the CDCE62005. This configuration can be achieved by using a lower jitter TCXO device. If the low jitter reference input is also of a frequency such that the CDCE62005 PFD frequency can be as high as possible, the CDCE62005 PLL loop filter bandwidth can be set as high as possible, thus taking advantage of the reference clock good near band-phase noise and switch over to the on-chip VCO phase noise when it is adequately low.

7.2 Lower Thermal Noise

As seen in Section 3, minimizing thermal noise on the clock improves the phase noise and improves SNR performance. These improvements are achieved by placing a narrowband crystal filter after the CDCE62005 LVCMOS output. The filter used is an Epson-Toyocom TF2-C2EC1 122.88-MHz crystal filter with approximately 20 kHz of total pass bandwidth. The crystal filter introduces approximately 6 dB of insertion loss. As previously discussed, the combination of the filter insertion loss and conversion from a square wave output to a sine wave output reduces the transition slope of the clock waveform. The benefit of the added filter is negated by the insertion loss and the loss of the signal slope. Adding a 4:1 transformer immediately after the filter compensates for the loss of the filter and provides steep clock transitions. It also converts the single-ended filtered clock output to a differential signal.

The phase noise of the CDCE62005 LVPECL output is shown in Figure 14; the CDCE62005 LVCMOS output coupled with the filter is shown in Figure 15. Comparing both figures, it can be seen that below the corner frequency of the band-pass filter, the performance between the two cases is nearly identical. Once the corner frequency is reached, phase noise of filtered clock output improves and rivals that of a near-identical source.

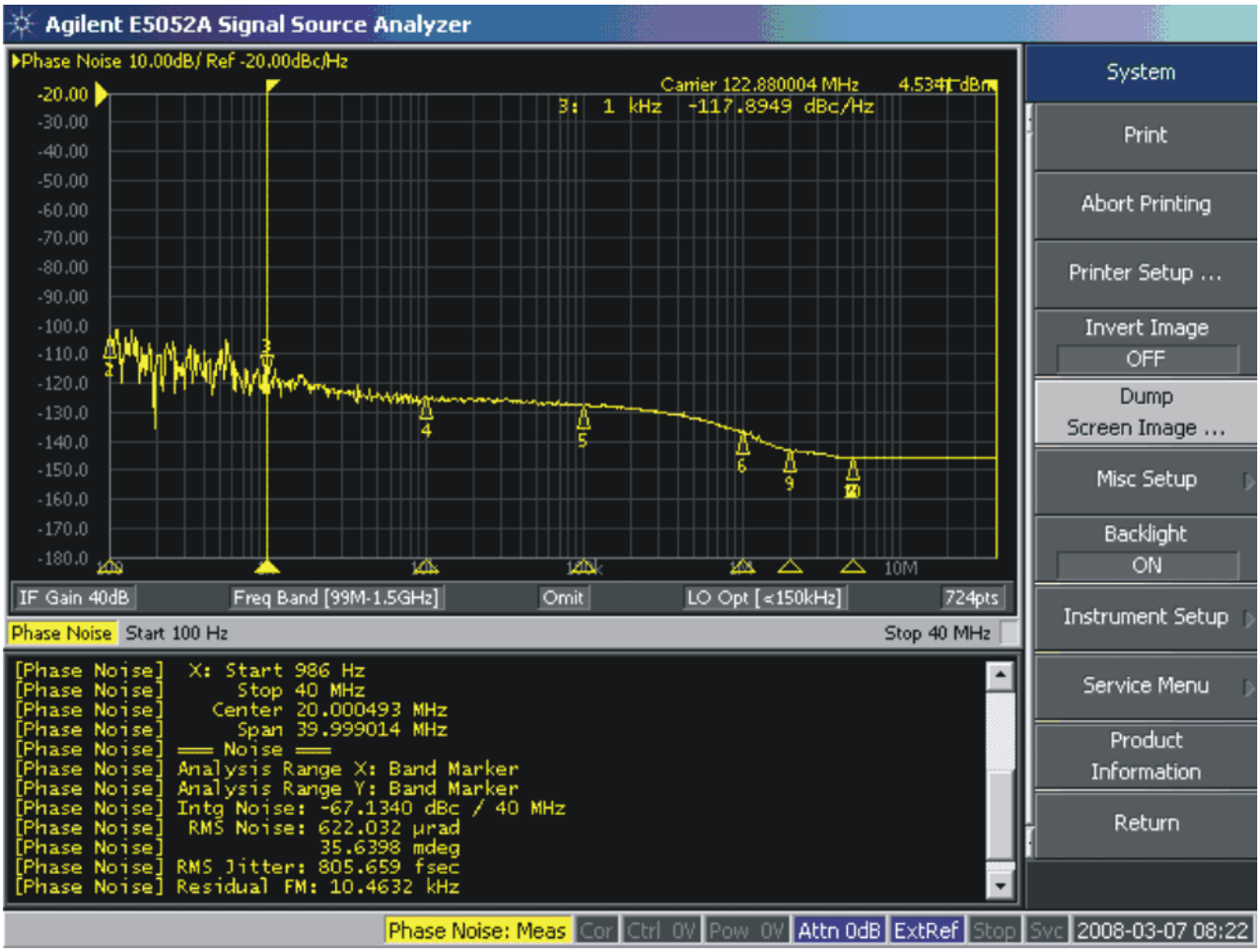

Figure 14. CDCE62005 122.88-MHz HS-LVPECL Output Phase Noise

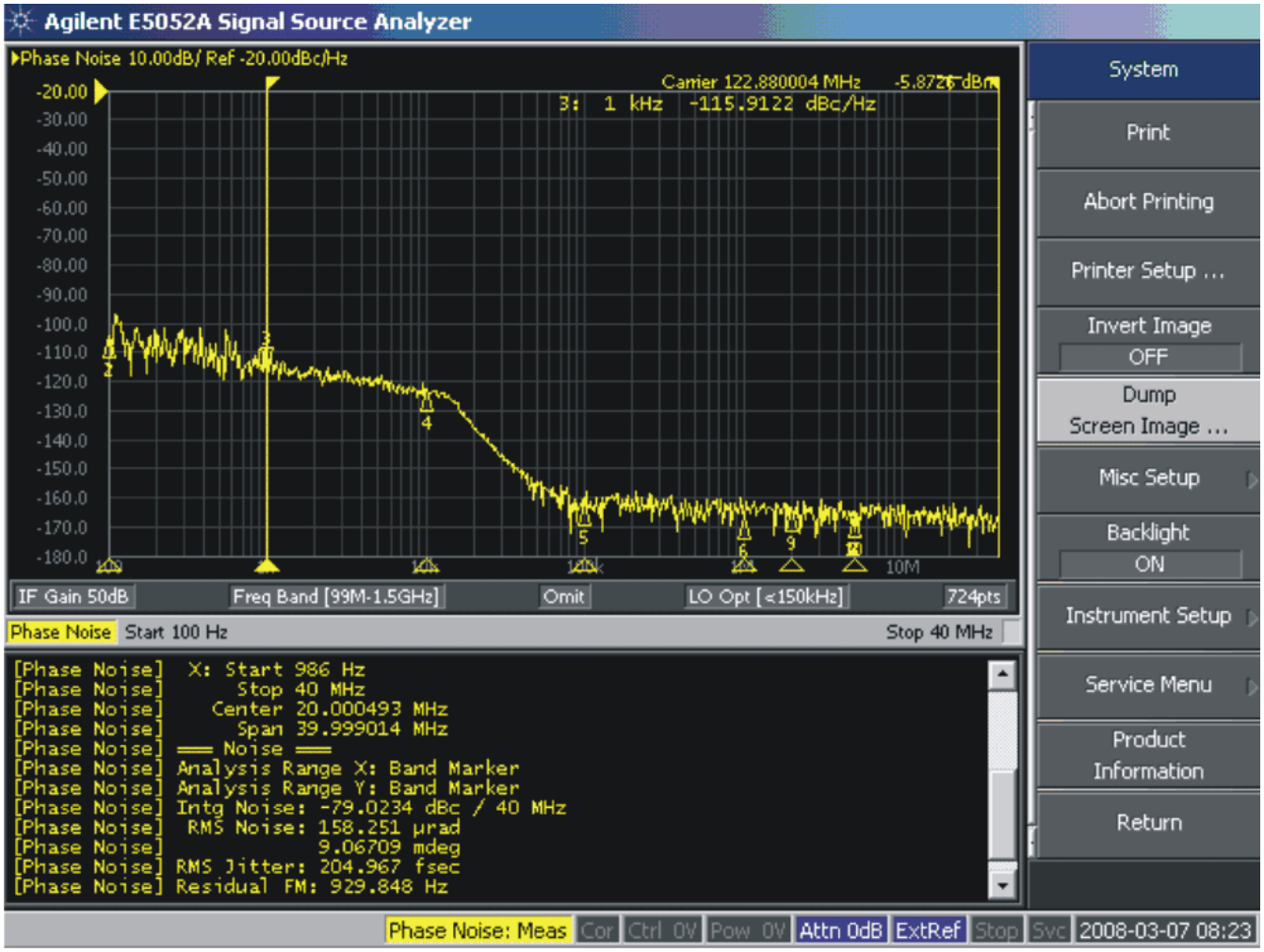

Figure 15. CDCE62005 122.88-MHz Filtered LVCMOS Output Phase Noise

The ADS5527 device is measured using the CDCE62005 and the crystal filter-transformer network. The performance is measured over higher IF input frequencies and the results are shown in Table 2.

Table 2. SNR and SFDR Measurements on ADS5527 with modified clock source

Freq (MHz)	SNR (dBFS)		SFDR (dBc)	
	Baseline	CDCE62005-BPF-Xformer	Baseline	CDCE62005-BPF-Xformer
70	70.4	70.2	84	84
100	70.3	70	78	78
170	69.6	69.3	79	78

Figure 16 compares the result of the device measured with the near-ideal clock and the CDCE62005 with crystal filter and transformer.

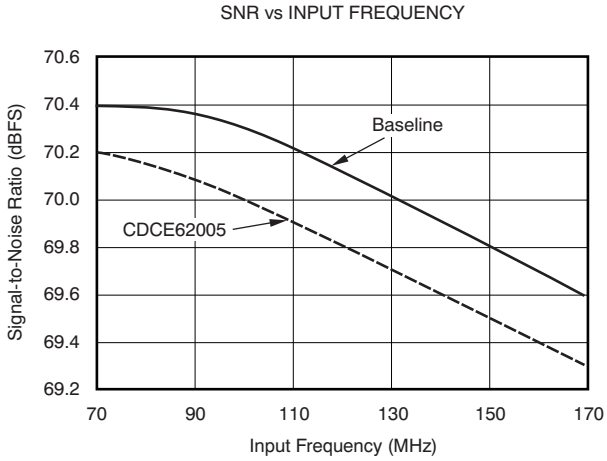

Figure 16. SNR Performance vs IF Input Frequency

Using the crystal filter-transformer combination improves SNR performance more than 5 dB at high IF frequencies and closely matches the baseline performance. SNR performance of 69d BFS or greater is achieved up to 170-MHz IF. The spectral plot of the performance at 170-MHz IF is shown in Figure 17.

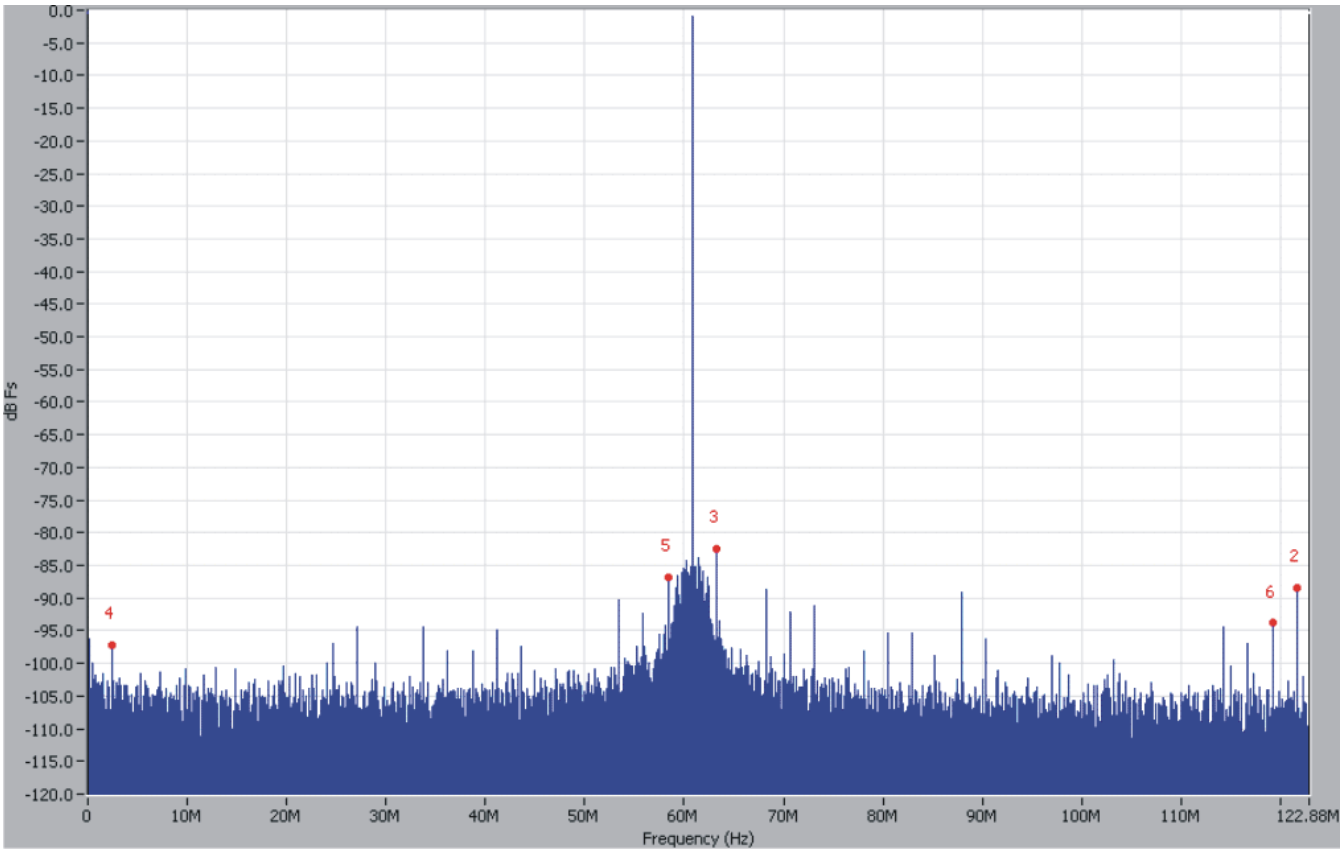

Figure 17. Spectral Performance with the CDCE62005-BPF-Transformer at 170-MHz IF Input

8 Conclusion

The CDCE62005 device is a clock synthesizer and distribution chip that satisfies stringent clocking requirements for high-end ADCs such as the ADS5527. For applications with low input frequencies, the CDCE62005 is a suitable clock for the ADC device to achieve excellent performance. For applications that requires a medium-to-high IF input frequency, the performance degrades in a linear fashion with respect to frequency. This degradation can be eliminated by including a narrow band filter, such as a crystal band-pass filter, at the output of the CDCE62005 along with a transformer to ensure sufficient clock amplitude. With this technique, near-ideal ADC performance is achievable with any desired IF frequency. Further, this technique provides an inexpensive real-world solution for clocking high speed ADCs at high IF frequencies. Additionally, the CDCE62005 can supply the clock signal, not only to the ADCs, but also the other sampled systems within the design.

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