Application Report
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CDCE72010 Phase Noise Performance and Jitter Cleaning Ability

Madhu Balasubramanian *Serial Link Products*

ABSTRACT

This application report presents phase noise data taken on the CDCE72010 jitter cleaner and synchronizer PLL device from Texas Instruments. The phase noise performance of the CDCE72010 depends on the phase noise of the reference clock, VCXO clock, and the CDCE72010 itself. This application report shows the phase noise performance at several of the most popular CDMA frequencies. This data helps the user to choose the right clocking solution for specific applications. These test results confirm that the CDCE72010 can provide clocks better than –145dBc/Hz phase noise at 1-MHz offset from the carrier frequency. This type of low phase noise is required for wireless applications as well as many other high-performance sampling systems.

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1 Introduction

The CDCE72010 is a low phase noise/low jitter clock synthesizer and jitter cleaner with programmable outputs and inputs. An external low-pass loop filter in addition to an external VCXO or VCO is required to complete the phase-locked loop (PLL). Proper selection of the VCXO and loop bandwidth is critical to achieve the best performance from the CDCE72010.

This report includes phase noise plots of the most common frequencies used in wireless basestation applications. In addition, the phase noise of the clock source that feeds the CDCE72010 is included for completeness. Phase noise measurements of the 30.72-MHz reference, the 491.52-MHz Epson-Toyocom VCXO (TCO-2111), and output phase noise of the CDCE72010 at various frequencies are included. The root-mean-square (RMS) jitter was calculated from the various phase noise plots over the following ranges with the Agilent E5052A phase noise analyzer:

- 1 kHz to 40 MHz for frequencies greater than 100 MHz
- 1 kHz to 20 MHz for frequencies above 40 MHz
- 1 kHz to 5 MHz for frequencies above 10 MHz

In addition, additive phase noise jitter of the CDCE72010 is included in these integrated bandwidths. However, these data do not include jitter contributions from the external clock reference and the VCXO.

1.1 Definitions

Crosstalk— This characteristic is used to measure parasitic coupling between signals, and is the effect of capacitive coupling that causes a logic transition. Capacitive coupling is the transfer of energy between nearby switching integrated circuits. The coupling depends on factors such as the distance between the traces, the signal swing, the operating frequency, and the permissiveness of the silicon dioxide. Coupling can be improved by physically increasing the distance between traces. Power and ground planes also act as shields to minimize crosstalk.

Cycle-to-cycle period jitter—Also known as adjacent cycle jitter; the variation in cycle time of a signal between consecutive cycles over a random sample of successive cycle pairs. Cycle-to-cycle jitter is also a good value to calculate the setup and hold time budgets because it defines the minimum and maximum variations of the timing variation from ideal for the next clock edge.

Jitter— Any edge deviation from the ideal occurrence. The causes of jitter include: power-supply noise, thermal and mechanical noise from the input signal and other external sources, reflection, electromagnetic interference (EMI), and other random noise. Suggestions to reduce jitter include: power-supply bypassing (10 μF to 47 μF) to prevent voltage droop and ripple because of current surges; filtering each VCC pin (with 0.1-μF, low effective series resistance [ESR] capacitor); using proper termination to remove reflections; using differential signaling as opposed to single-ended signaling; and minimizing noise coupling by isolating other high-frequency signals from the clock driver.

Peak-to-peak period jitter—The total jitter range from minimum to maximum values of a clock signal. Peak-to-peak jitter increases indefinitely with recording time. Thus, peak-to-peak jitter values are only meaningful if either the recording length or the relative bit error rate is known.

Period jitter—The deviation in cycle time of a signal with respect to an ideal period over a random sample of cycles. Period jitter is important because it includes the maximum and minimum frequencies, and it specifies the shortest clock period. It is important for the setup and hold time budgets. Calculations with period jitter are sufficient for subsystems that use clock and data signals derived from the same clock source. Period jitter can be measured with any oscilloscope.

Phase jitter— Phase jitter, or accumulated jitter, is the absolute deviation of a clock edge from its ideal position in timing. While period jitter only accounts for the variation between clock periods, phase jitter accumulates the error of each period and is therefore always larger. The wider the recording time window, the more frequency bandwidth becomes integrated into the total phase jitter. Phase jitter can also be measured by integrating phase noise over the frequency band of interest. Either way, the system designer must specify the minimum and maximum frequency for the integration.

For setup and hold time budget calculations, the peak-to-peak (PP) value of the phase jitter is important. Note that only the added phase noise by the clock driver is of interest to find the worst edge position between the master clock in the system and the subsystem. The absolute phase jitter of the master clock itself adds to all clock signals in the system, thus canceling its effect.

Phase noise—The short-term instability caused by frequency variation (phase) of a signal referenced to the carrier level and a function of the carrier offset (that is, relative noise level within a 1-Hz bandwidth). Integration of PN over a given frequency band yields phase jitter RMS.

RMS period jitter—One standard deviation (1 σ) of the peak-to-peak jitter of a clock signal. RMS jitter is only valid for Gaussian (that is, normal) distribution. RMS jitter is independent of the sampling window, and therefore more suitable for comparing the performance of two or more devices where the sampling time window differs or is unknown.

Timing budget—Defined by dynamic (jitter) and static errors (skew). Depending on the system architecture, only a subset of parameters from the datasheet affect the timing budget. Jitter is a timing distribution of the clock signal that expresses the edge deviation from the ideal occurrence. Jitter is composed of both deterministic and random (Gaussian) content.

2 Test Equipment and Setup

All measurements discussed in this application report were taken under nominal conditions: a 3.3-V power supply, at room temperature, and in a PLL lock condition except for additive jitter, which was performed for a VCXO held at a control voltage of 1.65 V. The CDCE72010EVM evaluation module is used with a 491.52-MHz Epson-Toyocom (TCO-2111) VCXO. Figure 3 shows the CDCE72010 device configuration. The power supply is provided by the HP6624A; a reference input of 30.72 MHz LVCMOS is provided by an HP8133. Phase noise is measured using the Agilent E5052A. Figure 2 shows the test setup that was used for all phase noise testing. Output dividers were set to /1, /2, /3, /4, and /5 for overall and additive phase noise measurements. An output divider of /4 was used for jitter cleaner tests where the 30.72 MHz LVCMOS input was fed into a NoiseCom noise generator box to increase the noise floor, thus raising the input jitter. The RMS jitter was calculated from the phase noise plots over a 1 kHz to 40 MHz range for frequencies greater than 100 MHz, from 1 kHz to 20 MHz for frequencies above 40 MHz, and from 1 kHz to 5 MHz for frequencies above 10 MHz. A 60-Hz loop filter bandwidth is used; Figure 1 illustrates the filter topology for this loop filter. All HS-LVPECL, LVCMOS, and HS-LVDS outputs were properly terminated and tested for jitter.

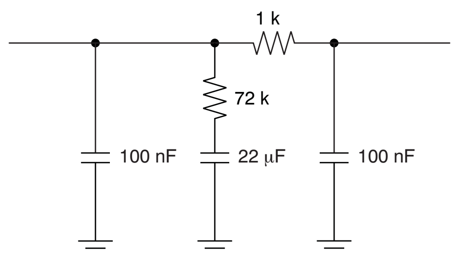

Figure 1. Passive Loop Filter Circuit

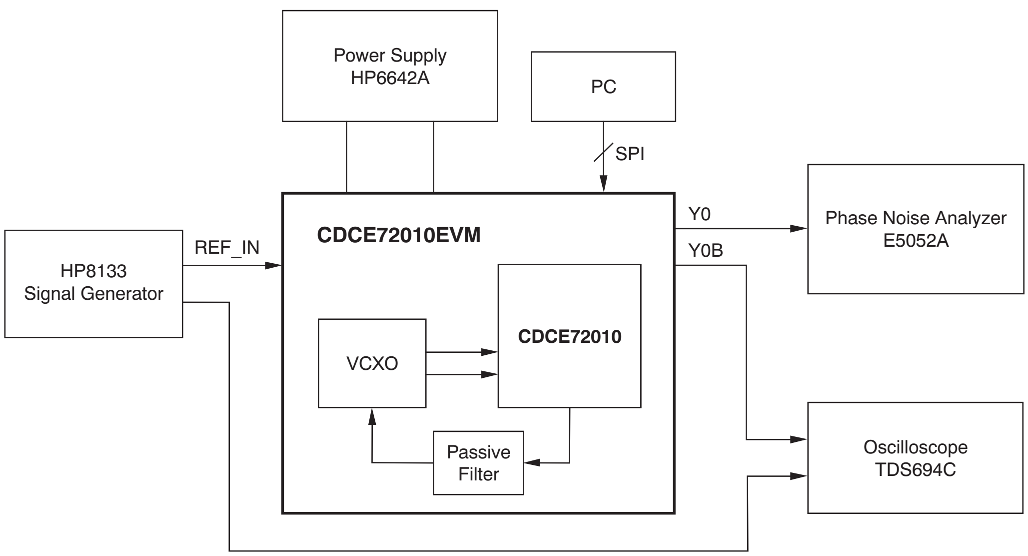

Figure 2. Phase Noise Measurement Test Setup

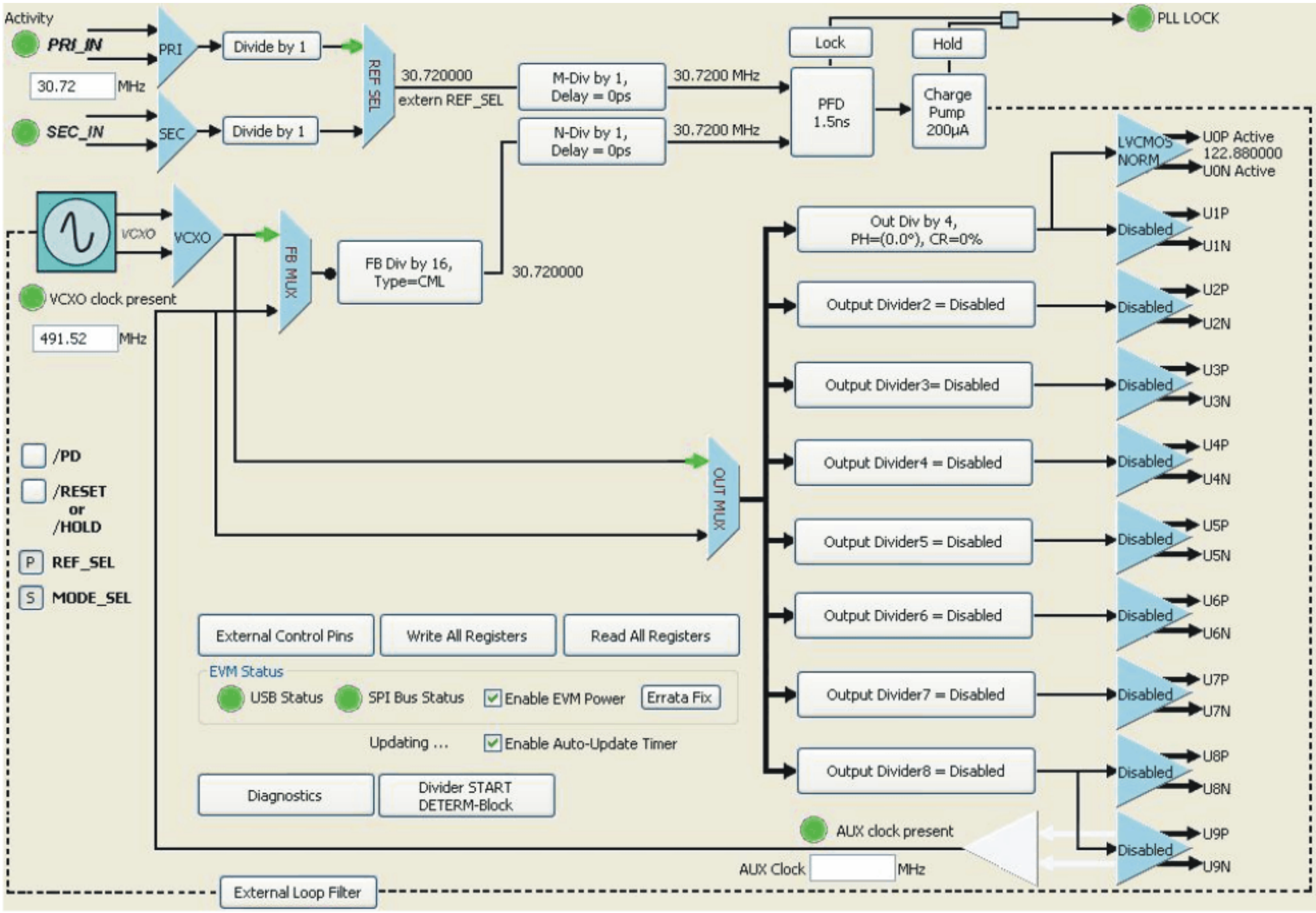

Figure 3. CDCE72010 Device Configuration

3 Total Phase Noise Measurements

Section 3.1 summarizes the total phase noise/jitter measurements made on the CDCE72010 with a 491.52-MHz VCXO and for /1, /2, /3, /4, and /5 output divider configurations for HS-LVDS, HS-LVPECL and LVCMOS output types. Section 3.2 shows the measurement results at different output frequencies and for different output types.

3.1 Performance Summary

Table 1 lists the total jitter of the CDCE72010 with a 491.52-MHz VCXO.

Table 1. CDCE72010 and 491.52-MHz VCXO Total Jitter Summary

Frequency (MHz)	Output Type	Phase Jitter (fs, RMS) 1 kHz to 40 MHz
491.52	HS-LVPECL	154.35
491.52	HS-LVDS	162.44
245.76	LVCMOS	243.67
245.76	HS-LVPECL	199.11
245.76	HS-LVDS	216.09
163.84	LVCMOS	246.74
163.84	HS-LVPECL	215.02
163.84	HS-LVDS	268.57
122.88	LVCMOS	281.05
122.88	HS-LVPECL	234.97
122.88	HS-LVDS	321.86
98.304	LVCMOS	228.91 (1 kHz to 20 MHz)
98.304	HS-LVPECL	192.14 (1 kHz to 20 MHz)
98.304	HS-LVDS	286.08 (1 kHz to 20 MHz)

3.2 Measurement Results

Figure 4 through Figure 17 show the measured results for output phase noise over a range of frequencies.

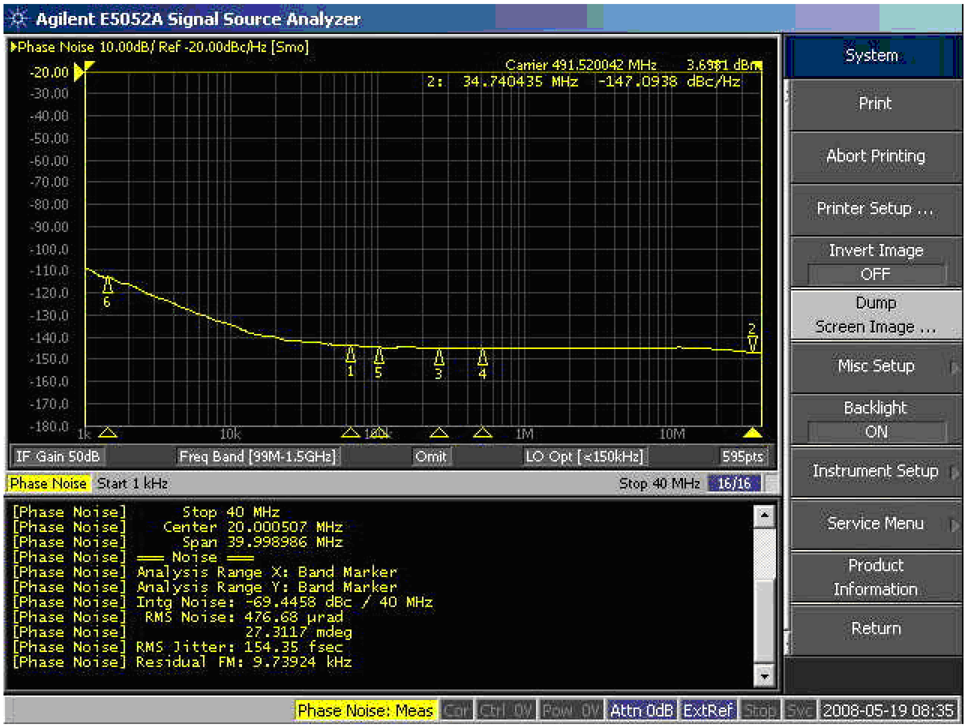

Figure 4. 491.52-MHz HS-LVPECL Output Phase Noise

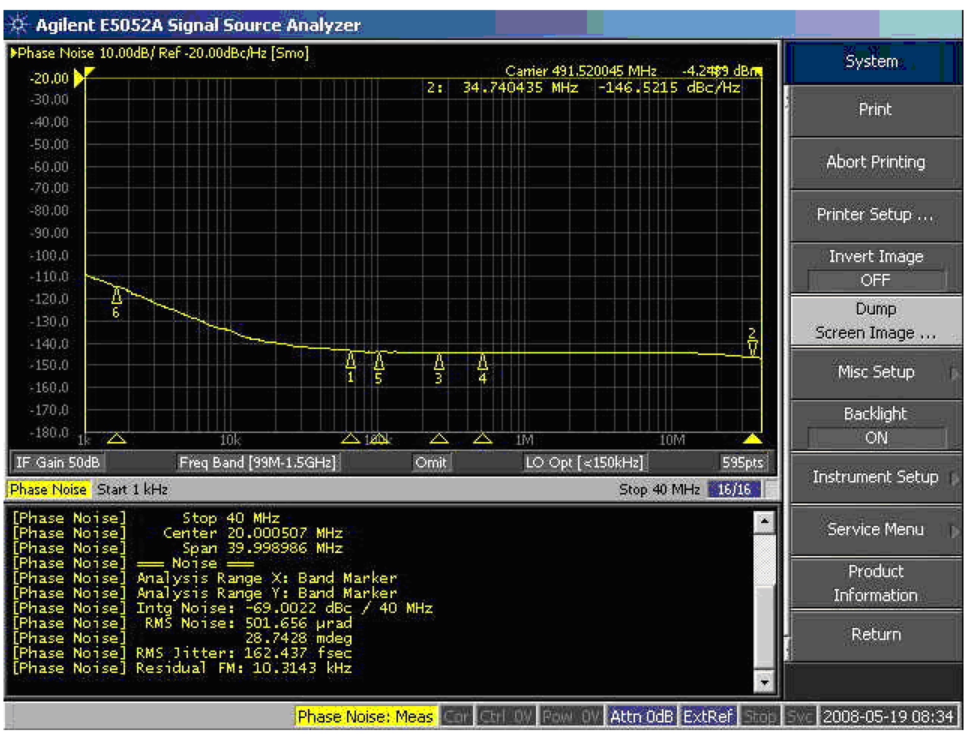

Figure 5. 491.52-MHz HS-LVDS Output Phase Noise

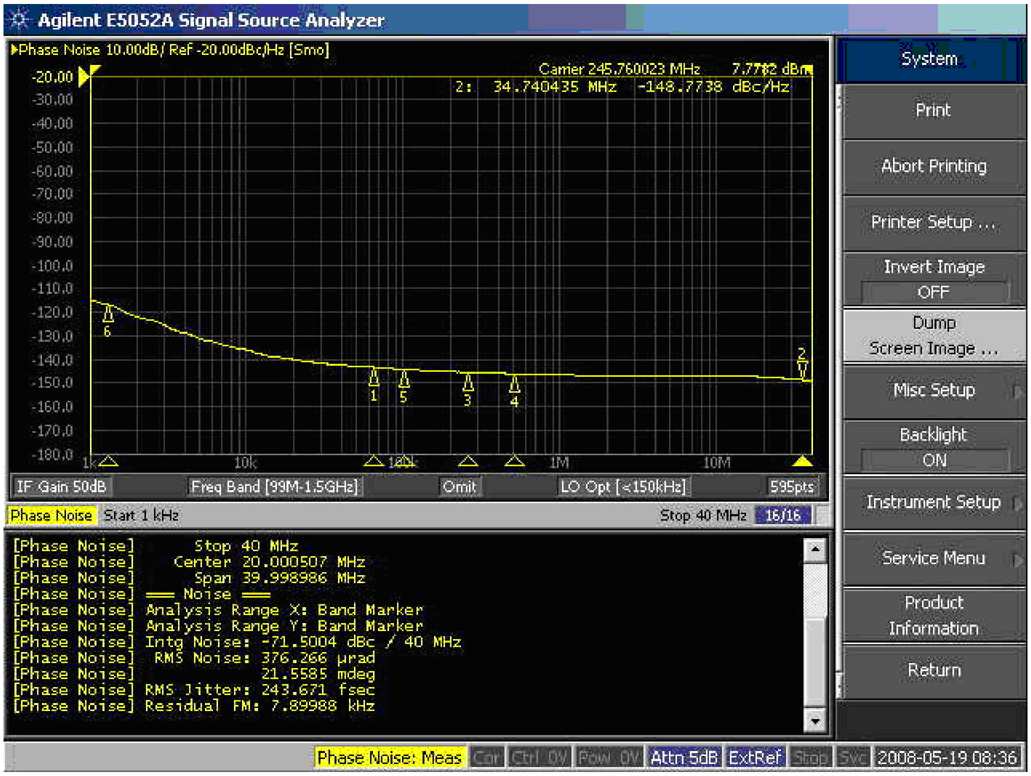

Figure 6. 245.76-MHz LVCMOS Output Phase Noise

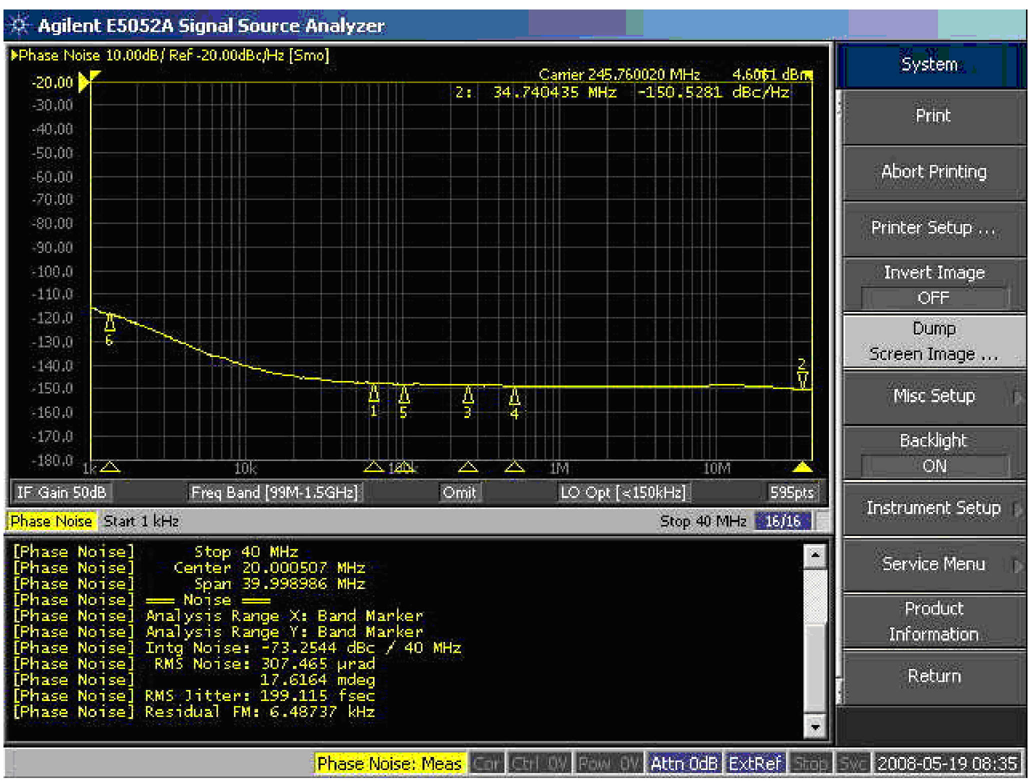

Figure 7. 245.76-MHz HS-LVPECL Output Phase Noise

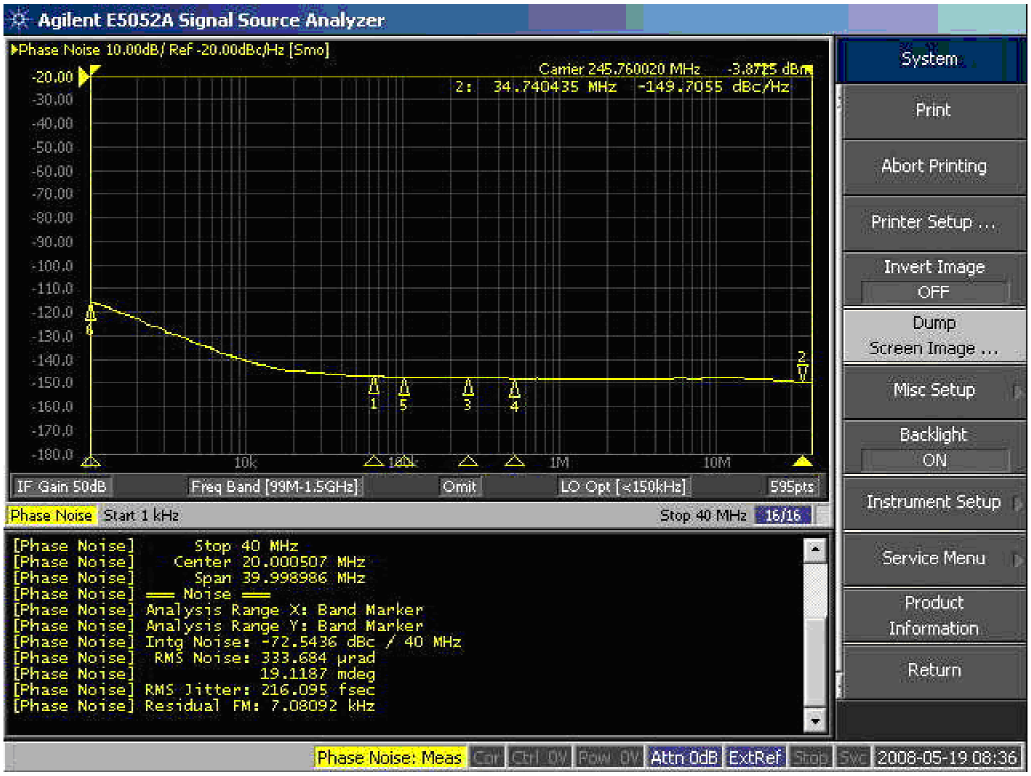

Figure 8. 245.76-MHz HS-LVDS Output Phase Noise

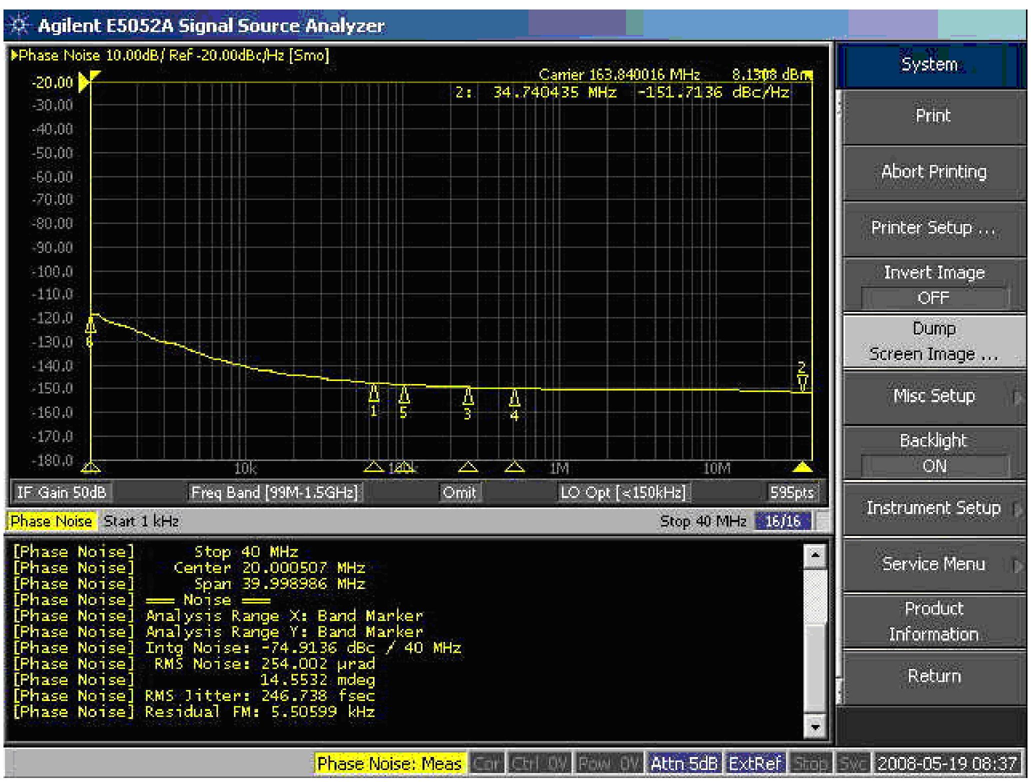

Figure 9. 163.84-MHz LVCMOS Output Phase Noise

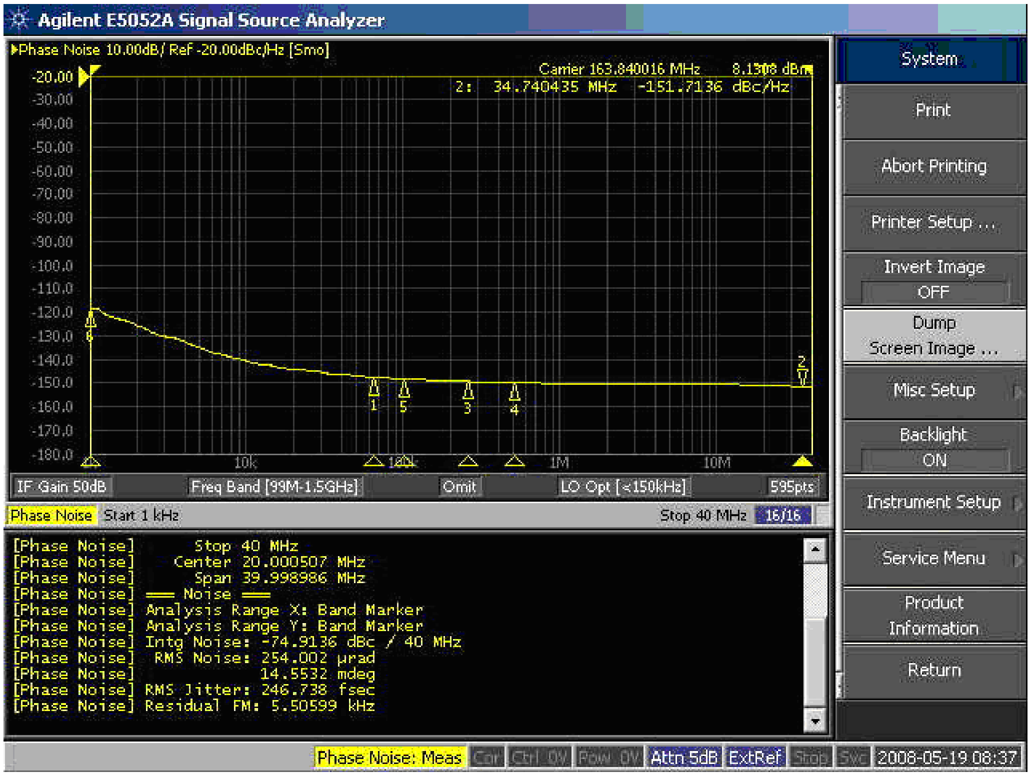

Figure 10. 163.84-MHz HS-LVPECL Output Phase Noise

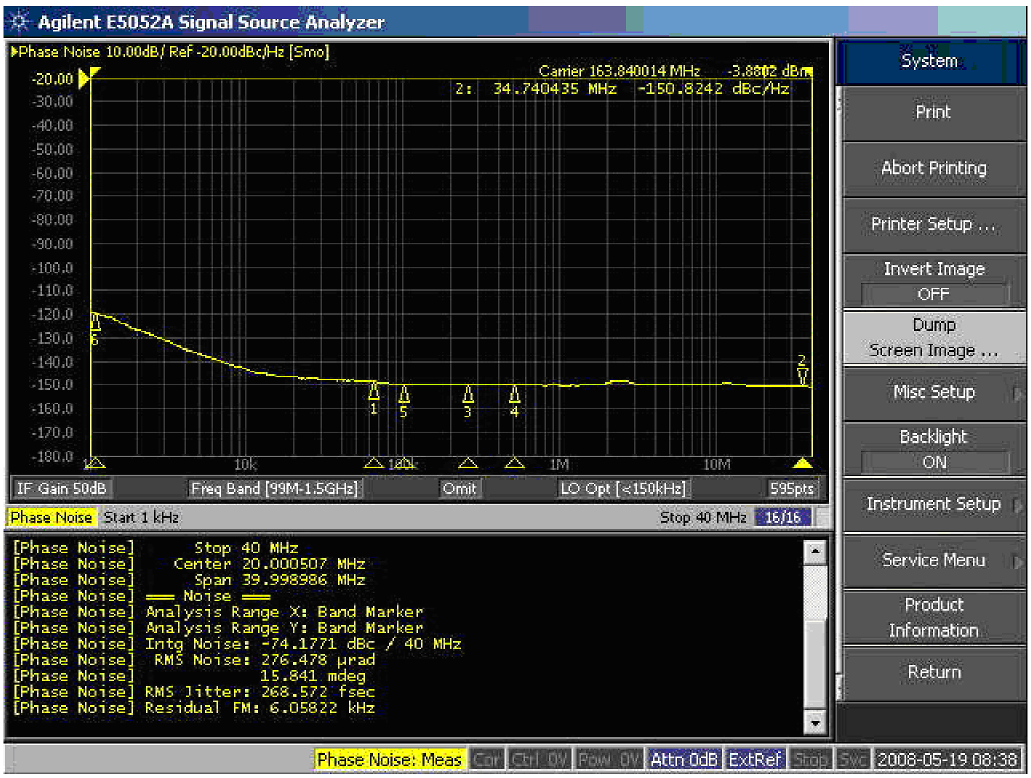

Figure 11. 163.84-MHz HS-LVDS Output Phase Noise

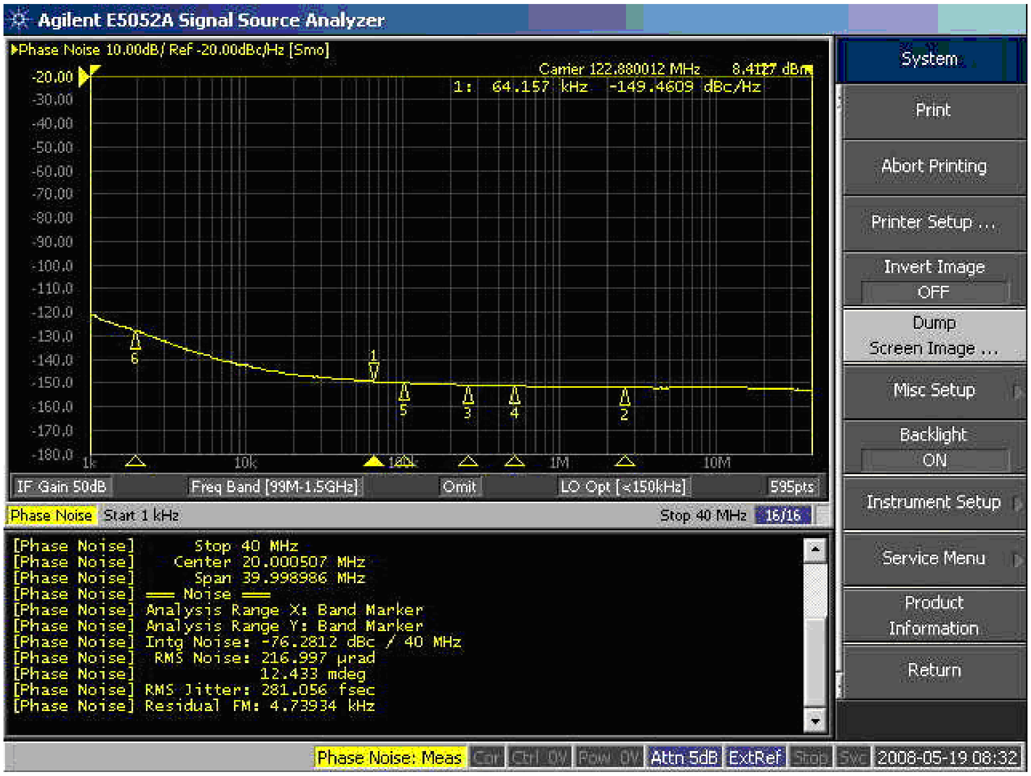

Figure 12. 122.88-MHz LVCMOS Output Phase Noise

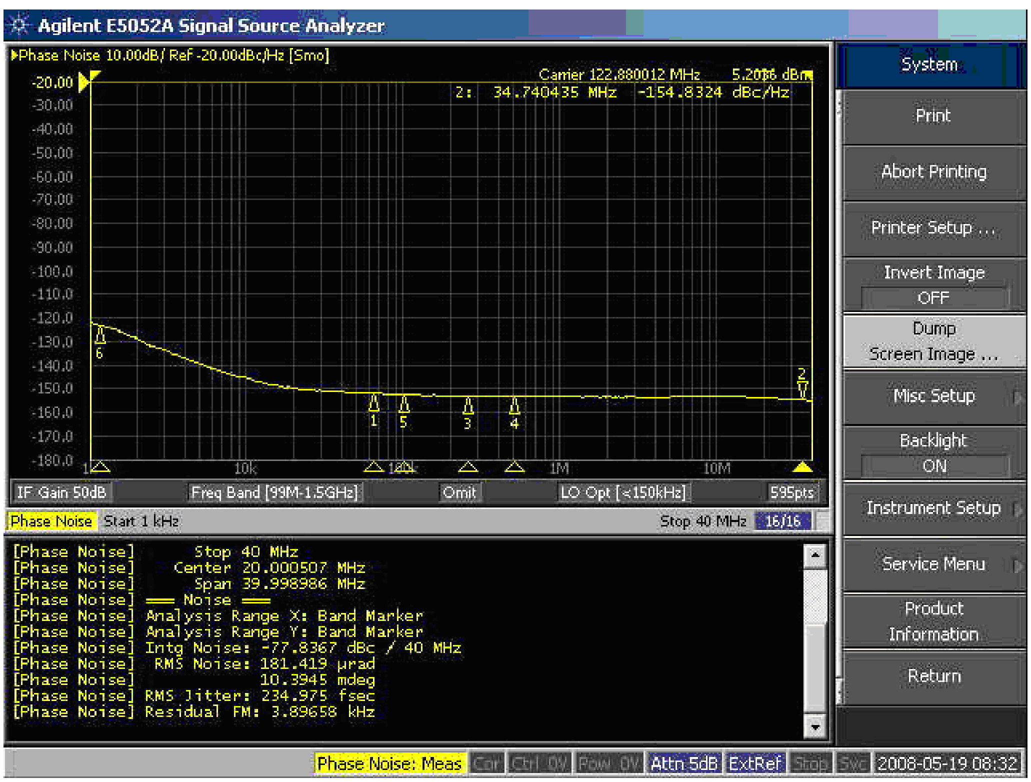

Figure 13. 122.88-MHz HS-LVPECL Output Phase Noise

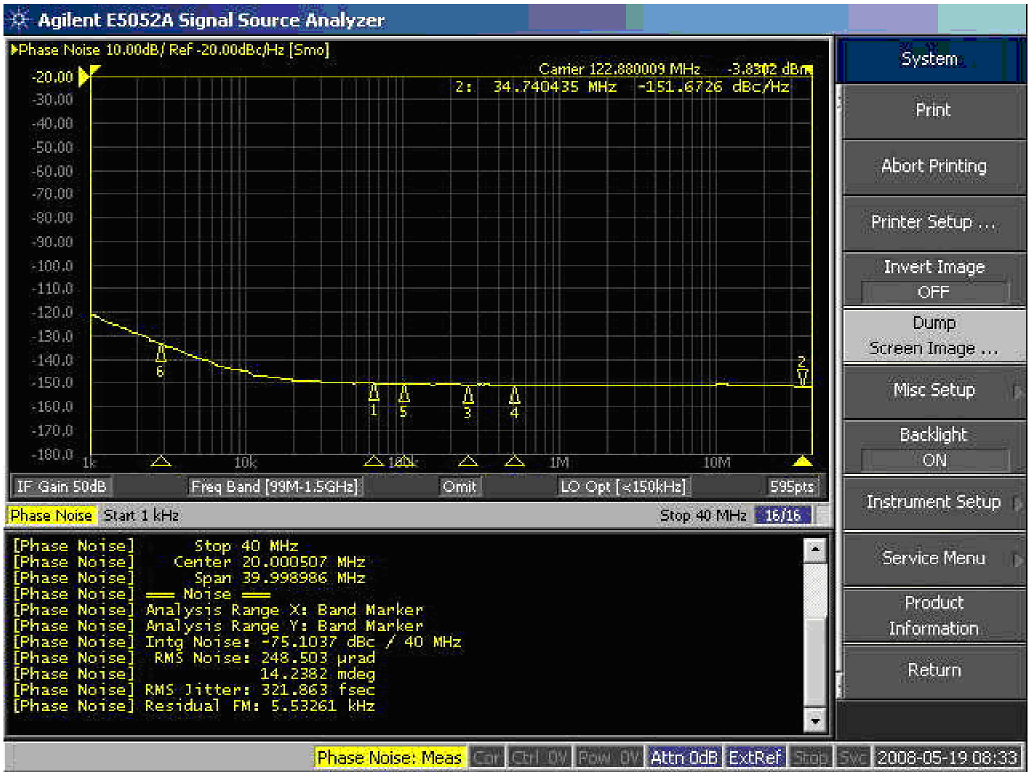

Figure 14. 122.88-MHz HS-LVDS Output Phase Noise

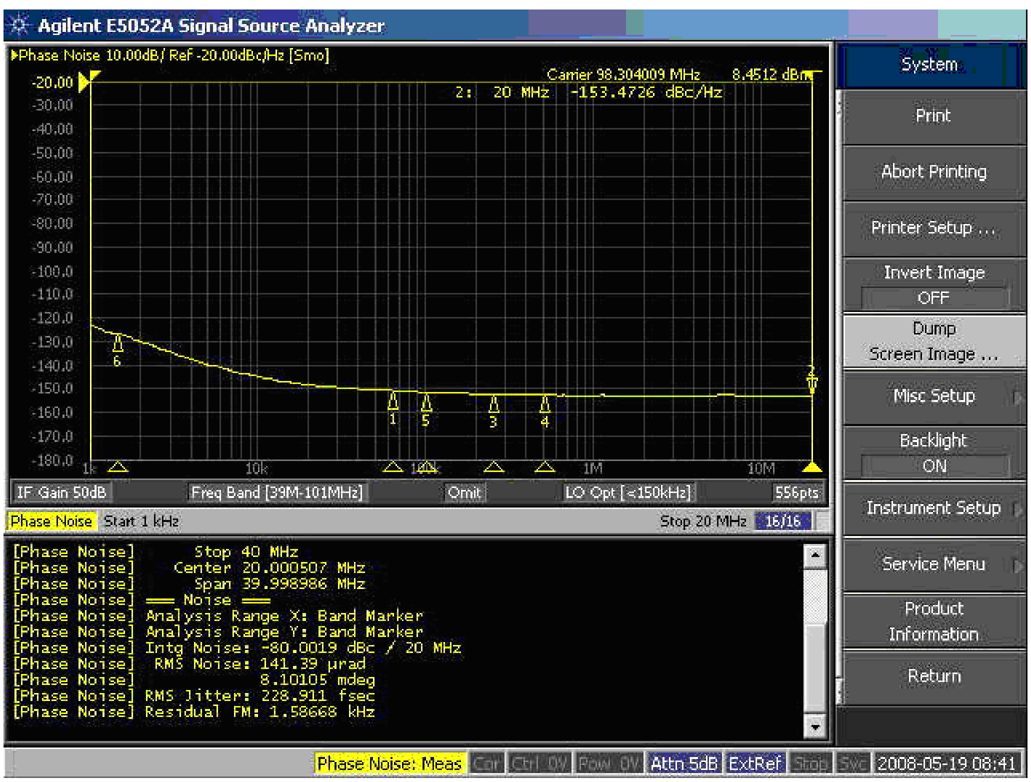

Figure 15. 98.304-MHz LVCMOS Output Phase Noise

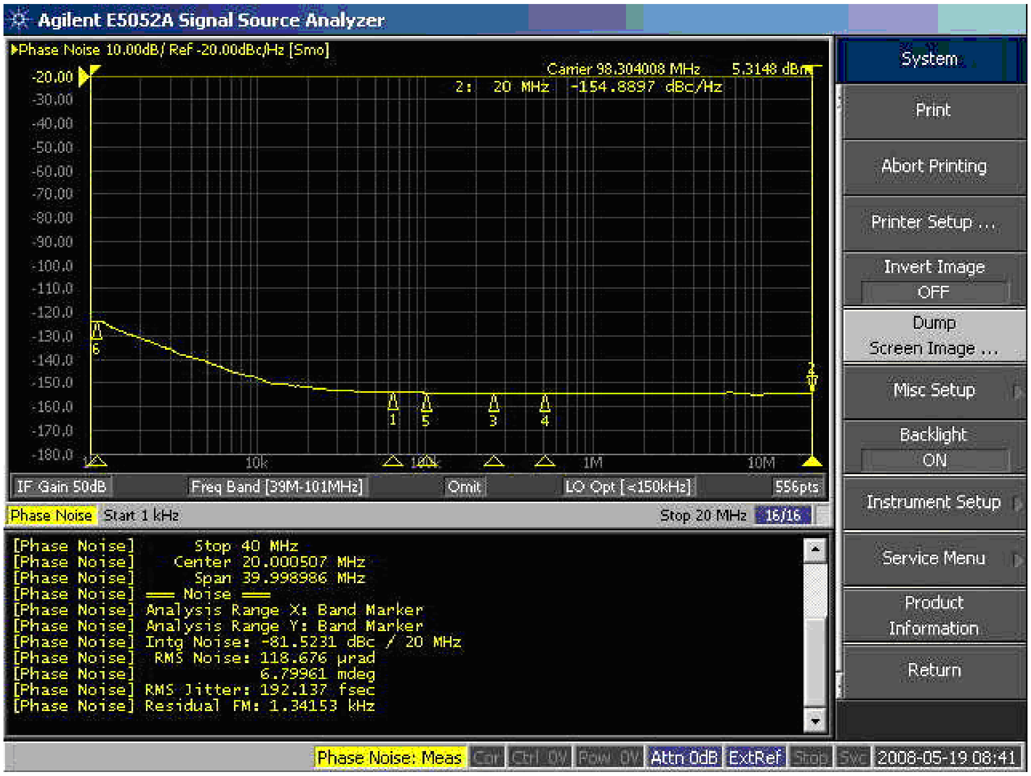

Figure 16. 98.304-MHz HS-LVPECL Output Phase Noise

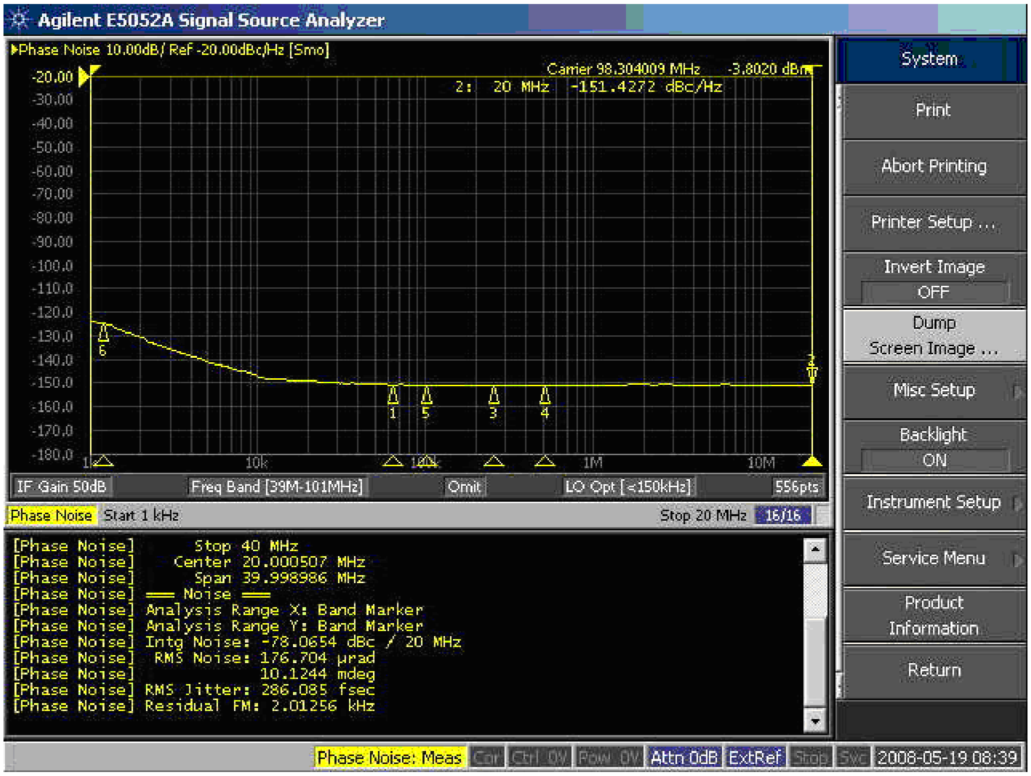

Figure 17. 98.304-MHz HS-LVDS Output Phase Noise

4 Total Phase Noise Measurements

Section 4.1 shows a summary of the CDCE72010 jitter cleaning ability with a 491.52-MHz VCXO and output divider of /4, for different output types. The input is a 30.72-MHz LVCMOS with varying phase jitter characteristics. Section 4.2 shows the measurement results.

4.1 Performance Measurement Summary

Table 2 describes the CDCE72010 jitter cleaning ability for a range of output types.

Table 2. CDCE72010 Jitter Cleaning Ability Summary

In-Phase Jitter (ps, RMS) 1 kHz to 5 MHz	Output Type	Out Phase Jitter (fs, RMS) 1 kHz to 40 MHz
1	LVCMOS	275.63
1	HS-LVPECL	225.98
1	HS-LVDS	314.26
5	LVCMOS	274.84
5	HS-LVPECL	227.99
5	HS-LVDS	314.08
10	LVCMOS	275.82
10	HS-LVPECL	226.39
10	HS-LVDS	315.18
25	LVCMOS	279.79
25	HS-LVPECL	233.76
25	HS-LVDS	318.49
50	LVCMOS	290.41
50	HS-LVPECL	238.39
50	HS-LVDS	319.32

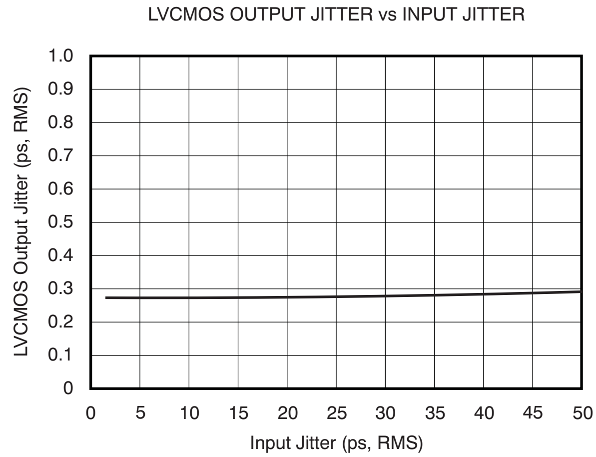

Figure 18. 122.88-MHz LVCMOS Output Jitter Cleaning Ability

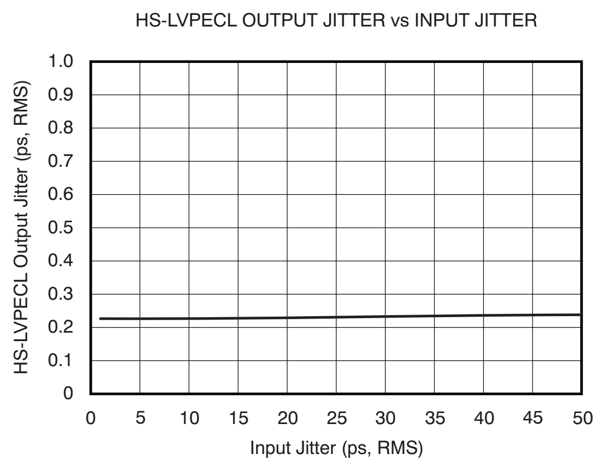

Figure 19. 122.88-MHz HS-LVPECL Output Jitter Cleaning Ability

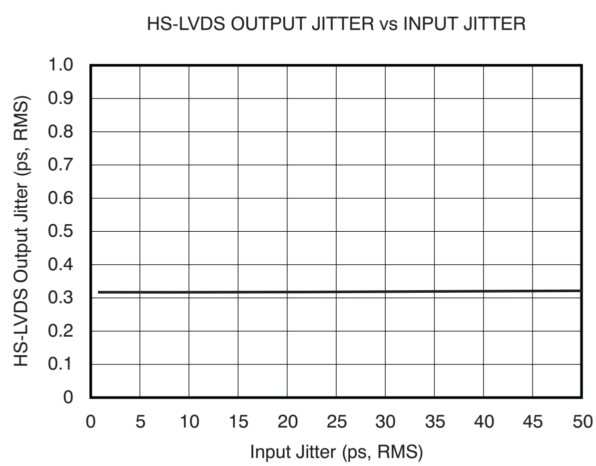

Figure 20. 122.88-MHz HS-LVDS Output Jitter Cleaning Ability

4.2 Measurement Results

Figure 21 through Figure 40 show the measured results for output phase noise over a range of frequencies.

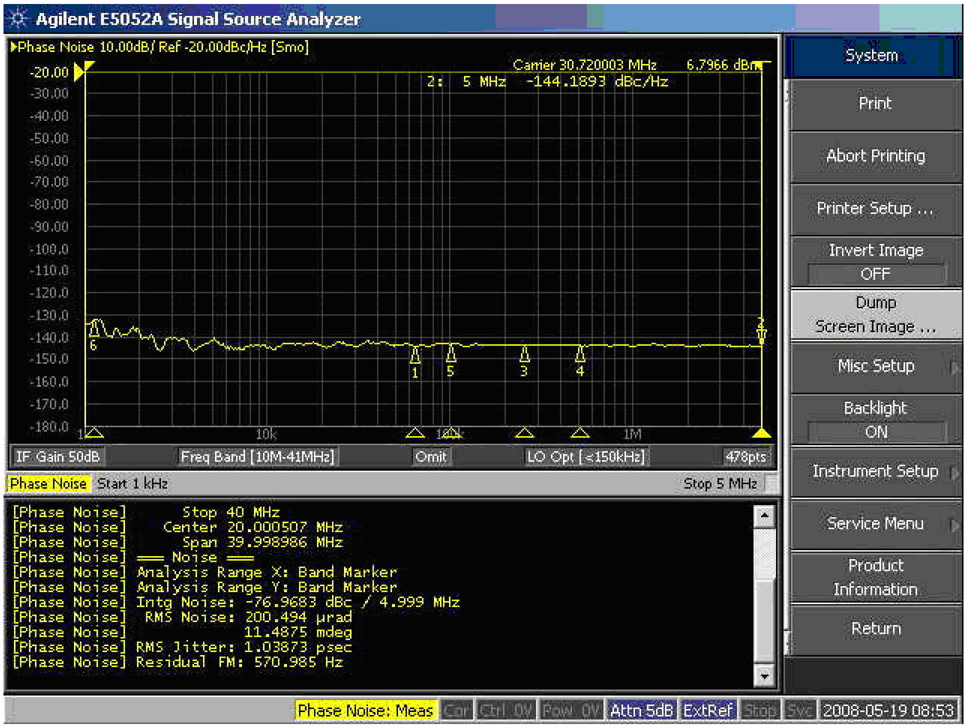

Figure 21. 30.72-MHz LVCMOS Input Phase Noise Profile (1 ps, RMS)

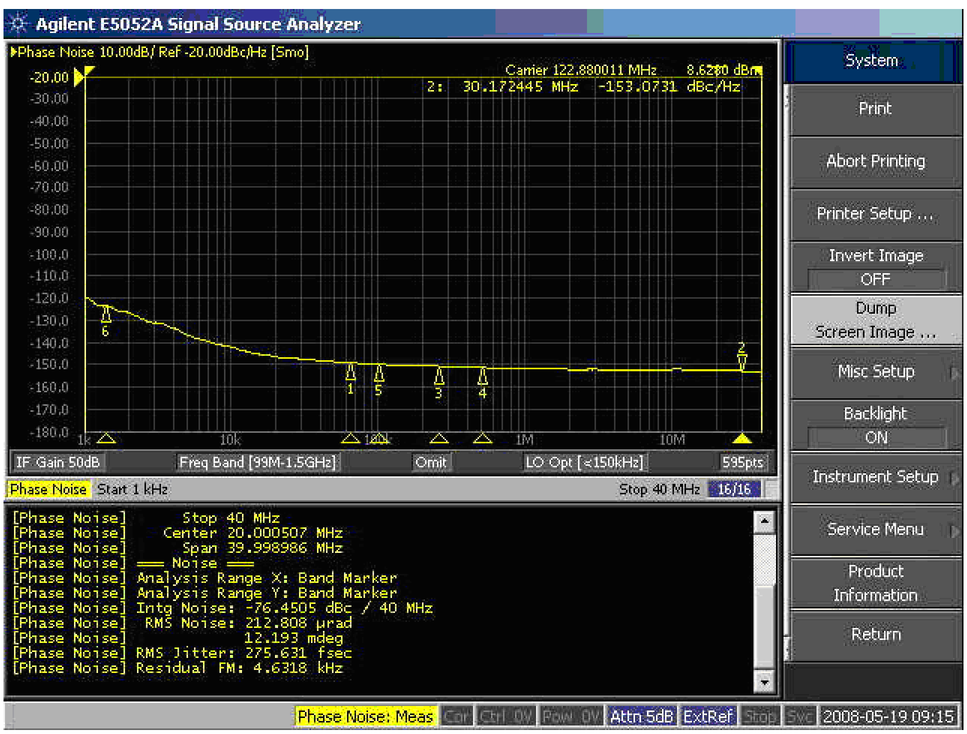

Figure 22. 122.88-MHz LVCMOS Output Phase Noise Profile (1 ps, RMS Input)

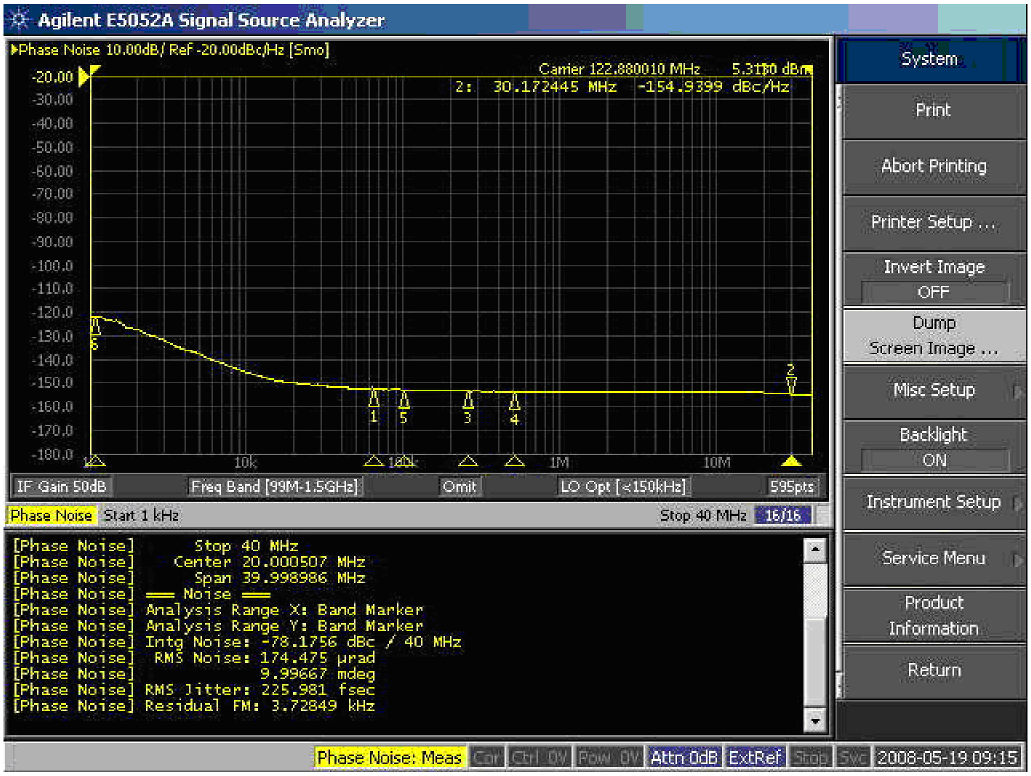

Figure 23. 122.88-MHz HS-LVPECL Output Phase Noise Profile (1 ps, RMS Input)

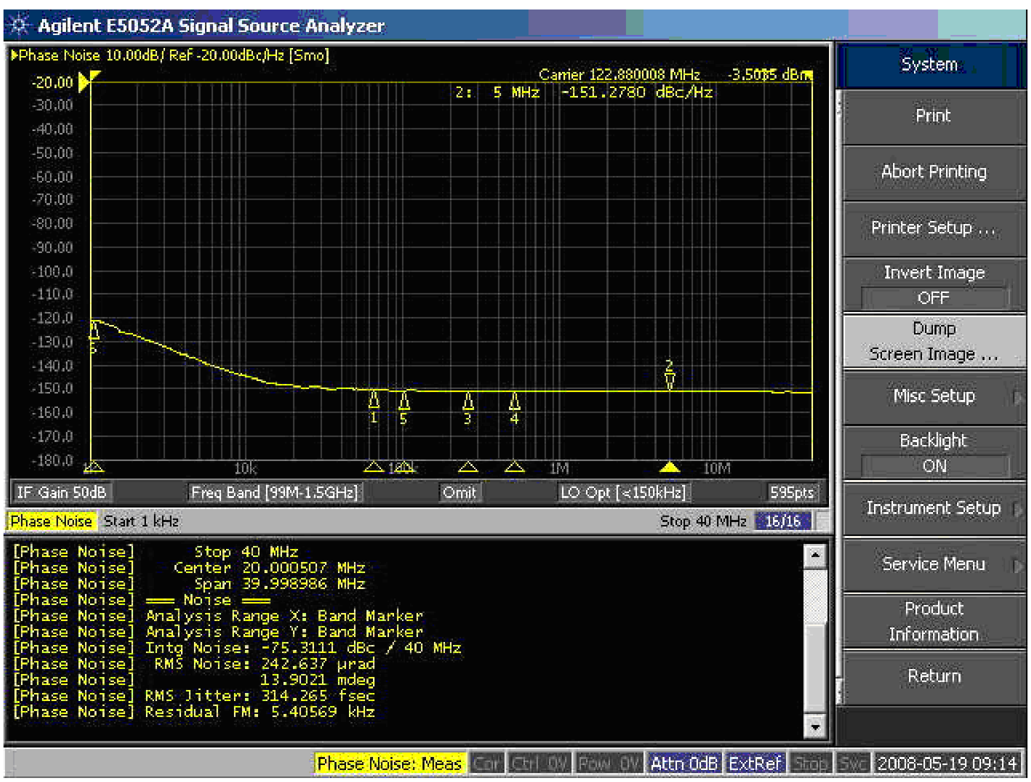

Figure 24. 122.88-MHz HS-LVDS Output Phase Noise Profile (1 ps, RMS Input)

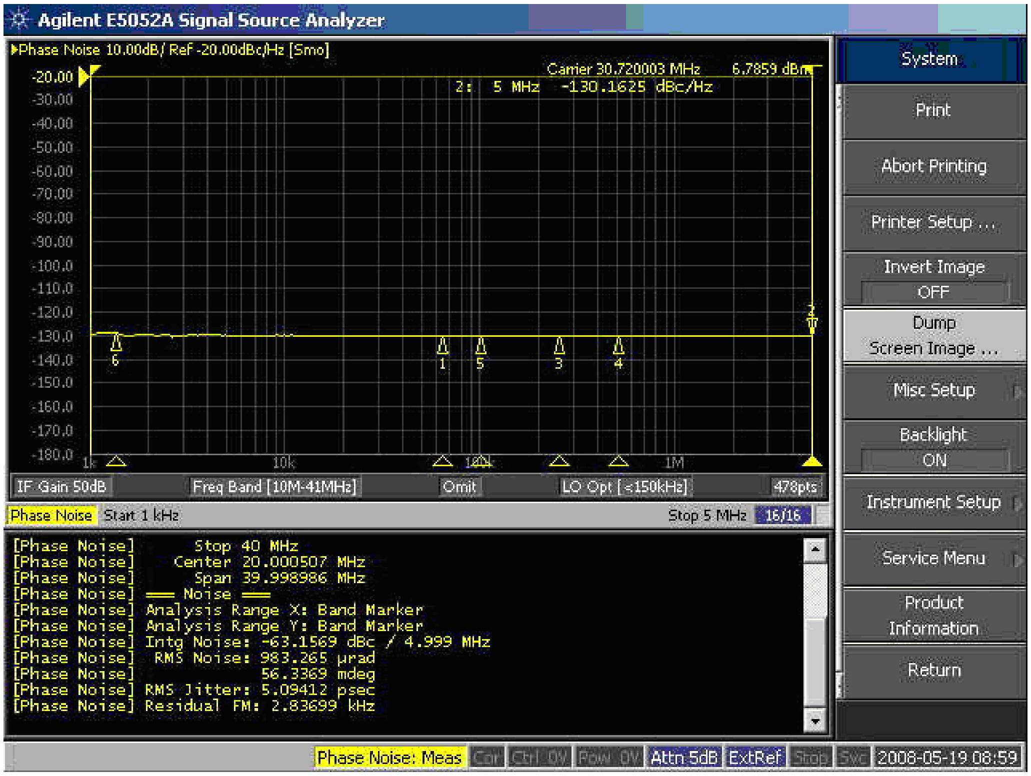

Figure 25. 30.72-MHz LVCMOS Input Phase Noise Profile (5 ps, RMS)

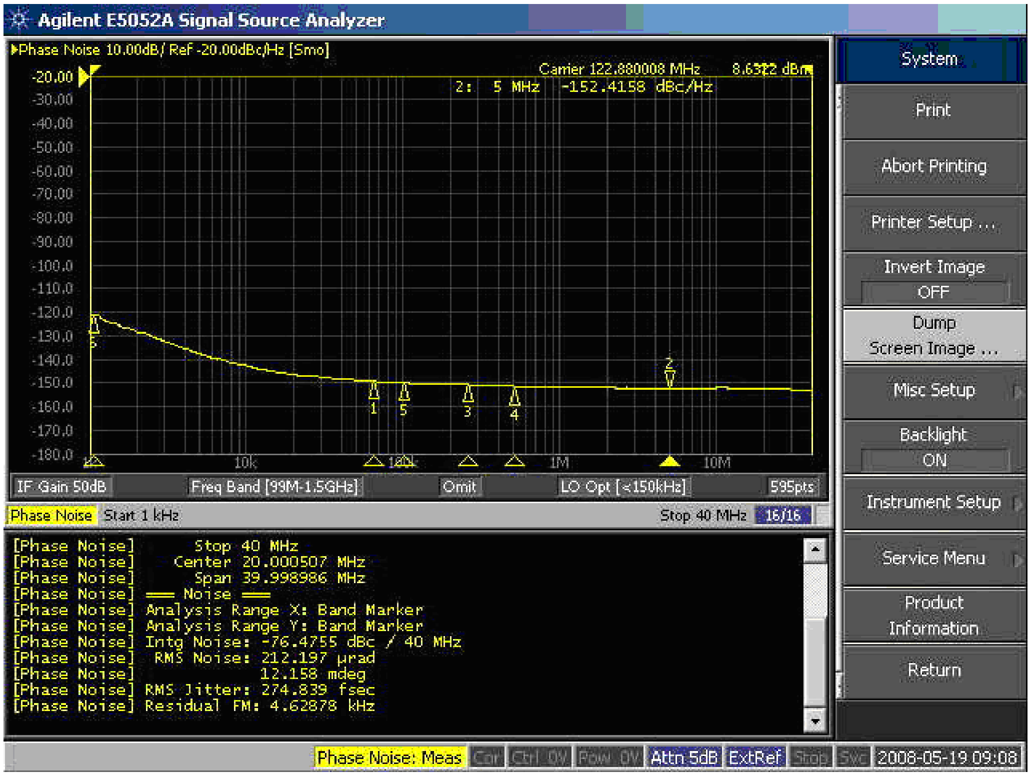

Figure 26. 122.88-MHz LVCMOS Output Phase Noise Profile (5 ps, RMS Input)

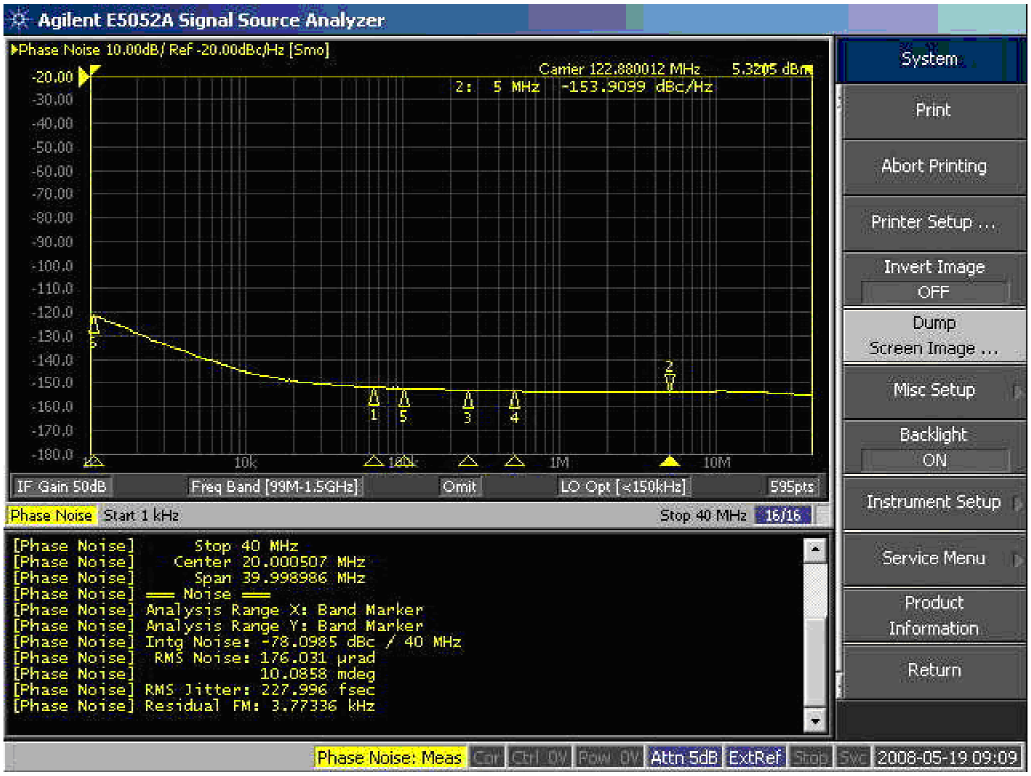

Figure 27. 122.88-MHz HS-LVPECL Output Phase Noise Profile (5 ps, RMS Input)

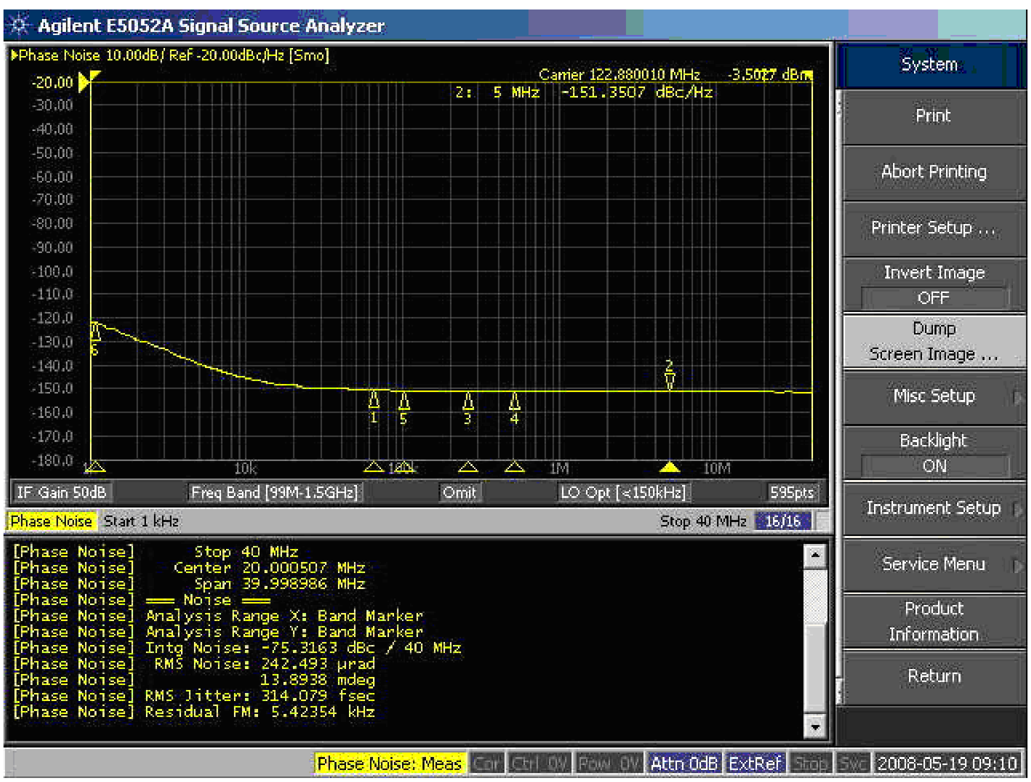

Figure 28. 122.88-MHz HS-LVDS Output Phase Noise Profile (5 ps, RMS Input)

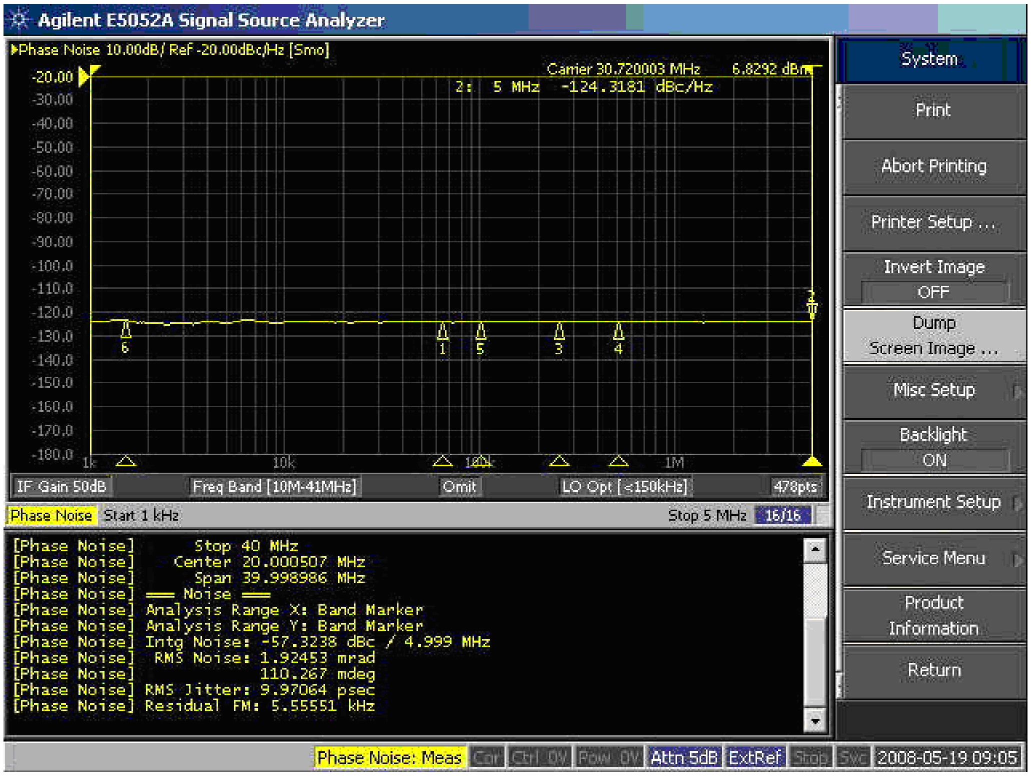

Figure 29. 30.72-MHz LVCMOS Input Phase Noise Profile (10 ps, RMS)

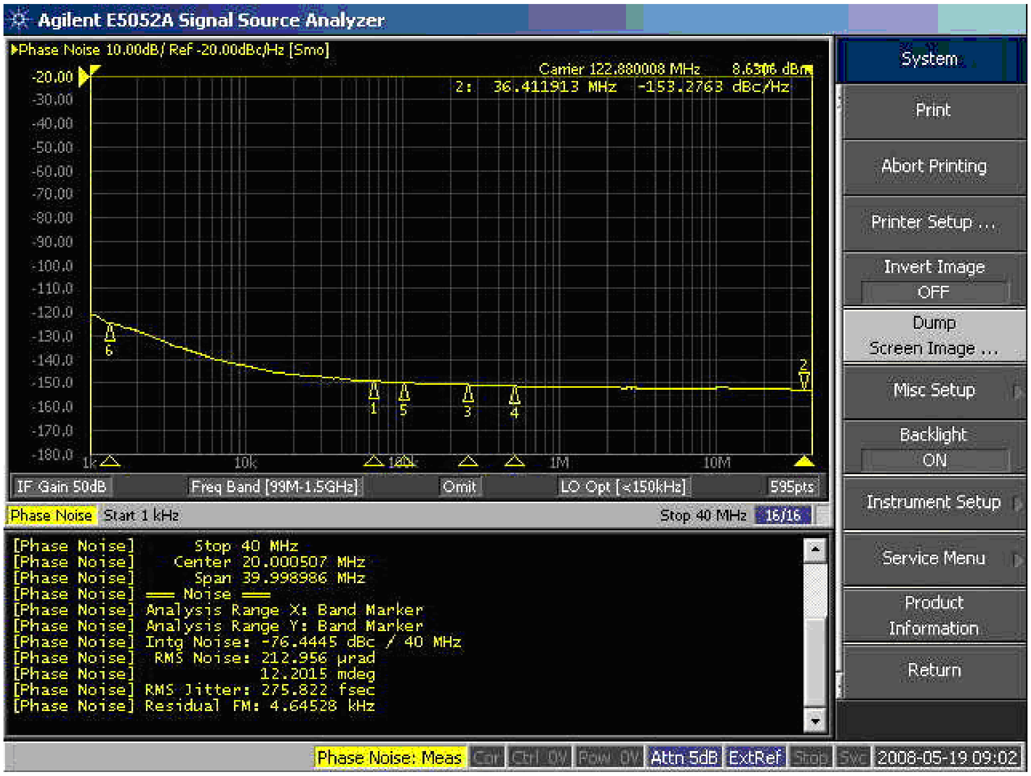

Figure 30. 122.88-MHz LVCMOS Output Phase Noise Profile (10 ps, RMS Input)

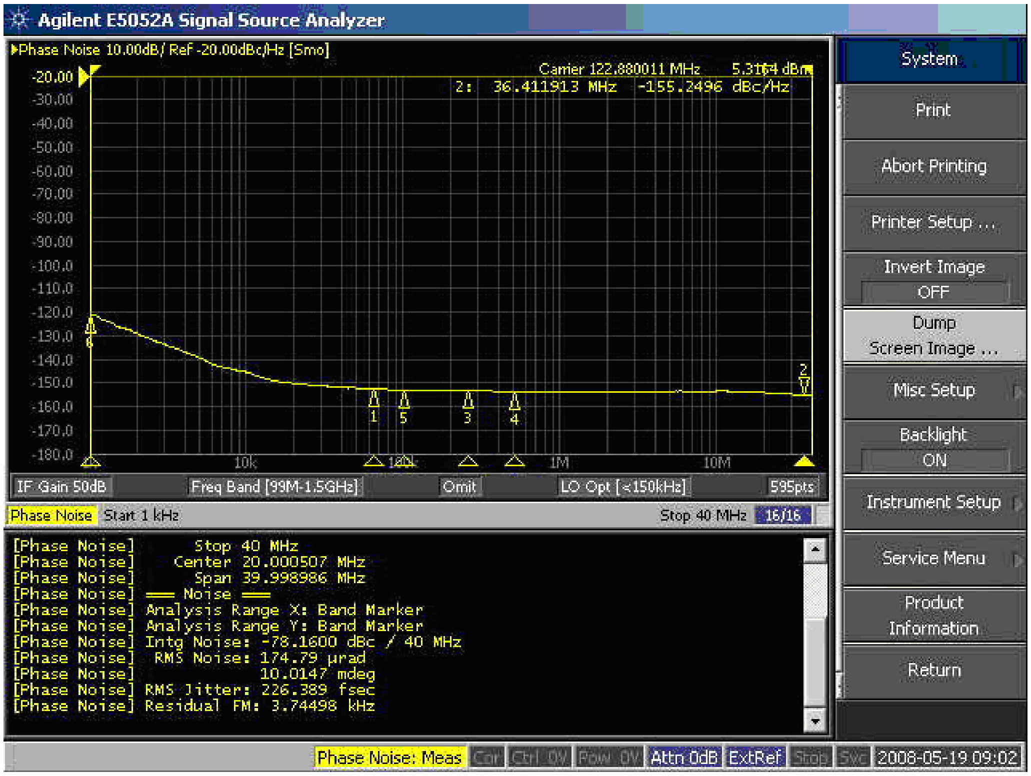

Figure 31. 122.88-MHz HS-LVPECL Output Phase Noise Profile (10 ps, RMS Input)

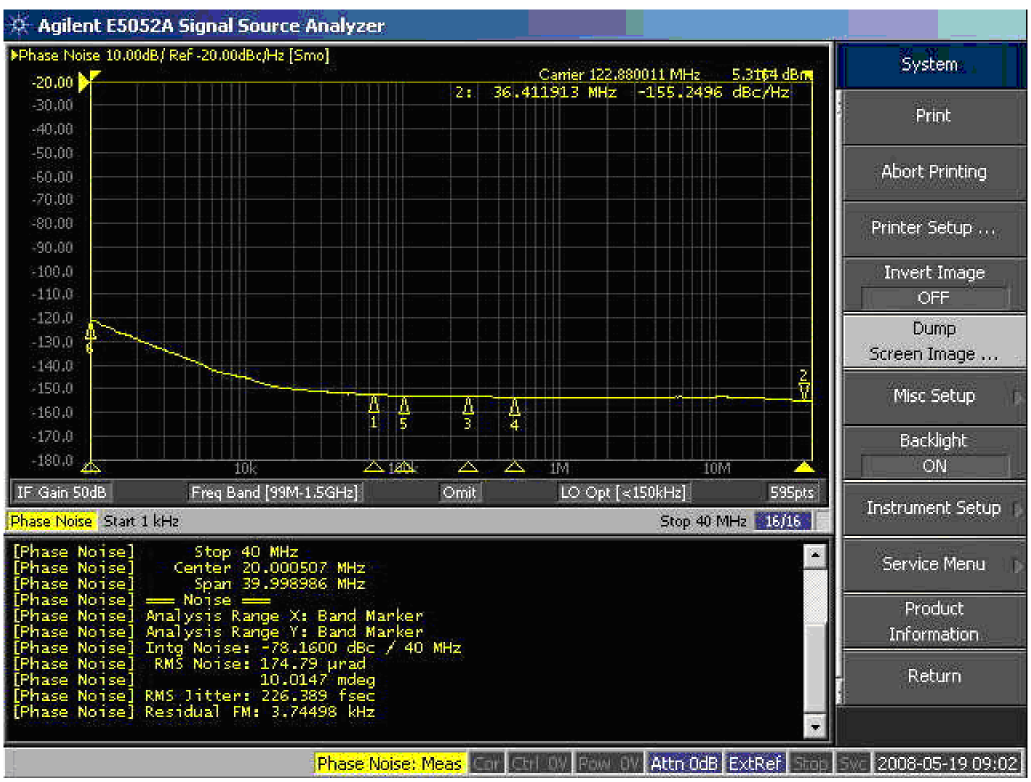

Figure 32. 122.88-MHz HS-LVDS Output Phase Noise Profile (10 ps, RMS Input)

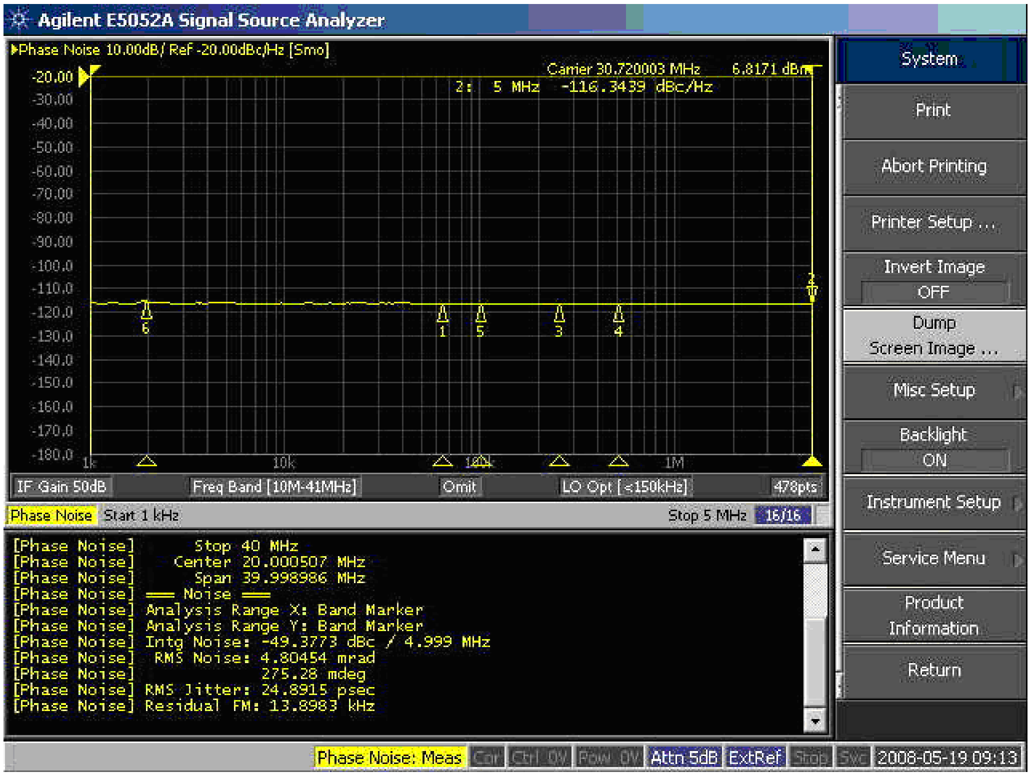

Figure 33. 30.72-MHz LVCMOS Input Phase Noise Profile (25 ps, RMS)

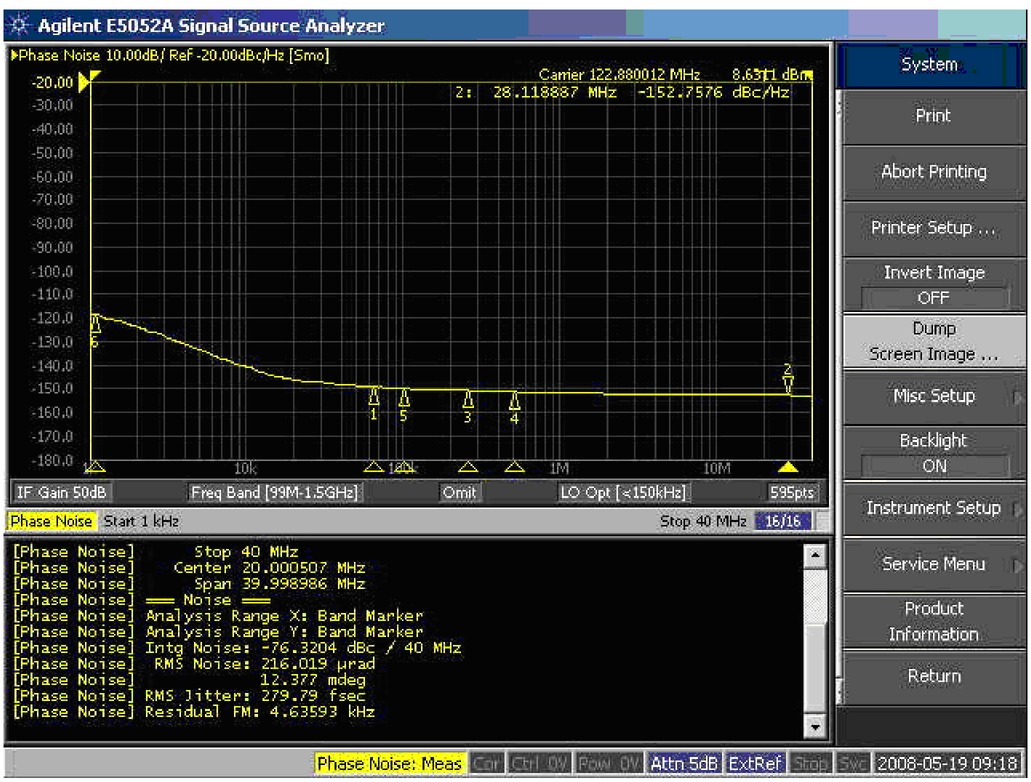

Figure 34. 122.88-MHz LVCMOS Output Phase Noise Profile (25 ps, RMS Input)

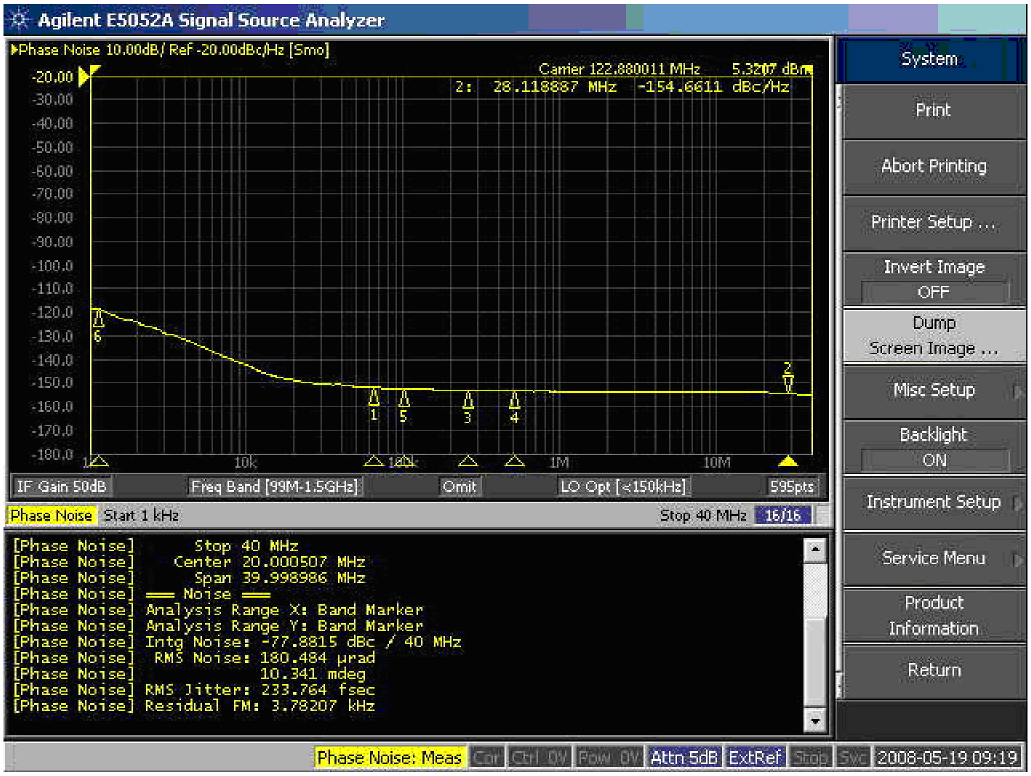

Figure 35. 122.88-MHz HS-LVPECL Output Phase Noise Profile (25 ps, RMS Input)

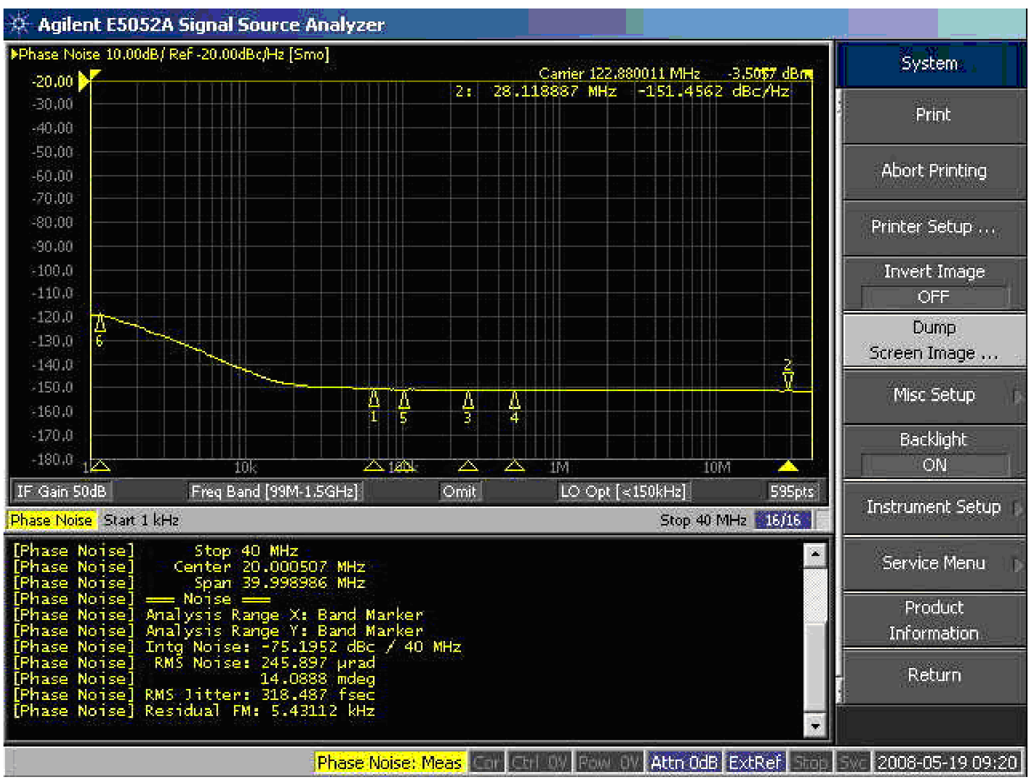

Figure 36. 122.88-MHz HS-LVDS Output Phase Noise Profile (25 ps, RMS Input)

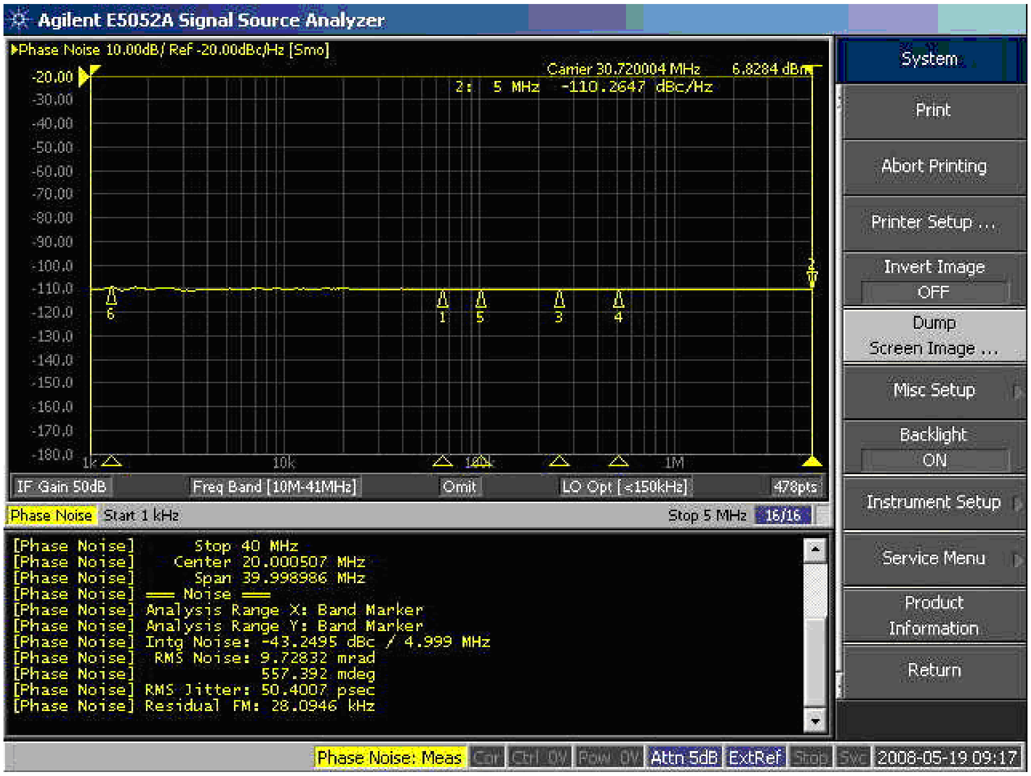

Figure 37. 30.72-MHz LVCMOS Input Phase Noise Profile (50 ps, RMS)

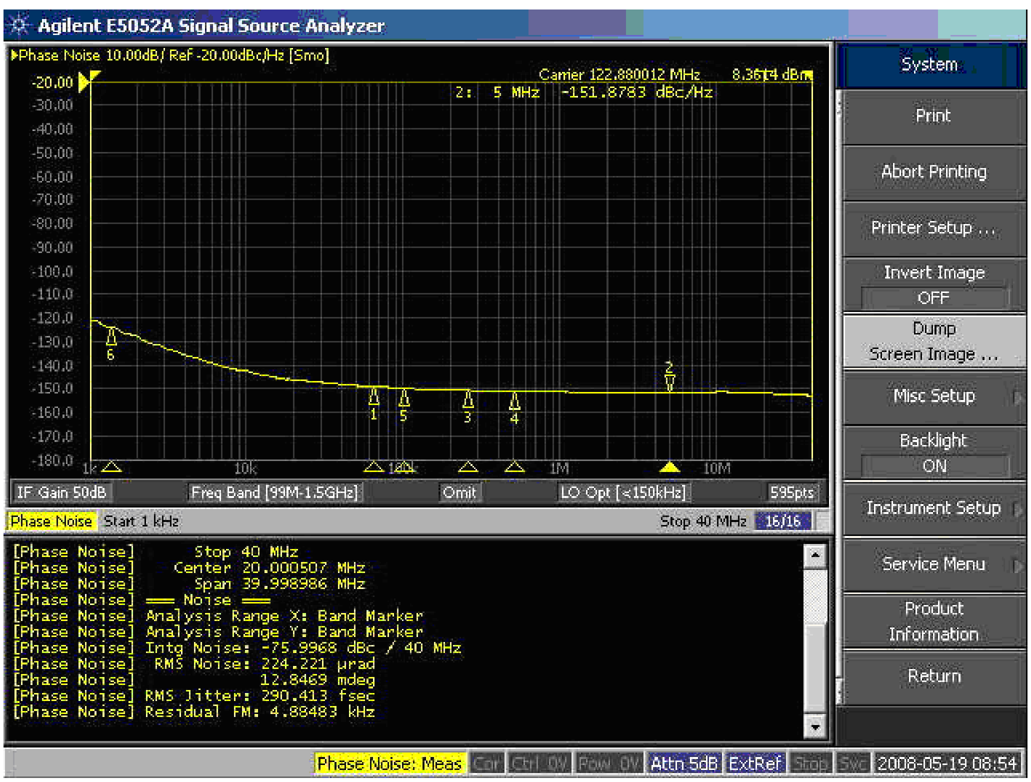

Figure 38. 122.88-MHz LVCMOS Output Phase Noise Profile (50 ps, RMS Input)

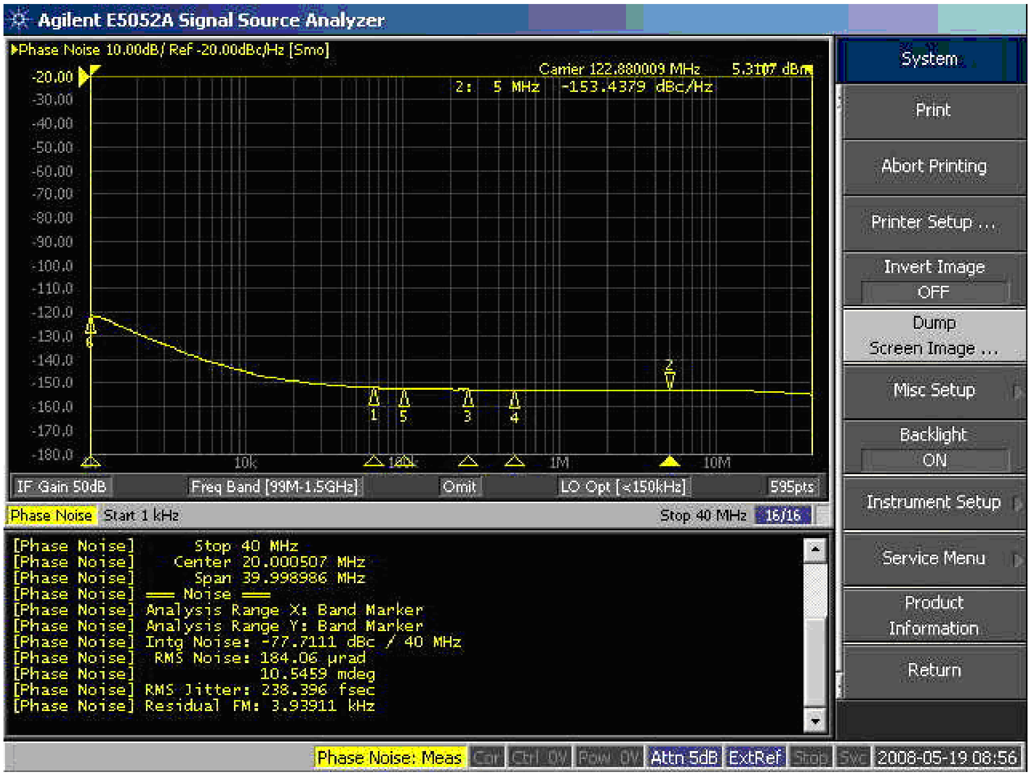

Figure 39. 122.88-MHz HS-LVPECL Output Phase Noise Profile (50 ps, RMS Input)

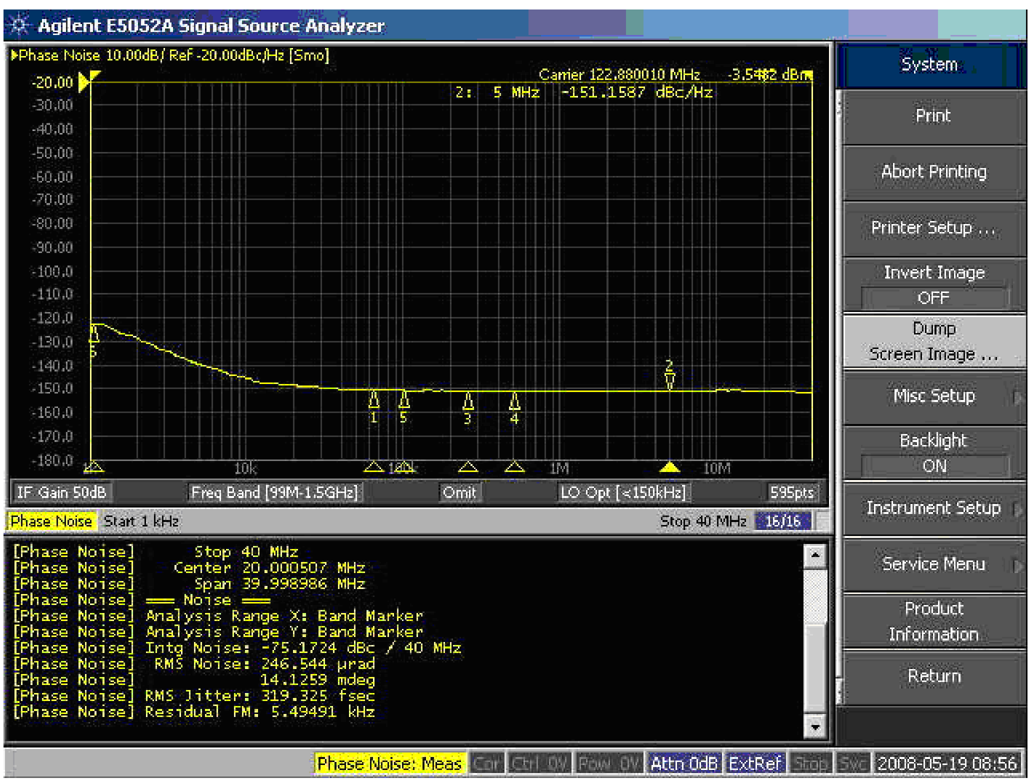

Figure 40. 122.88-MHz HS-LVDS Output Phase Noise Profile (50 ps, RMS Input)

5 Additive Phase Noise Measurements

Section 5.1 summarizes the additive phase noise/jitter measurements made on the CDCE72010 in an open loop configuration with a 491.52-MHz VCXO for /1, /2, /3, /4, and /5 output divider configurations for HS-LVDS, HS-LVPECL, and LVCMOS output types. Section 5.2 shows the 491.52-MHz LVPECL VCXO (TCO-2111) phase noise/jitter. The additive jitter can then be calculated in a specified integration band as shown in Equation 1.

$$t_{J,Additive} = \sqrt{t_{J,Output}^2 - t_{J,VCXO}^2} \quad (1)$$

5.1 Performance Summary

Table 3 lists the additive jitter capability of the CDCE72010.

Table 3. CDCE72010 Additive Jitter Capability Summary

Frequency (MHz)	Output Type	Phase Jitter (fs, RMS) 1 kHz to 40 MHz
491.52	HS-LVPECL	57
491.52	HS-LVDS	76
245.76	LVCMOS	196
245.76	HS-LVPECL	138
245.76	HS-LVDS	161
163.84	LVCMOS	200
163.84	HS-LVPECL	160
163.84	HS-LVDS	226
122.88	LVCMOS	242
122.88	HS-LVPECL	186
122.88	HS-LVDS	287
98.304	LVCMOS	182 (1 kHz to 20 MHz)
98.304	HS-LVPECL	136 (1 kHz to 20 MHz)
98.304	HS-LVDS	252 (1 kHz to 20 MHz)

5.2 Measurement Result

Figure 41 shows the phase noise profile of the 491.52-MHz LVPECL VCXO.

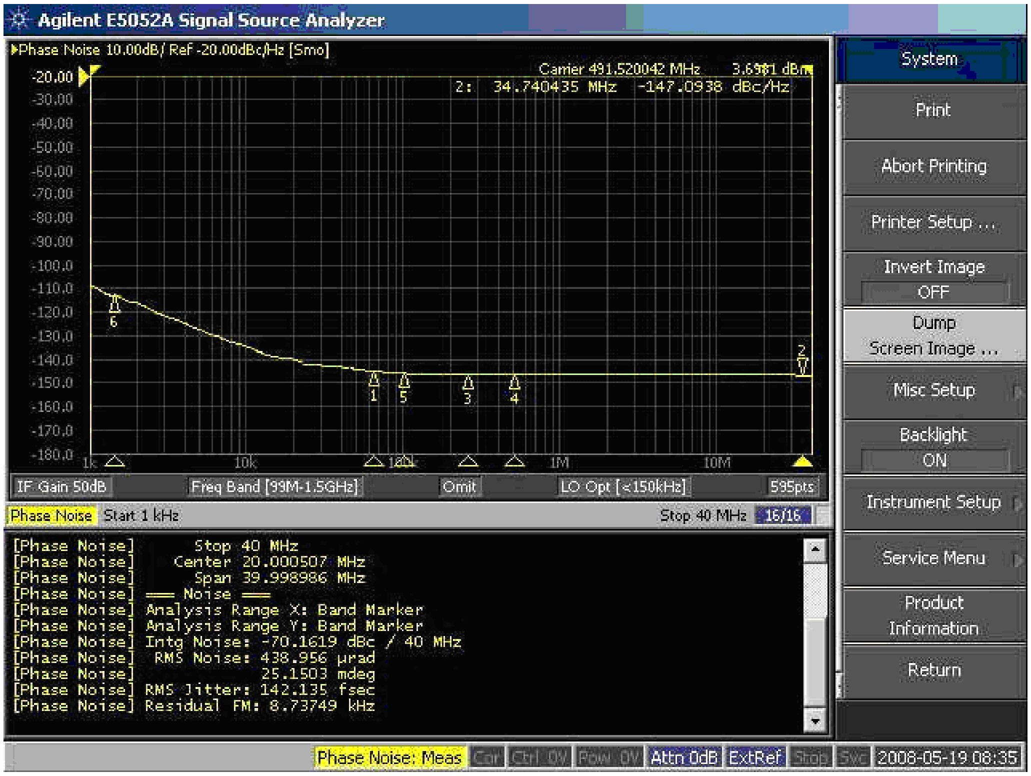

Figure 41. 491.52-MHz LVPECL VCXO (TCO-2111) Phase Noise Profile