Using the CDCE72010 as a Frequency Synthesizer

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ABSTRACT

This application report is a general guide for using the CDCE72010 from Texas Instruments as a frequency synthesizer. This document explains the methods to work with the phase-locked loop (PLL) of the CDCE72010 to achieve multiple output frequencies from any input frequency. It also describes the basic functionality and methods for using the device efficiently. Furthermore, it describes the clock termination method, decoupling the power-supply network with measurement results of the device PSRR, and presents several general applications.

Contents

List of Figures

1 Introduction

A phase-locked loop (PLL) is a closed-loop system that generates a signal related to the frequency and phase of an input reference signal. It typically involves locking its output (derived from a high-Q device) to its input, which is usually from a low-Q device. The PLL responds to input frequency and phase variations by automatically raising or lowering the frequency of the controlled oscillator through feedback, until the output is aligned with the system phase and frequency. A practical phase PLL usually assures lock in phase, but a lock in frequency with 0 ppm error has not yet been demonstrated. Typical commercial PLLs demonstrate ensured frequency lock with a margin of error.

PLLs are widely used for synchronization purposes in several communication and consumer domains, including radio transmission, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation, and clock distribution. PLLs typically used in high-performance, high-speed systems are required to have low noise/jitter clock outputs, and low clock skew, among other requirements.

1.1 High-Performance PLL Trends

High-performance, high-speed systems demand components that exhibit close-to-ideal characteristics, such that the precision is not compromised while ensuring that the systems themselves do not get overly complicated. In electronic systems, this approach has led to shifting all processing from the analog domain to the digital domain while the signal transmitting and receiving are performed in the analog domain. This shift means that high-performance systems generally have both analog and digital blocks as well as blocks to perform the analog-to-digital (A/D) and digital-to-analog (D/A) signal conversions. All the digital, A/D, and D/A blocks also require high-precision clocking that involves high-performance clock generation and distribution circuitry; typically, this circuitry is a high-performance PLL. For clocking very high performance devices such as high-resolution A/D converters, high-performance PLLs have traditionally relied on off-chip, high-Q mechanical devices such as voltage-controlled crystal oscillators to complete the feedback system in order to ensure high-quality outputs. Technology has not advanced enough to ensure a high-Q oscillator on silicon that integrates successfully with the rest of the PLL components to provide very low jitter clock outputs for these converters.

Texas Instruments' CDCE72010 is a device that uses an external voltage-controlled oscillator (VCO) or voltage-controlled crystal oscillator (VCXO) to synchronize to a backplane reference clock; it uses external components to set its PLL loop bandwidth while the other PLL components are on-chip. It also includes a SPI™ programming interface that enables the PLL to cover wide frequency ranges at its output and operate at a wide range of PLL bandwidths while ensuring very low noise/jitter over its entire operating range.

2 Functional Description

The CDCE72010 is a high-performance, low-jitter, and low skew clock synchronizer and jitter cleaner that synchronizes one of two reference clocks to the external VCXO frequency. The input reference clock can either be an LVPECL, LVDS, or LVCMOS signal. The CDCE72010 input buffers support either differential or single-ended signals and also provide the choice of turning on its internal termination (50 Ω single-ended to the respective V_{BB}) or use external termination for setting the bias voltage. The external VCXO can also either be an LVPECL, LVDS, or LVCMOS signal. Additionally, the CDCE72010 VCXO and Auxiliary input buffers support either differential or single-ended signals and provide the choice of turning on its internal termination (50 Ω single-ended to the respective V_{BB}) or use external termination for setting the bias voltage. The programmable predividers (M and N) give a high flexibility to the frequency ratio of the reference clock to output clock that operates up to 1.5 GHz.

Through the selection of external VCXO and loop filter components, the PLL loop bandwidth and damping factor can be adjusted to meet different system requirements. Each of the outputs can be programmed to either a total of 10 LVPECL/LVDS outputs, 20 LVCMOS outputs, or any combination through programming the SPI. The SPI also allows individual control of the frequency and enable/disable state of

each output. The device operates in a typical 3.3V- environment, and has an onboard EEPROM that allows for saving default startup conditions. The built-in latches ensure that all outputs are synchronized on device power-up or when the PLL is reconfigured after toggling the Reset pin. The device is ensured to be functional up to 500 MHz. The CDCE72010 is characterized for operation from 3.0 V to 3.6 V and from –40C to +85°C. Figure 1 shows a block diagram of the CDCE72010.

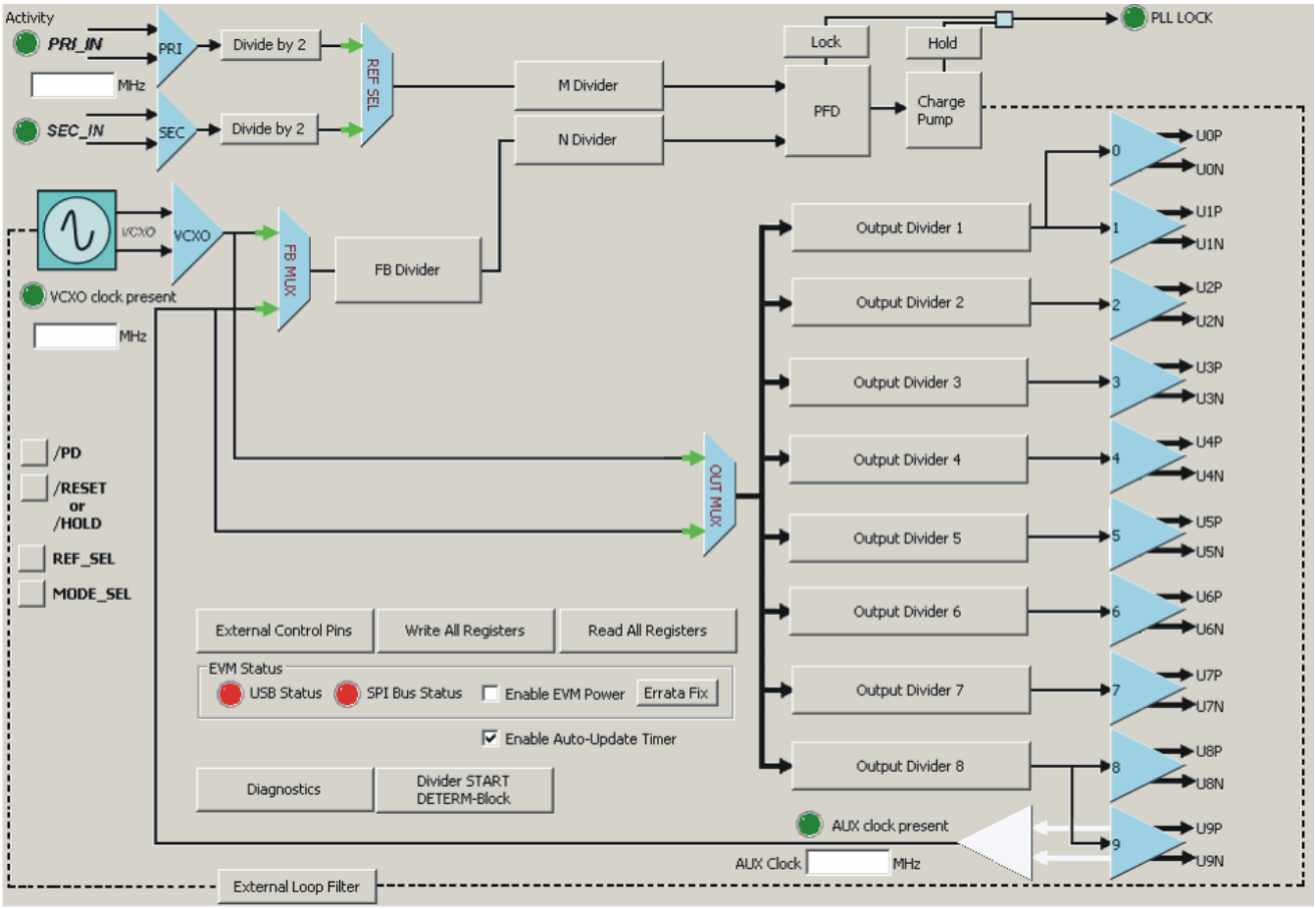

Figure 1. CDCE72010 Block Diagram

2.1 Clock Synthesizer

As shown in Figure 1, the CDCE72010 has internal dividers, a phase frequency detector, charge pump, and LVPECL/LVDS/LVCMOS input and output buffers. Together with an external VCXO and loop filter, the device completes a PLL. Through the PLL operation, the VCXO input clock synchronizes with the reference clock input, and ultimately with all clock outputs. All outputs are completely synchronized in terms of phase and frequency with the reference clock input.

2.2 Frequency Multiplication and Division

Through programming the SPI, the predividers M and N can be set from 1 to 16384. Depending on the integer values of these two dividers, the output frequency can be fixed to almost any integer or fractional number of the input frequency within the specified frequency range as stated in the product data sheet (note that a VCXO with the correct frequency is required to generate the corresponding application frequency). Choosing the values of M and N determines the reference and feedback frequencies for the phase frequency detector (PFD); these two frequencies must be the same. It is recommended to use the same M and N predividers, if possible, for best PLL performance. The outputs are directly related to the VCXO input frequency. The output frequency can be scaled down by a value of 1, 2, 3, 4, 5, 6, and so on up to 80.

2.3 Jitter Cleaner

The advantage of having an external VCXO and loop filter is that a wide range of PLL loop bandwidths, as well as low noise VCXO, can be chosen depending on the jitter requirements of the system. The jitter cleaning action depends on the PLL loop bandwidth. Up to the loop bandwidth level, all noise (jitter) passes through the filter; above the loop bandwidth, all signal noise is cleaned. The ideal loop bandwidth is chosen such that the reference clock source starts to exceed the VCXO noise floor. If the input has a great deal of jitter, this noise can be cleaned by selecting a low loop bandwidth. For the CDCE72010, a low loop bandwidth (in the sub-10-Hz range) can be achieved. The CDCE72010 itself adds a low noise to its outputs. For jitter cleaning operation, the VCXO noise performance is critical. Thus, with a proper loop bandwidth and applicable VCXO, the CDCE72010 can function as a jitter cleaner.

2.4 Clock Distribution with Dividing Options

The CDCE72010 has 10 differential (LVPECL/LVDS) or 20 single-ended (LVCMOS) outputs, or any combination of outputs. The frequency of each output is directly related to the VCXO input with an output divider of /1, /2, /3, /4, /5, and so on up to /80. Each output can be programmed individually using the SPI.

2.5 Phase Adjustment

Each output on the CDCE72010 can also be phase adjusted; the granularity of the phase adjustment depends on the output divide value. For any output divide from the allowable ratios, the number of phase setting options (including the current zero phase shift) is ***P***. The phase adjust granular step size is ($2\pi/P$), where *P* is the output divide value. For example, say P is selected as 4. Then, the total number of phase offsets that can be chosen for a bank of outputs is 4; the phase adjust granular step size is $\pi/2$, or 90 degrees. The input-to-output phase can also be shifted up to ±2.75 ns through the SPI. This adjustment can be performed accurately through the SPI with certain steps.

2.6 External Feedback Option

Output Y9 of the CDCE72010 can also be configured as an auxiliary input to the PLL and/or outputs, and thus can be configured as an external feedback option. This technique offers the user the ability to configure the device as a zero-delay buffer to reduce the input/output phase offset. This auxiliary input can also be used with a different frequency VCXO (separate from the VCXO frequency at the device VCXO input), and thus can be used with the ability to support multiple frequency plans (in this type of configuration, either VCXO is used at any given time).

3 CDCE72010 Frequency Synthesis

This section provides some insight on choosing the input frequency, divider, and VCXO settings needed to generate a particular set of output frequencies using the multiple outputs of the CDCE72010 device.

3.1 Single VCXO, Multiple Frequency Synthesis Example

Assume a typical application, where a total of two 192-MHz LVPECL, two 384-MHz LVPECL, two 38.4-MHz LVCMOS, two 76.8-MHz LVDS, and one 153.6-MHz LVPECL output clocks are desired and should be phase-locked to a single backplane 10-MHz input reference clock. The goal of this example is to identify the M, N, feedback (FB), and output (P) divider values, the VCXO frequency to lock to, and the related PLL settings necessary to derive the different output frequencies from the common input and VCXO frequencies. The following steps may be followed to achieve this goal.

Step 1. From Figure 1, it can be inferred that the relationship between the output frequency and the input frequency is described by these equations:

$$F_{OUT} = F_{IN} \times \frac{(N \times FB)}{(M \times P)}$$

where:

- $F_{VCXO} = F_{OUT} \times P$

Provided that:

- $(F_{IN}/M) < 100$ MHz
- $(F_{OUT} \times P) < 1500$ MHz

Step 2. Keep these parameters in mind while satisfying the equations in Step 1:

- The P divider can be chosen from 1, 2, 3, 4, 5, up to 80.
- The external VCXO range is up to 1.5 GHz.
- The M and N dividers can be chosen from 1 to 16384, and are operational up to 250 MHz.
- The FB divider can be chosen from 1, 2, 3, 4, 5, up to 80.
- It is better to have the M and N dividers be equal (or close to each other) for optimal PLL performance.

Step 3. Given multiple desired output frequencies and the input frequency, the first step would then be to establish the M, N, and FB divider values for different P divider settings in order to satisfy these equations:

$$F_{IN} = F_{OUT1} \times (M \times P_1) \times (N \times FB)$$
$$F_{IN} = F_{OUT2} \times (M \times P_2) \times (N \times FB)$$
$$F_{IN} = F_{OUT3} \times (M \times P_3) \times (N \times FB)$$
$$F_{IN} = F_{OUT4} \times (M \times P_4) \times (N \times FB)$$
$$F_{IN} = F_{OUT5} \times (M \times P_5) \times (N \times FB)$$
$$F_{VCXO} = F_{OUT1} \times P_1 = F_{OUT2} \times P_2 = = F_{OUT3} \times P_3 = F_{OUT4} \times P_4 = F_{OUT5} \times P_5$$

Such that these parameters are valid:

- The common PFD frequency always is less than 100 MHz.
- The M and N divider input frequencies are always less than 250 MHz
- The VCXO frequency is the same for deriving all outputs

For our example of deriving these outputs, in order to use a common VCXO frequency, the P dividers to be used are:

- P1 = 4
- P2 = 2
- P3 = 20
- P4 = 10
- P5 = 5

The common VCXO frequency is 768 MHz. Moreover, the FB divider to be used is:

FB = 80

The N divider to be used is:

N = 120

These values ensure that the (F_{IN}/M) ratio is within 100 MHz and is set at 80 kHz. Thus, the M divider value to be used is (M = 125).

Figure 2 illustrates this configuration.

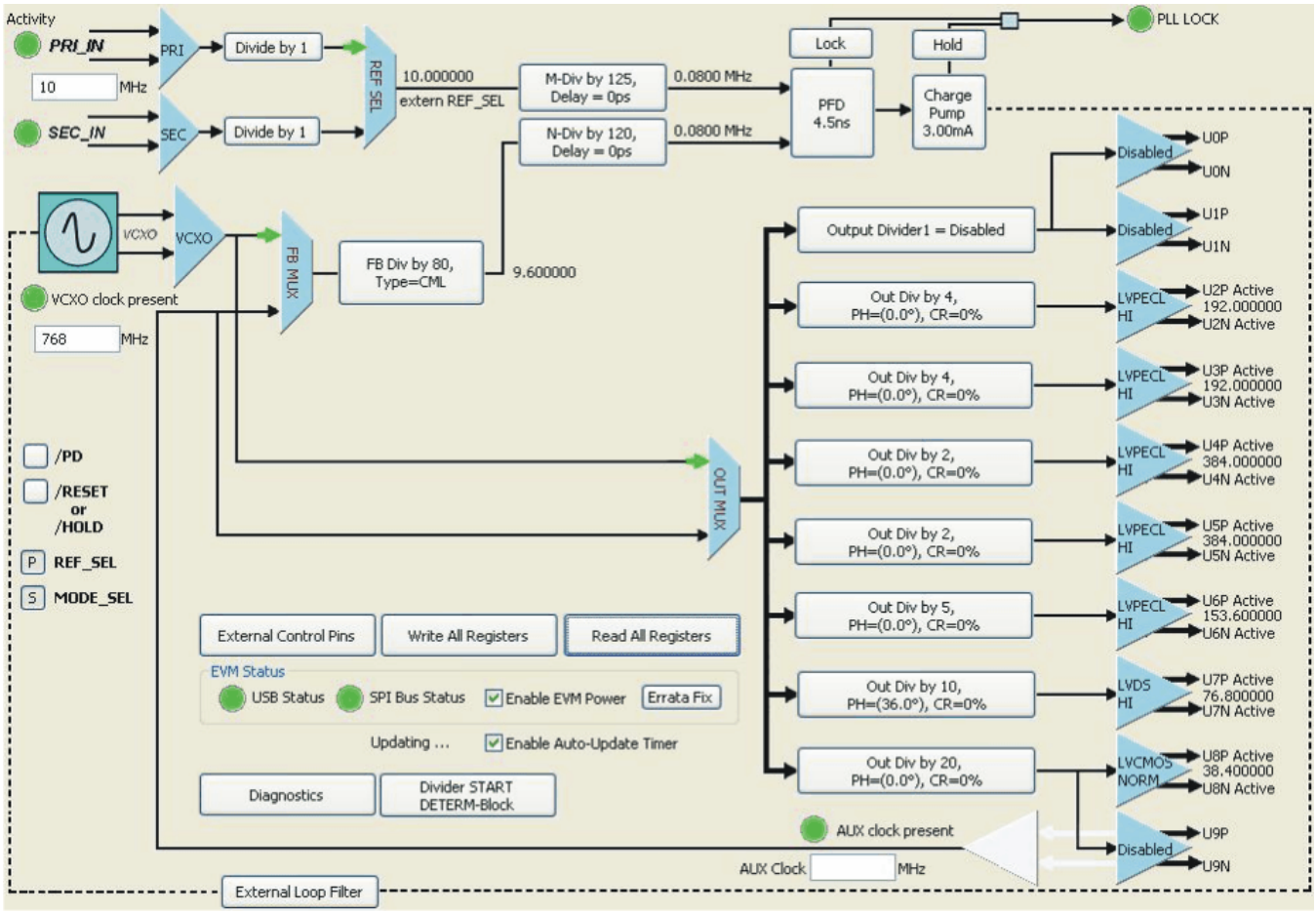

Figure 2. CDCE72010 Programming Settings for Single VCXO, Multiple Frequency Synthesis Example

3.2 Single Frequency Synthesis Example

Assume that in addition to achieving the frequencies shown in the first example with a 768-MHz VCXO, another requirement exists. A second frequency plan must be established where a 491.52-MHz VCXO must be used at the Auxiliary input. Working through the process as shown in Section 3.1 for the 768-MHz VCXO, the P dividers to be used are:

- P1 = 4
- P2 = 2
- P3 = 20
- P4 = 10
- P5 = 5

Moreover, the FB divider to be used is:

FB = 80

The N divider to be used is

N = 120

These values ensure that the (F_{IN}/M) ratio is within 100 MHz and is set at 80 kHz. Thus, the M divider value to be used is (M = 125). Figure 3 shows this configuration.

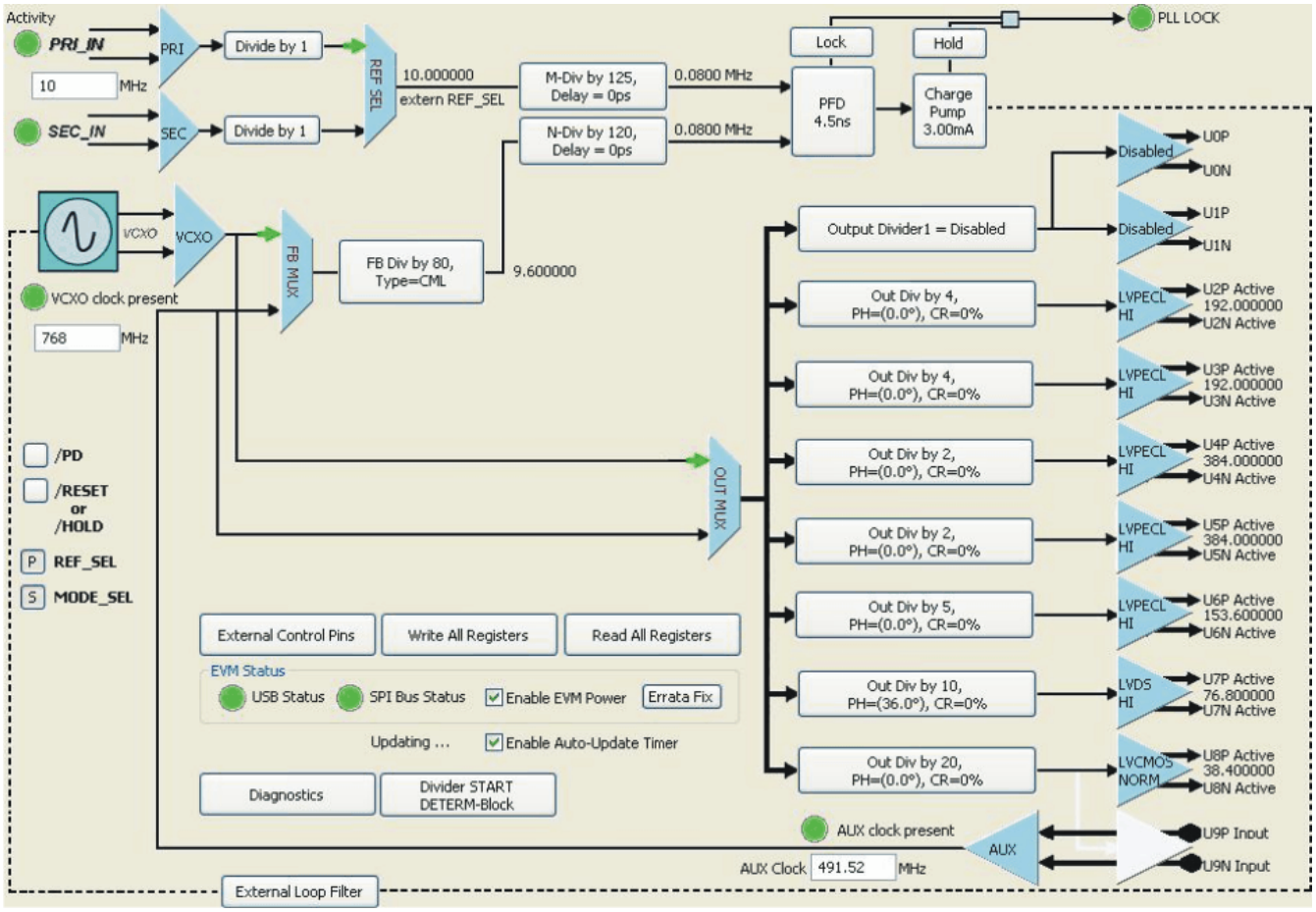

Figure 3. CDCE72010 Programming Settings for Multiple VCXO Frequency Synthesis Example (768-MHz VCXO)

Following the steps summarized in Section 3.1 a second time for the 491.52-MHz VCXO at the Auxiliary input, the P dividers to be used are:

- P1 = 4
- P2 = 2
- P3 = 20
- P4 = 10
- P5 = 5

Moreover, the FB divider to be used is:

FB = 48

The N divider to be used is:

N = 128

These values ensure that the (F_{IN}/M) ratio is within 100 MHz and is set at 80 kHz. Thus, the M divider to be used is (M = 125). Figure 4 illustrates this approach.

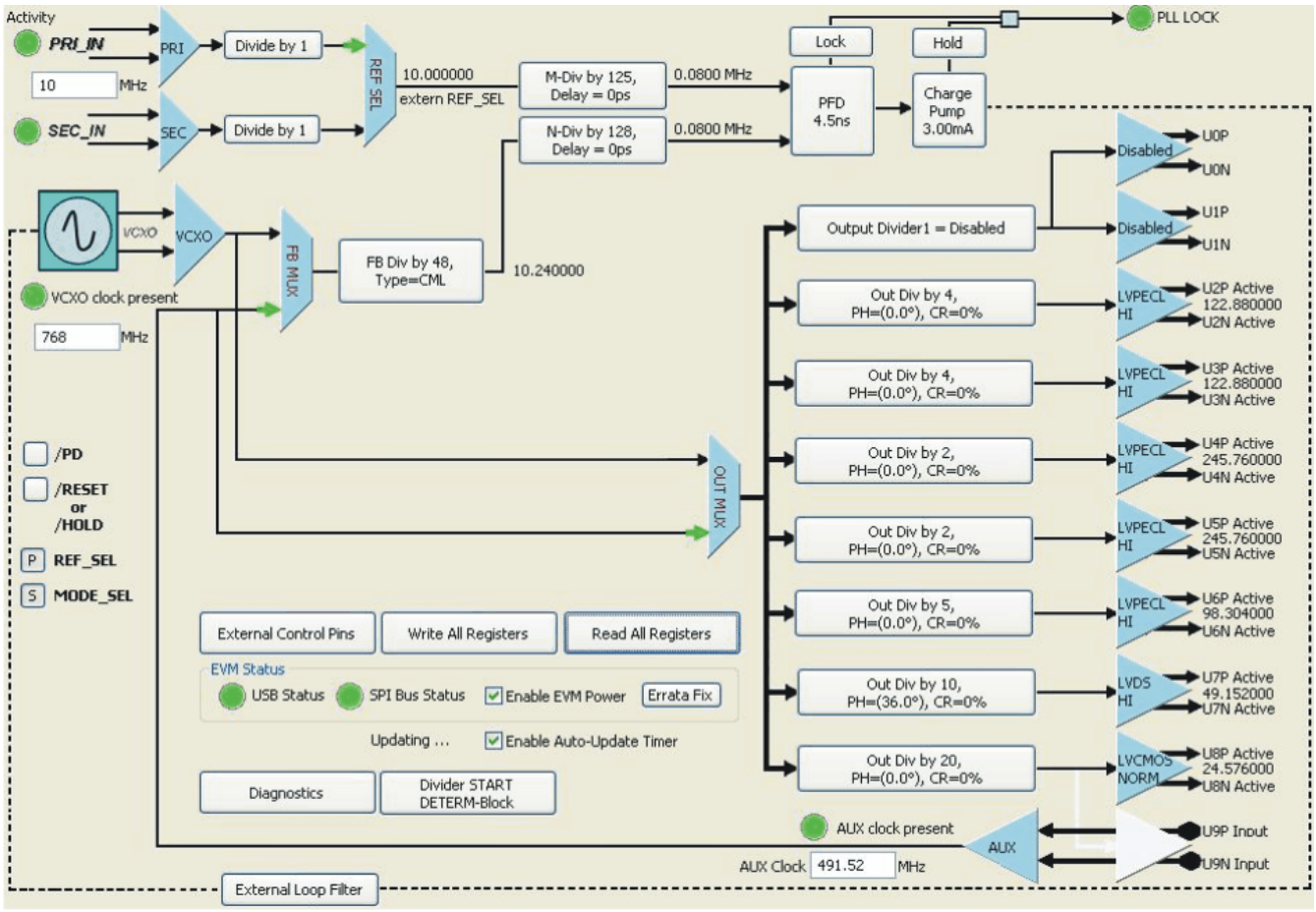

Figure 4. CDCE72010 Programming Settings for Multiple VCXO Frequency Synthesis Example (491.52-MHz VCXO)

4 CDCE72010 Default Configuration

The CDCE72010 onboard EEPROM has been factory preset to the following default settings, as shown in Figure 5:

- REG0 = 002C0040
- REG1 = 83840051
- REG2 = 83400002
- REG3 = 83400003
- REG4 = 81800004
- REG5 = 81800005
- REG6 = EB040006
- REG7 = EB040717
- REG8 = 010C0158
- REG9 = 01000049
- REG10 = 0BFC07CA
- REG11 = C000058B
- REG12 = 61E09B0C

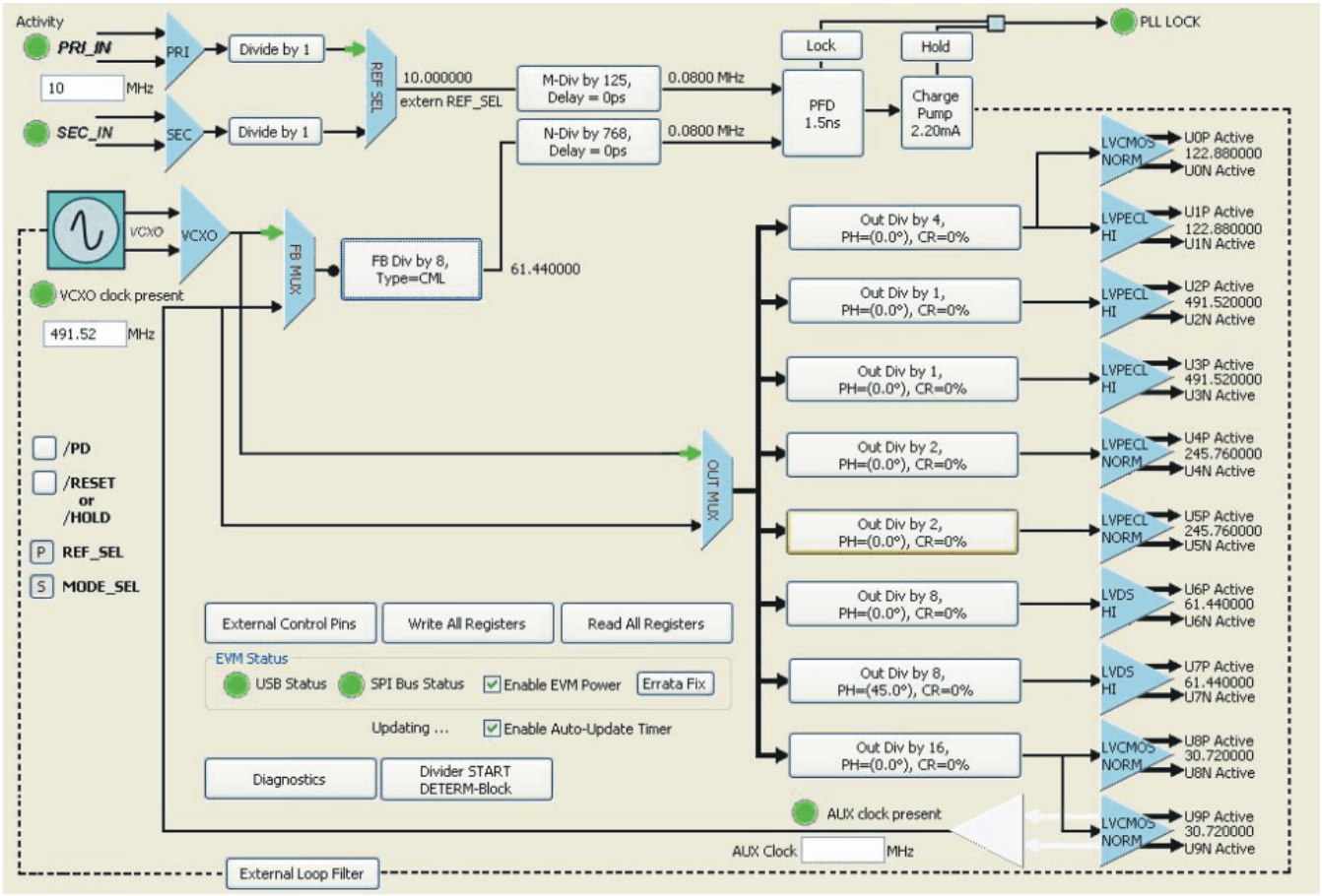

Figure 5. CDCE72010 Default Startup Settings (491.52-MHz VCXO)

5 VCXO Selection Guidelines

The CDCE72010 has the ability to be driven by a LVPECL, LVDS, or LVCMOS VCXO. It features internal termination to the respective bias voltage or can alternatively be selected to have external termination for bias setting. LVCMOS VCXOs are measured to have the best phase noise floor, followed by LVPECL and LVDS. Table 1 lists several recommended VCXO vendors.

Table 1. Recommended Crystal Manufacturers

Manufacturer	Part Number
Epson-Toyocom	TCO-21xx
Vectron	VS-7xx

6 CDCE72010 PLL Bandwidth Selection

Unlike other PLLs, the CDCE421 loop filter components and charge pump current are not fixed. It is possible to choose a loop bandwidth from the range of less than 10 Hz to a few MHz in value.

6.1 Loop Bandwidth

The PLL bandwidth depends on the loop filter, charge pump current, VCO gain, and phase frequency detector (PFD) update frequency. The pre/post dividers determine the PFD update frequency, as Figure 6 shows.

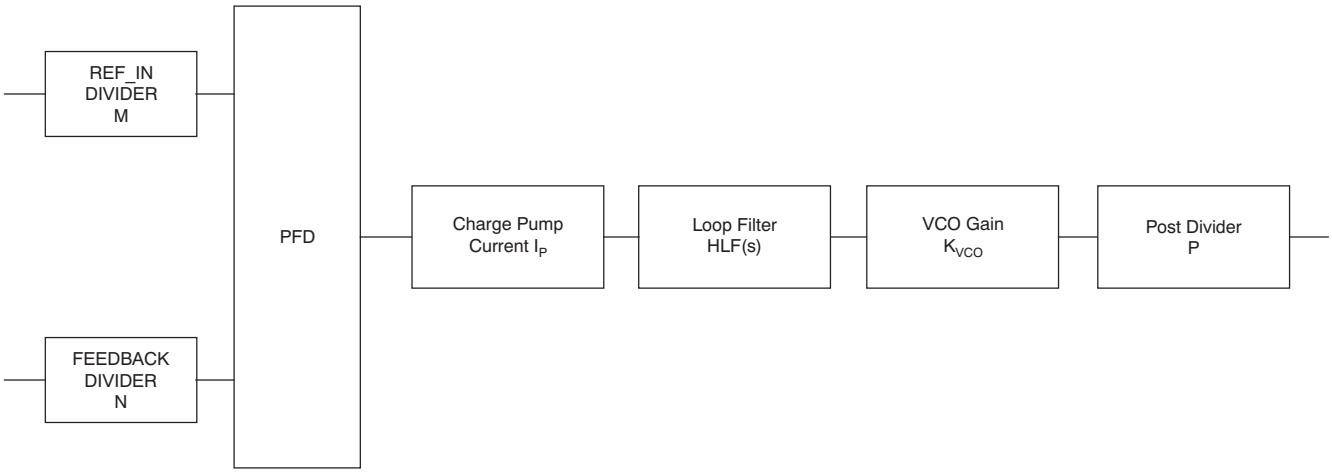

Figure 6. PLL Bandwidth Dependencies

6.2 Jitter Peaking

Around the loop bandwidth, any incoming jitter from the reference clock may be amplified. This phenomenon is called *jitter peaking*. In some applications, this peaking has an adverse effect on overall jitter performance ***if*** the jitter peaking occurs within the band of interest. If the jitter peaking occurs outside the band of interest, the application generally suffers no adverse effects. In any case, care should be taken to limit jitter peaking to within 10 dB in order to prevent the loop from becoming unstable. An example of a PLL phase response with jitter peaking of 2 dB is shown in Figure 7.

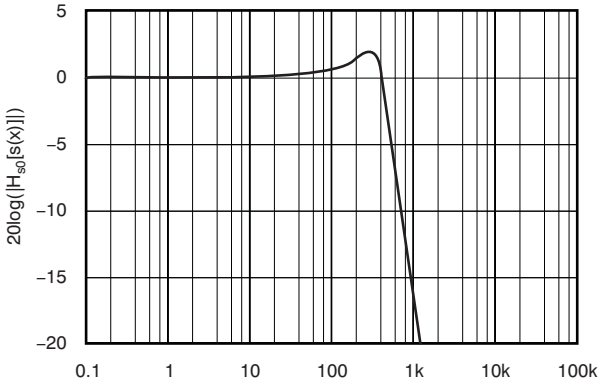

Figure 7. Jitter Peaking Around PLL Bandwidth

6.3 Phase Margin

Phase margin is important for PLL stability and influences the PLL lock time. How quickly the PLL output settles to its final value depends on the PLL phase margin. As a rule of thumb, a minimum 30-degree phase margin is recommended for stable clock operation.

7 Allowable CDCE72010 Loop Filter Topologies

The CDCE72010 can be configured with two types of loop filters. First, the device can support an external operational amplifier as part of an active loop filter topology. Additionally, an external RC passive filter can also be used and is recommended for loop filters, because it does not add noise to the charge pump output. If the VCXO input impedance is low, an active loop filter is recommended; this type of loop filter can handle a lower impedance by compensating for leakage currents.

7.1 Recommended PLL Bandwidth

The PLL loop bandwidth of the CDCE72010 is recommended to be set according to the phase noise profile of its reference input and the phase noise profile of the VCXO clock. It is recommended to set the PLL loop bandwidth as the crossover point of the reference input phase noise and the phase noise of the VCXO clock. When the input clock is clean and any near-frequency offset are better than the VCXO clock, it is beneficial for the PLL bandwidth to be at a few kHz as determined by the crossover point. This configuration is illustrated in Figure 8.

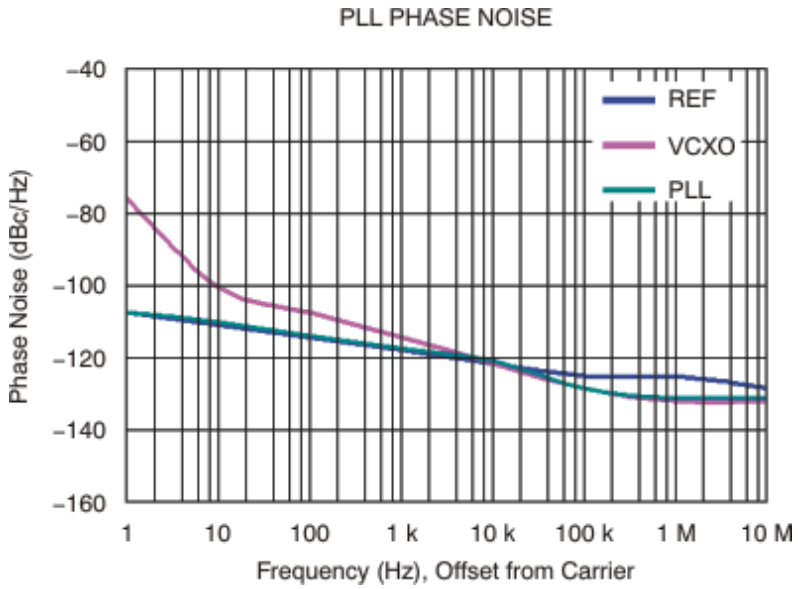

Figure 8. PLL Loop Bandwidth for Clean Reference Inputs

When the input clock is *dirty* and at most frequency offsets worse than the VCXO clock, it is beneficial for the PLL bandwidth to be as low as possible (preferably below 10 Hz), as determined by the crossover point; this approach is shown in Figure 9.

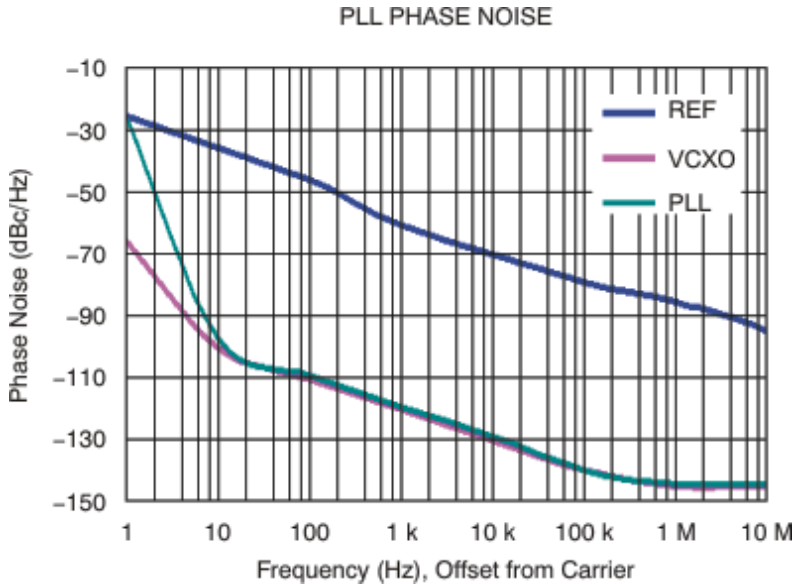

Figure 9. PLL Loop Bandwidth for Dirty Reference Inputs

8 Output Termination

The CDCE72010 is a 3.3-V clock driver that has the following available output types: LVDS, LVPECL, or LVCMOS.

8.1 LVPECL Termination

The CDCE72010 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination is required to ensure correct operation of the device and to ***maintain*** signal integrity. Proper termination for LVPECL outputs is a 50-Ω to (V_{CC} – 2 V) supply, but this dc voltage is not readily available on a printed circuit board (PCB). Either a direct termination or ac-coupled terminations can be used to terminate the LVPECL outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

8.1.1 Direct Coupled LVPECL Termination

In order to eliminate the necessity of having a (V_{CC} – 2 V) supply on the board, a Thevenin equivalent network composed of two resistors with 3.3-V supply replace the 50-Ω to (V_{CC} – 2 V) to ensure required biasing and termination. Figure 10 shows a recommended termination circuit for direct termination.

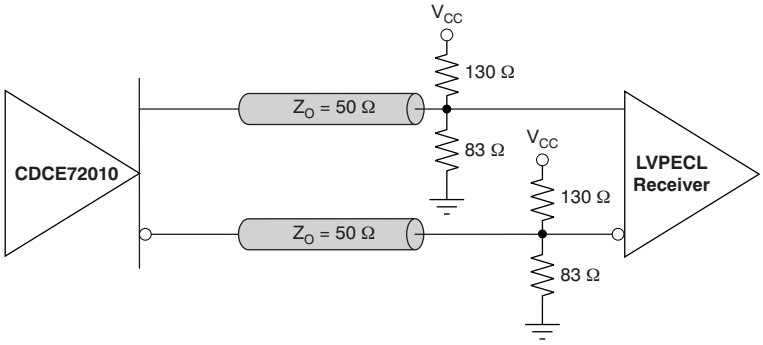

Figure 10. LVPECL DC Termination Circuit

8.1.2 LVPECL DC Termination Circuit

If ac-coupled termination is used, the input and output stages must be biased properly. The 150-Ω resistor close to the CDCE72010 ensures proper output biasing, while the 1.3-kΩ and 2-kΩ resistor network bias the LVPECL receiver input stage. Figure 11 shows a recommended termination circuit for ac-coupled termination.

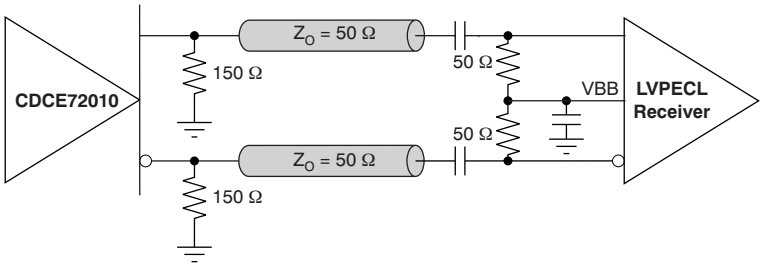

Figure 11. LVPECL AC-Coupled Termination Circuit

8.2 LVDS Termination

The CDCE72010 has on-chip, 100-Ω termination between the two LVDS outputs. Therefore, no additional biasing is needed, but termination is required to ***maintain*** signal integrity. The proper termination for signal integrity over two 50-Ω lines is a 100-Ω resistor between the outputs on the receiver end. Either a direct termination or ac-coupled terminations can be used to terminate the LVDS outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

8.2.1 Direct Coupled LVDS Termination

Figure 12 shows a recommended termination circuit for direct termination of LVDS outputs for an LVDS receiver that is assumed to have on-chip, 100-Ω termination between the outputs.

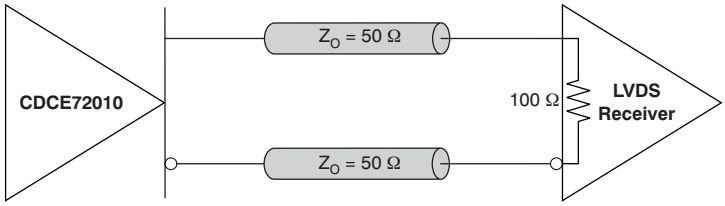

Figure 12. LVDS DC Termination Circuit

8.2.2 AC-Coupled LVDS Termination

Figure 13 shows a recommended termination circuit for ac-coupled termination of LVDS outputs for an LVDS receiver that is assumed to have on-chip, 100-Ω termination between the outputs.

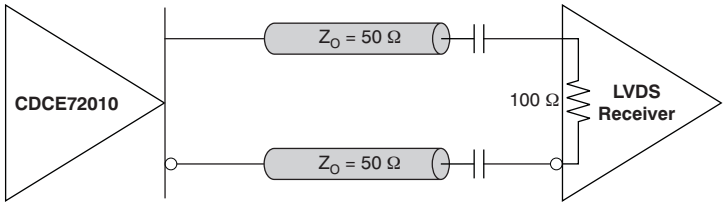

Figure 13. LVDS AC-Coupled Termination Circuit

8.3 LVCMOS Termination

Each differential output of the CDCE72010 can be configured to two single-ended, 3.3-V LVCMOS outputs. For a 3.3-V system, direct coupling is recommended as shown in Figure 14. For other supply voltage systems, direct coupled voltage dividers are recommended to achieve acceptable receiver LVCMOS levels.

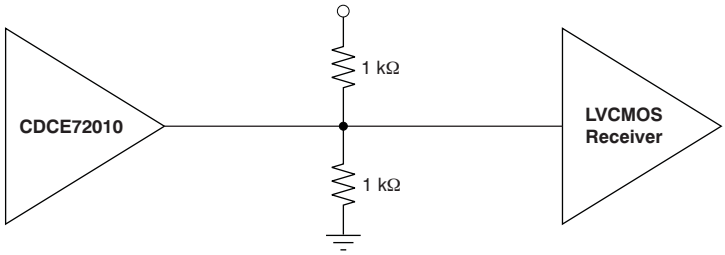

Figure 14. 3.3V LVCMOS DC-Coupled Termination Circuit

9 Input Termination

The CDCE72010 is a 3.3-V clock driver that has an option of the following reference input types: LVPECL, LVDS, or 3.3-V LVCMOS. It provides the option of using its internal 50-Ω, single-ended termination resistors to V_{BB} which can be set accordingly. In this case, when the input buffer is properly chosen for ac or dc coupling (according to the selected biasing for the driver circuit) along with input termination, no external termination is needed.

9.1 LVPECL Input (No Internal Termination)

The proper termination for LVPECL is a 50-Ω to (V_{CC} – 2 V) supply, but this dc voltage is not readily available on a board. Either a direct termination or terminations for ac-coupling can be used to terminate the LVPECL outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

9.1.1 Direct Coupled LVPECL Termination

In order to eliminate the necessity of having a (V_{CC} – 2 V) supply on the board, a Thevenin equivalent network composed of two resistors with a 3.3-V supply replace the 50-Ω to (V_{CC} – 2 V) supply to ensure required biasing and termination. Figure 15 shows a recommended termination circuit for direct termination.

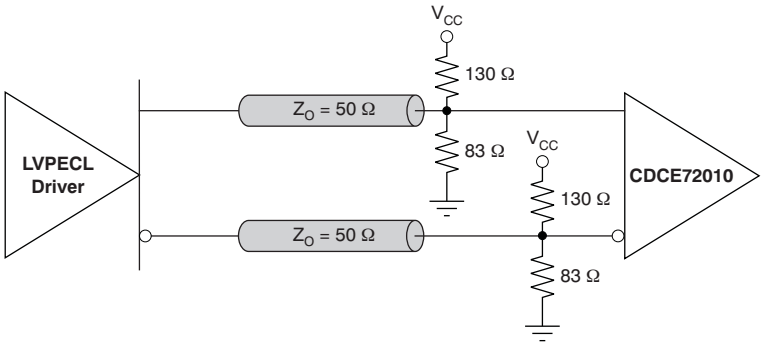

Figure 15. LVPECL DC Termination Circuit

9.1.2 AC-Coupled LVPECL Termination

If ac-coupled termination is used, the input and output stages must be biased properly. The 150-Ω resistor close to the driver ensures proper output biasing, while the 1.3-kΩ and 2-kΩ resistor network bias the CDCE72010 LVPECL input stage. Figure 16 shows a recommended termination circuit for ac-coupled termination.

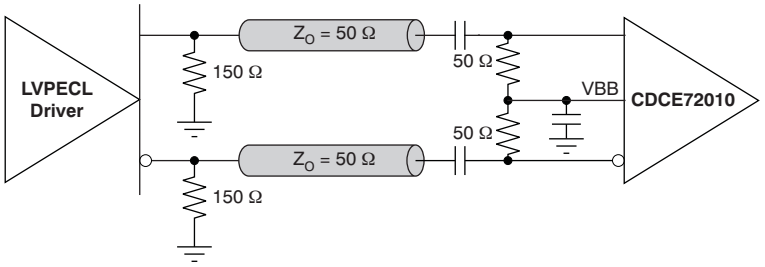

Figure 16. LVPECL AC-Coupled Termination Circuit

9.2 LVDS Termination (No Internal Termination)

The proper termination for signal integrity over two 50-Ω lines is a 100-Ω resistor between the outputs on the receiver end. Either direct termination or terminations for ac-coupling can be used to terminate the LVDS outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltage of the driver and receiver are different, ac-coupling is required.

9.2.1 Direct Coupled LVDS Termination

Figure 17 shows a recommended termination circuit for direct termination of the LVDS outputs for LVDS inputs on the CDCE72010.

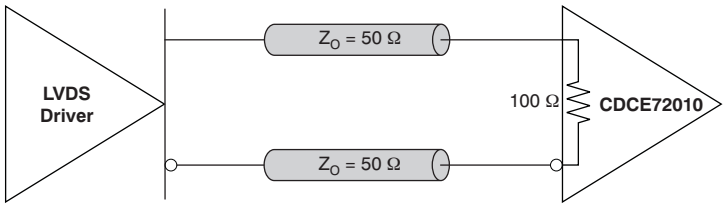

Figure 17. LVDS DC Termination Circuit

9.2.2 AC-Coupled LVDS Termination

Figure 18 shows a recommended termination circuit for ac-coupled termination of the LVDS outputs for LVDS inputs on the CDCE72010.

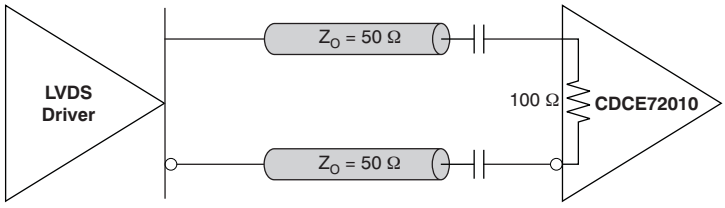

Figure 18. LVDS AC-Coupled Termination Circuit

9.3 LVCMOS Termination

For a 3.3-V driver, direct coupling is recommended as shown in Figure 19 to interface to the LVCMOS inputs on the CDCE72010.

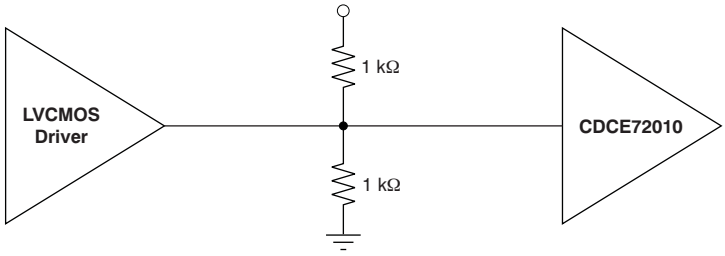

Figure 19. 3.3-V LVCMOS DC-Coupled Termination Circuit

10 Power-Supply Decoupling

PLL-based frequency synthesizers are very sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. This characteristic is especially true for analog-based PLLs. Therefore, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL would have attenuated jitter because of power supply noise at frequencies beyond the PLL bandwidth as a result of attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, whereas the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. Inserting a ferrite bead between the board power supply and the chip power supply isolates the high-frequency switching noise generated by the clock driver, preventing it from leaking into the board supply. Choosing an appropriate ferrite bead with low dc resistance is important because it is imperative to maintain a voltage at the CDCE72010 power-supply pin that is above the minimum voltage needed for its proper operation. At dc, the ferrite bead would have a voltage drop across itself; the maximum drop would depend on its maximum dc resistance and the maximum dc current that the CDCE72010 would draw from the 3.3-V power supply.

For proper operation, the CDCE72010 requires a minimum power-supply voltage of 3 V and draws a maximum supply current of 1400 mA. The split for the power-supply currents among the power-supply pins on the CDCE72010 follows this configuration:

- VCC_PLL draws a maximum supply current of 100 mA
- VCC_A and VCC_IN draw a maximum supply current of 50 mA each
- VCC_CP and VCC_VCXO draw a maximum supply current of 25 mA each
- VCC_OUT (for all output supplies) draws a maximum supply current of 1200 mA

Assuming a 3.3-V board supply, the ferrite bead maximum dc resistance for VCC_PLL can be 3 Ω; for VCC_A and VCC_IN , the resistance can be 6 Ω each; for VCC_CP and VCC_VCXO, it can be 12 Ω each; and for VCC_OUT it can be 0.25 Ω. Figure 20 shows a general recommendation for decoupling the power supply for each of the following power supply pins: VCC_PLL, VCC_IN, VCC_A, VCC_CP, VCC_VCXO, and VCC_OUT. For each power-supply pin in the device, it is also recommended to add an additional 0.1 μF to filter out any power-supply noise that might creep into the sensitive PLL power supplies.

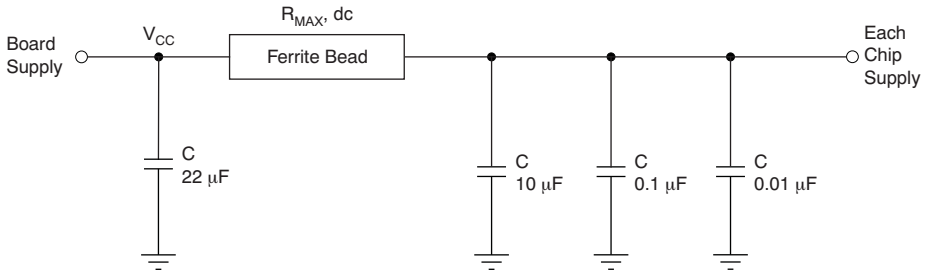

Figure 20. Power-Supply Decoupling

11 Application Example—Providing Low-Phase Noise Clocks to D/A and A/D Converters

D/A and A/D converters require low-noise clock signals to ensure adequate signal-to-noise ratios (SNR) and effective numbers of bits (ENOB). The clocking requirement becomes more pronounced at high analog input bandwidths of the data converters. The CDCE72010 can generate low-noise clock signals using an external VCXO and low PLL loop bandwidth. The PLL itself adds less than 0.1 ps, RMS (over 12-kHz to 20-MHz bandwidth) jitter to the outputs. Figure 21 shows a clocking solution for a typical wireless base station system.

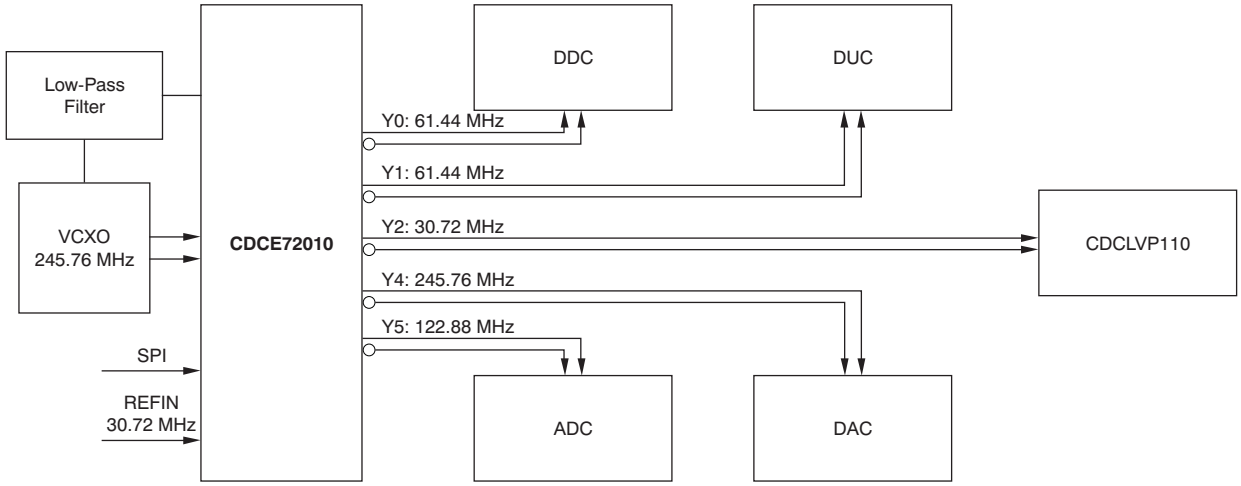

Figure 21. Typical Wireless Base Station System Clocking Solution

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