Application Report
SCAA088–March 2008

Generating Low Phase-Noise Clocks for Audio Data Converters from Low Frequency Word Clock

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ABSTRACT

Generating a high-frequency system clock F_S ($128f_s$ to $768f_s$) from a low-frequency sampling clock f_s (10 kHz to 200 kHz) is challenging, while attempting to maintain low phase jitter. A traditional phase-lock loop (PLL) can do the frequency translation, but the added phase jitter prevents the generated system clock signal from effectively driving high-performance audio data converters. This application note discusses how a low-cost and low-phase noise clocking solution can be synthesized from a distributed sampling clock using a CDCE913 VCXO/PLL and a CD74HC4046A phase detector.

Introduction

For many audio applications a sampling clock or *word clock* of 44.1 kHz or 48.0 kHz is available through a distribution network. The audio data converters in such applications are often Delta-Sigma, modulator-based devices that can over-sample the signal by a factor of up to 512, resulting in a system clock of 22.5792 MHz or 24.5760 MHz. This system clock must be synchronized with the low-frequency sampling clock using a phase-locked loop (PLL), but the sampling clock is often too low in frequency for use with many PLL-based clock drivers. Some audio PLLs can accept the low frequency sampling clock, but create so much jitter on the system clock, that performance degrades.

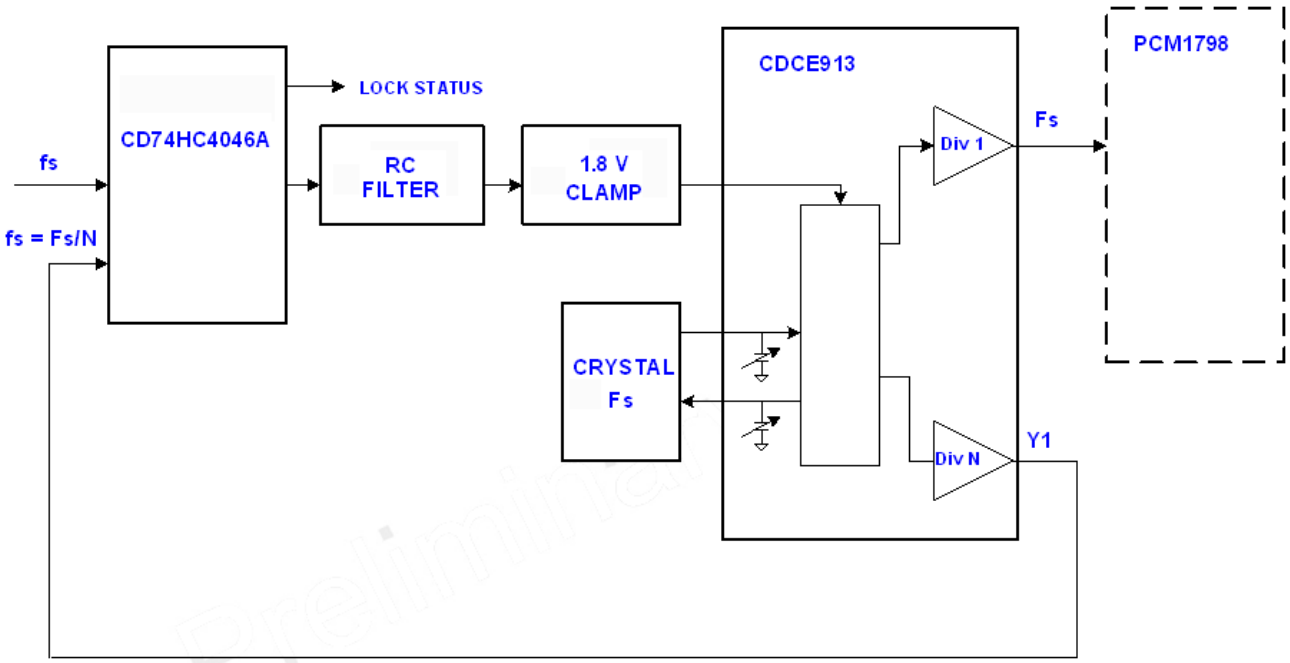
The CDCE913 is a PLL-based clock driver with a VCXO input. It can drive a fundamental mode crystal in the range of 8 to 32 MHz or receive a 1.8 V LVCMOS clock ranging from 8 to 160 MHz. Like most PLLs, if the PLL internal to the CDCE913 is used to generate the system clock, it generates too much long-term jitter; even though it has an excellent short-term period jitter performance of typically 60 ps peak-to-peak. If we use its VCXO capabilities for synchronization and create a very low-loop bandwidth PLL, using an external phase comparator (CD74HC4046A) and loop filter; a complete PLL is formed with excellent long-term jitter performance and jitter-cleaning properties.

References

- CDCEx913 TI data sheet (SCAS849)
- CDx4HCx4046A TI data sheet, (SCHS204)
- VCXO Application Guideline for CDCE(L)9xx Family TI application report, (SCAA085)

The System Level Block Diagram

Figure 1. Functional Block Diagram



Functional Block Diagram Description

The CD74HC4046A in Figure 1 is a complete Phase-Locked-Loop circuit containing a linear VCO and three different phase comparators. In this application, the internal VCO and two of the phase detectors are not used. The remaining comparator, PC2, is used to generate an error signal based on the phase difference of signal input (sample frequency) and a divided-down feedback signal from the CDCE913. This device offers an analog status pin which can indicate whether the PLL is locked. The Phase detector's output controls the VCXO of the CDCE913 through a simple RC loop filter. A 1.8 V clamp circuit is required as the VCXO input is limited to 1.8 V and the output of the RC loop filter could far exceed this. Any comparator with an open-collector output can be used as a clamp as shown in the schematic of Figure 5.

In this application the CDCE913 requires a crystal having a center frequency equal to the desired system clock frequency. The Y1 output has a 10-bit divider that divides down the VCXO frequency to f_s for the external phase comparator. The PLL internal to the CDCE913 is bypassed, and the remaining Y2, Y3 outputs are connected directly to the data converters with an optional division stage.

Like any PLL, the system clock (F_s) is synchronized with the sampling clock frequency (f_s).

Using the CDCEx913 as a Low Phase Noise Clock Generator

The CDCE913 is a TI programmable clock synthesizer. The core supply voltage as well as control voltage range for the VCXO input is 1.8 V. This device has an internal fractional-N PLL that can also be used in some applications, but for this application note it will by bypassed.

The device can be programmed through an I^2C interface and it has an EEPROM capable of permanently storing programmed settings. Pre-programmed parts based on the custom requirements are also available through TI or a third party. The CDCE913 has three control pins (Figure 2 and Figure 3) and these control pins are also programmable.

The CDCE913 offers three outputs, Y1–Y3, each having a dedicated divider. One of the outputs (Y1) has 10 bit divider capable of division up to 1024. In this application, this output is chosen as feedback for the external phase comparator to eliminate the need for external frequency division. The outputs levels may be 3.3 V or 2.5 V LVCMOS. If 1.8 V LVCMOS outputs are required, then CDCEL913 can be selected; the CDCEL913 has the same footprint, yet can output 1.8 volts.

Figure 2. CDCE913 Functional Block Diagram

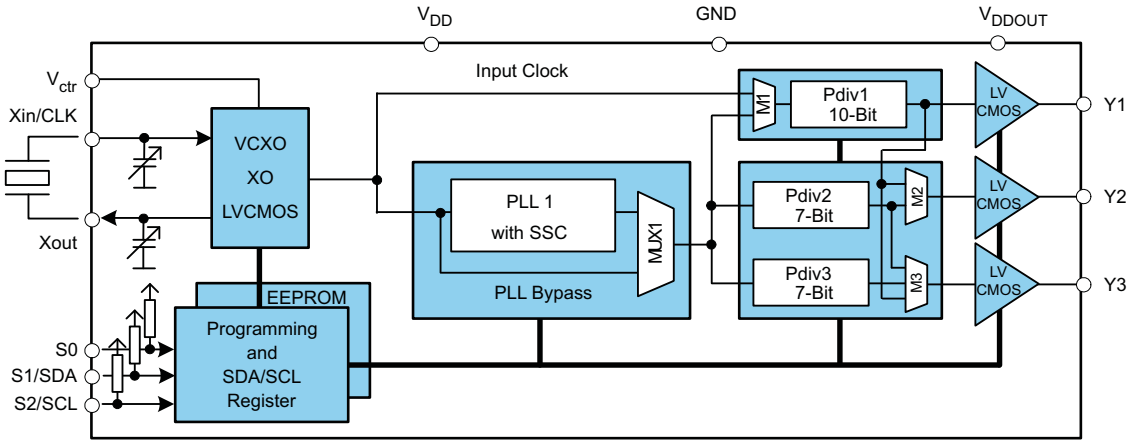
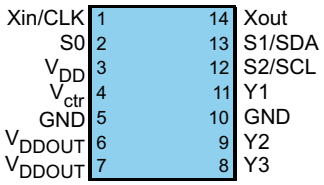


Figure 3. CDCE913 Pin-Out Diagram

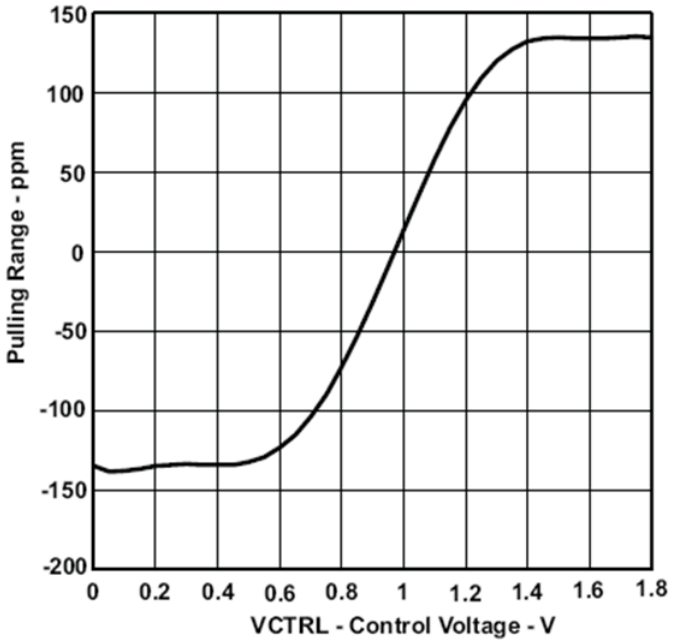


For all detailed specifications, refer the CDCE913 data sheet (SCAS849).

Selecting Crystals for the Application with VCXO Mode

Because the CDCE913 is used in the VCXO mode, an important consideration is the pulling range. Pulling range is the frequency range over which the VCXO can be modulated by sweeping the control voltage. A higher pulling range (Figure 4) ensures smooth locking of the PLL and depends primarily on crystal parameters and PCB layout.

Figure 4. Pulling Range vs. Control Voltage



In order to achieve good pull-ability, the ratio $p = C_0/C_1$ should be less than 220, where C_1 is motional capacitance and C_0 is the shunt capacitance. Having $C_1 > 20$ fF also ensures better performance (pull-ability > 120 ppm). The ESR should be as small as possible to ensure VCXO start-up, and C_0 must be smaller than 6 pF.

TI recommends you place the crystal as close to the CDCE913 IC as possible, to avoid any parasitic effects.

For additional details, see the *VCXO Application Guideline for CDCE(L)9xx Family* TI Application Report, (SCAA085).

Measurement Information

Using the functional block diagram shown in Figure 1, an evaluation module was developed to verify the concept and measure the phase noise/jitter (Figure 5).

Figure 5. Partial EVM Board Schematic

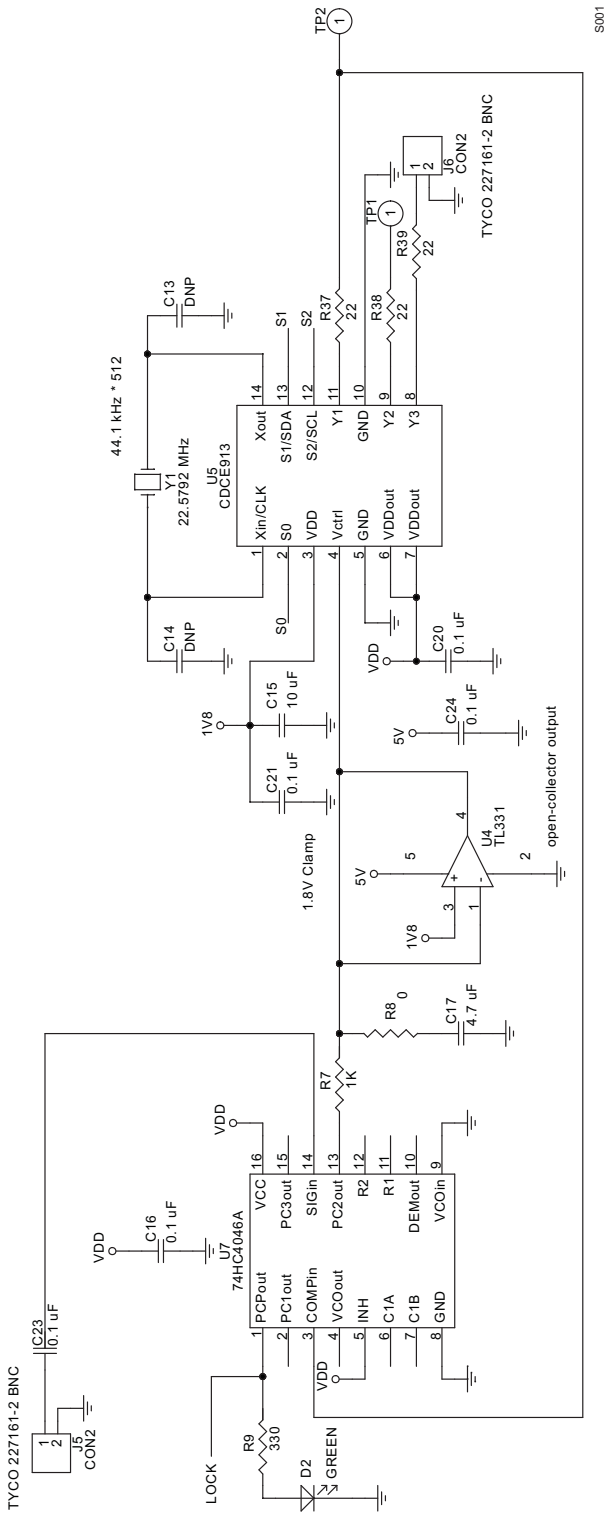
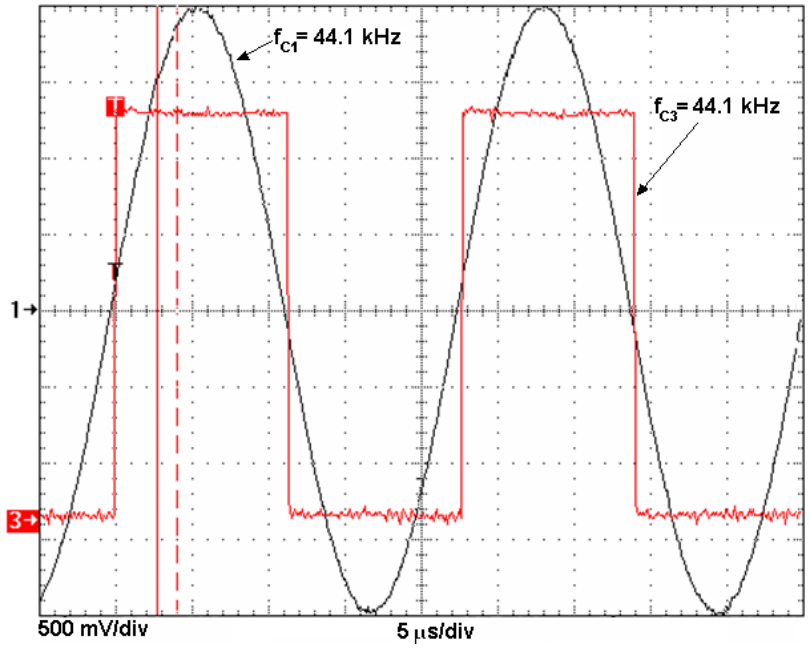


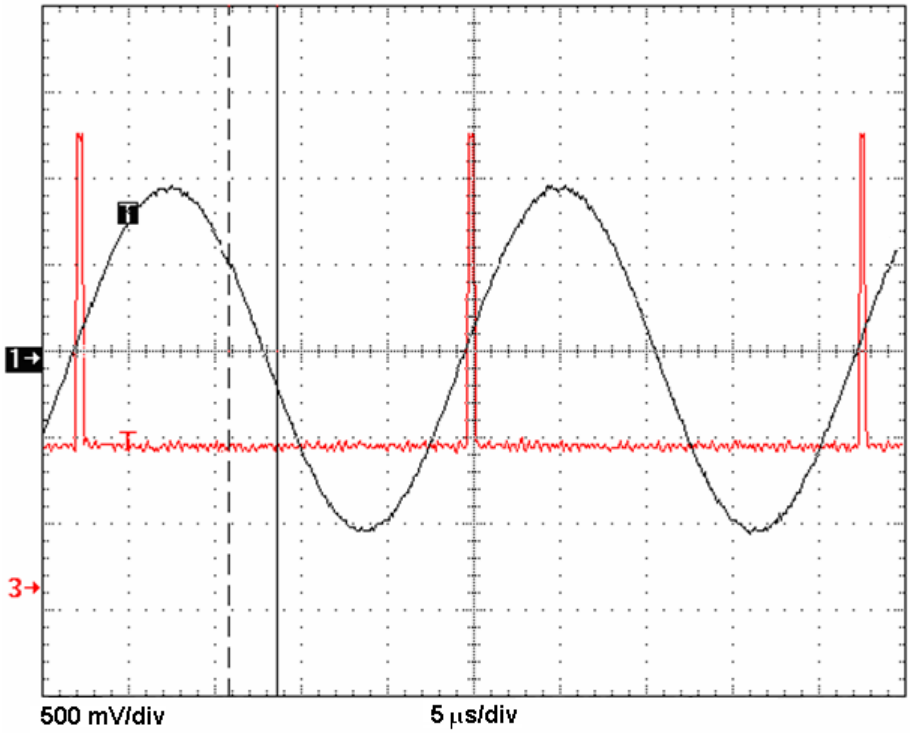
Figure 6. Reference Clock and Feedback Clock at Locked Condition



C1 (Black) – reference clock from signal generator

C3 (Red) – feedback clock from CDCE913 (Y1 output)

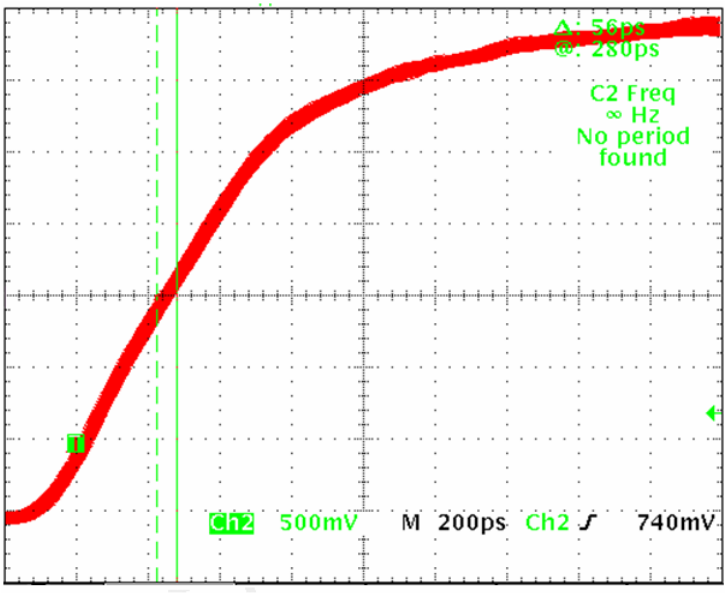
Figure 7. Phase Comparator Output at Locked Condition



C1 (Black) – reference clock from signal generator

C3 (Red) – phase comparator output (at pin 13 of CD74HC4046A)

Figure 8. Infinite Persistence Mode of CDCE913 Output (Y3)



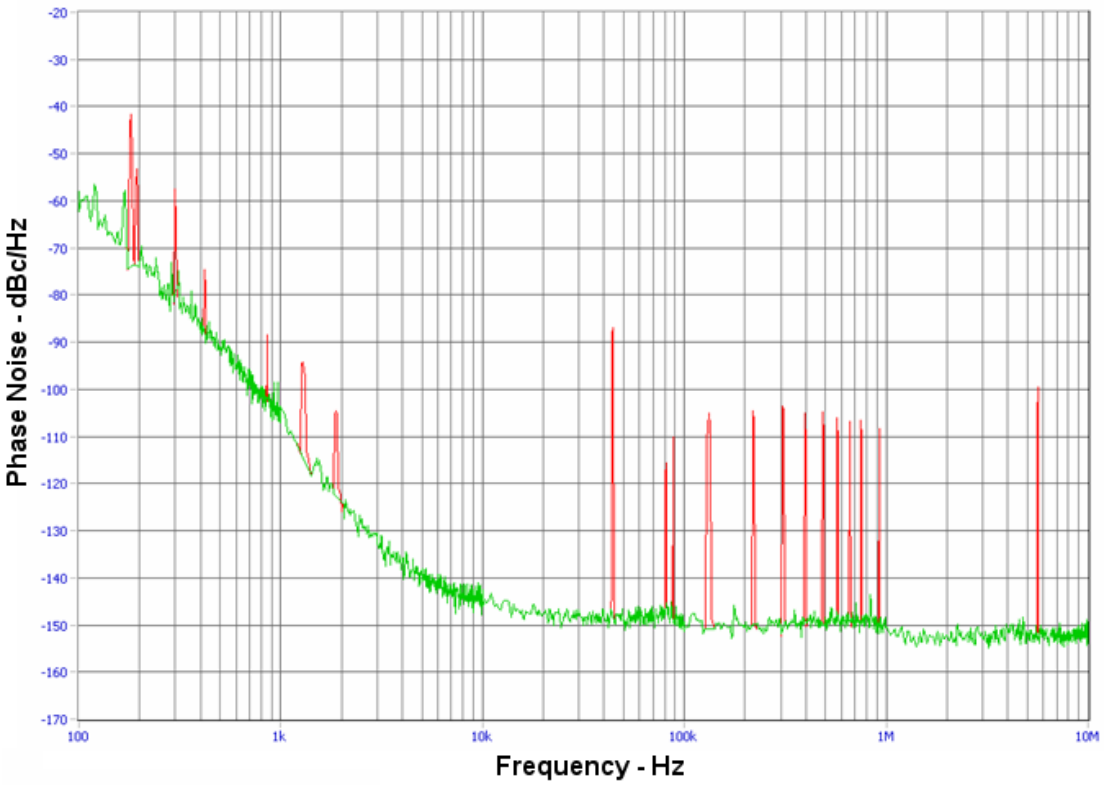
(1) Infinite persistence method used to show jitter accumulation of the audio clock frequency.

Phase Noise and Jitter Measurement of 22.5972 MHz System Clock

Figure 9 and Figure 10 display specifications:

- PLL is locked
- Crystal center frequency = 22.5972 MHz
- Input clock = 44.1 kHz (from signal Generator)

Figure 9. Phase Noise vs. Frequency (From the Carrier)



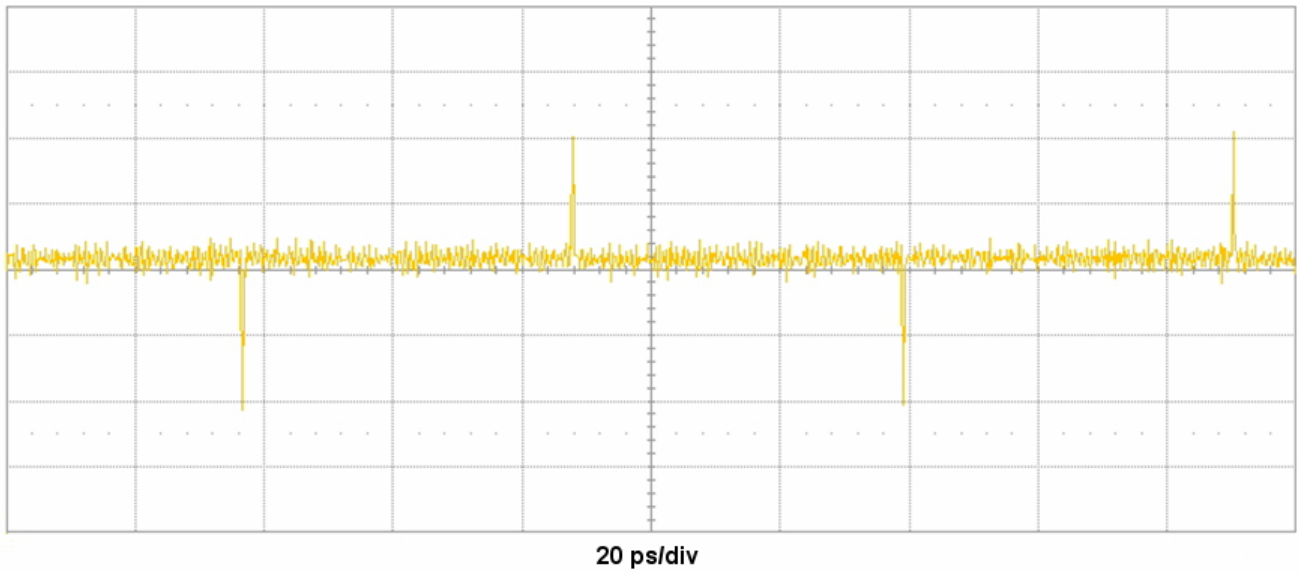
(1) Measurements made with Phase Noise Analyzer PN9000.

(2) The carrier frequency is 22.5792 MHz.

(3) The spike at 44.1 kHz is from the PFD update frequency and the other spikes are its harmonics.

(4) The RMS jitter is 1.32 ps and peak-to-peak jitter is 15.03 ps within the 10 kHz to 10 MHz band

Figure 10. Time Domain Measurement at Locked Condition



Measure	P1:dper@lv(C2)	P2:per@lv(C2)	P3:freq(C2)	P4:pkpk(C2)	P5:pkpk(F1)
value	-4 ps	44.284 ns	22.5814 MHz	250 mV	85 ps
mean	-0 fs	44.28865 ns	22.579146 MHz	250.23 mV	84.53 ps
min	-56 ps	44.240 ns	22.5551 MHz	250 mV	85 ps
max	48 ps	44.336 ns	22.6042 MHz	250 mV	85 ps
sdev	5.36 ps	3.64 ps	1.856 kHz	250 µV	---
num	45.155e+3	45.157e+3	45.157e+3	2	1
status	✔	✔	✔	✔	✔
histo					

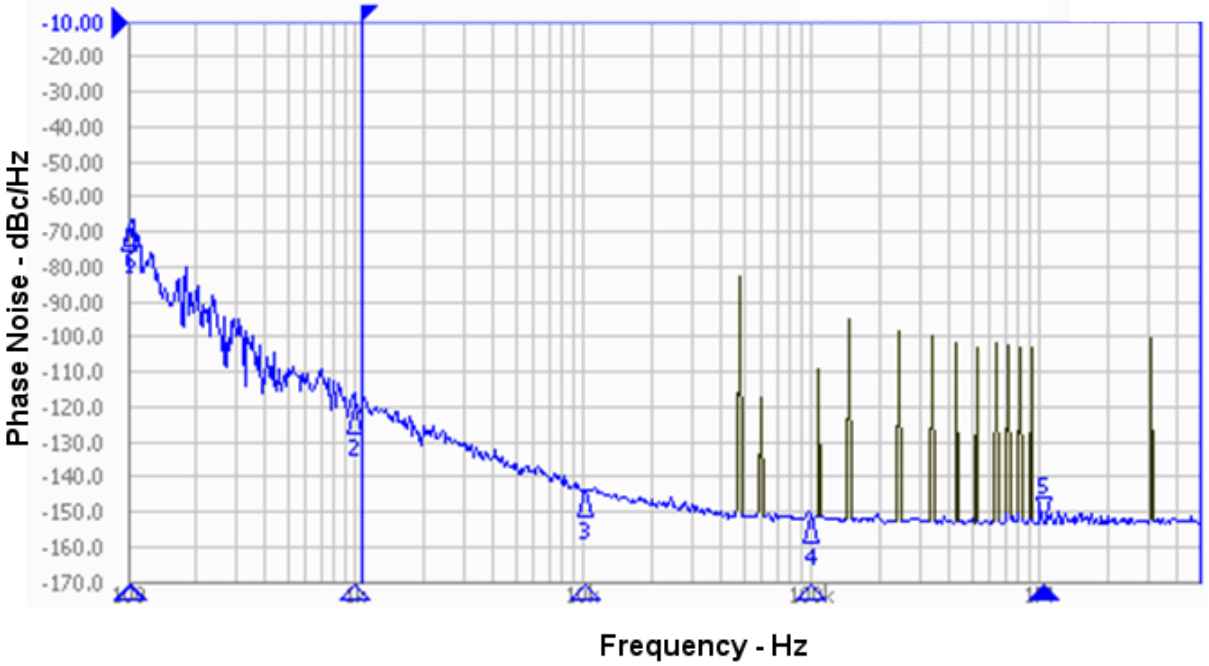
(1) This data shows cycle-to-cycle jitter (second column) and peak-to-peak jitter (sixth column) of period jitter measurement.

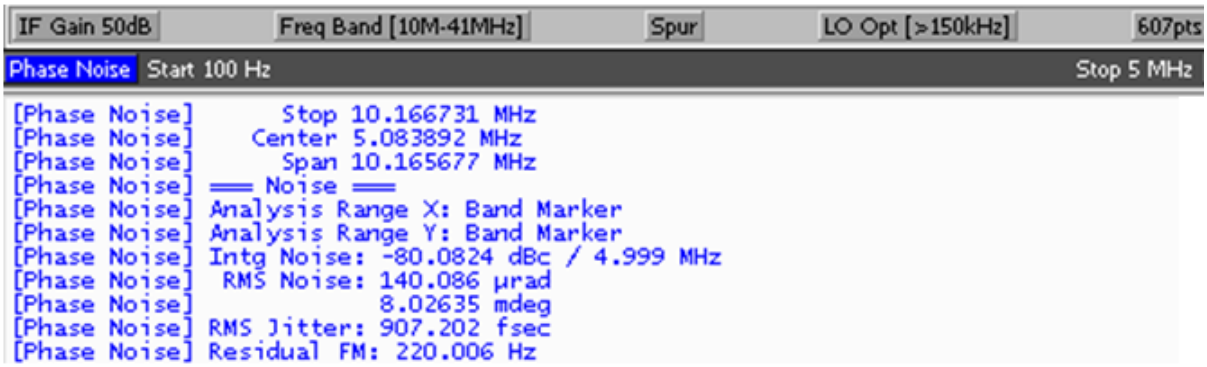
Phase Noise and Jitter Measurement of 24.576 MHz System clock

Figure 11, Figure 12, and Figure 13 display specifications:

- PLL is locked
- Crystal center frequency = 24.576 MHz
- Input clock = 48 kHz (from signal Generator)

Figure 11. Phase Noise vs. Frequency (From the Carrier)

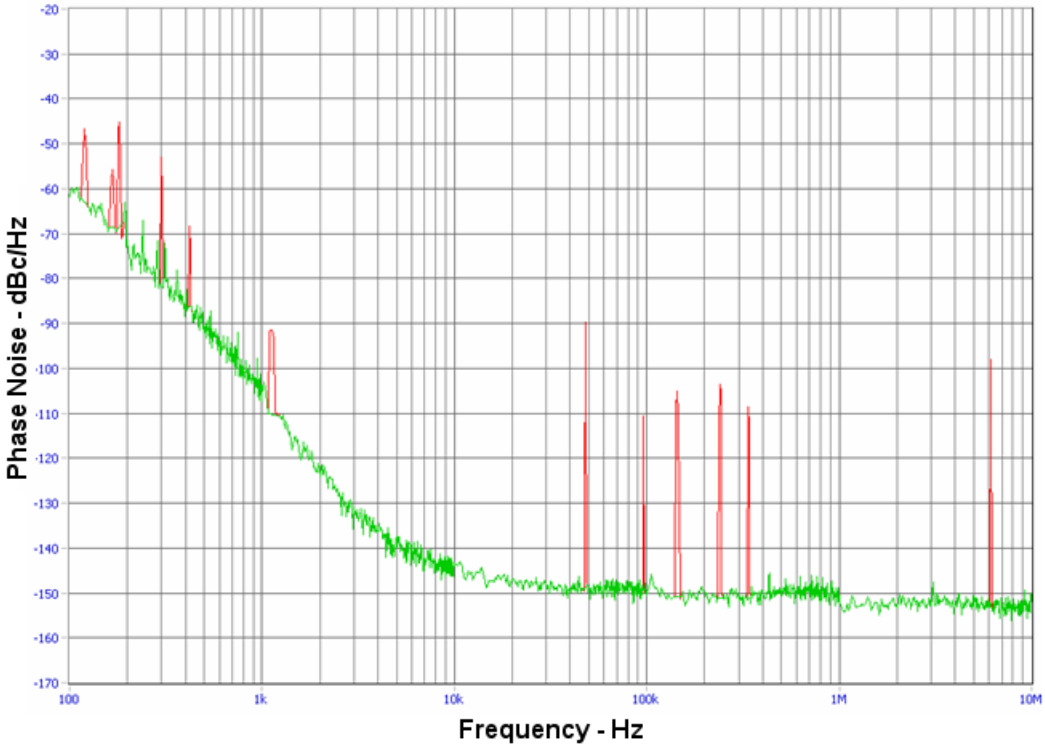




(1) Used an Agilent 5052A Phase Noise Analyzer

(2) This data shows 907 fs RMS jitter within the 1 kHz to 5 MHz band.

Figure 12. Phase Noise vs. Frequency (From the Carrier)



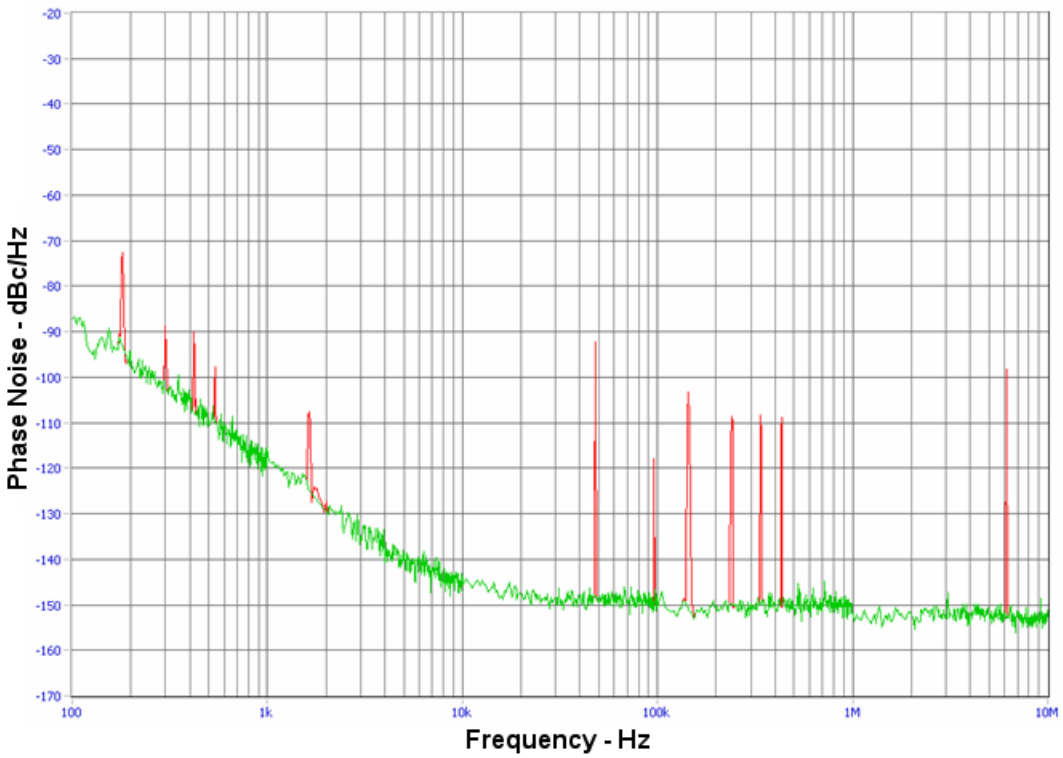
(1) Measurements made with Phase Noise Analyzer PN9000.

(2) The carrier frequency is 24.576 MHz.

(3) The spike at 48 kHz is from the PFD update frequency and the other spikes are its harmonics.

(4) The RMS jitter is 998.88 fs within the 10 kHz to 10 MHz band.

Figure 13. Phase Noise vs. Frequency (From the Carrier)



(1) Measurements made with Phase Noise Analyzer PN9000.

(2) The carrier frequency is 24.576 MHz.

(3) The input clock source is the output clock of another PLL.

(4) The spike at 48 kHz is from the PFD update frequency and the other spikes are its harmonics.

(5) The peak-to-peak jitter is 12.76 ps within the 10 kHz to 10 MHz band.

Generating System Clocks Referenced to 44.1 KHz or 48.0 kHz Word Clocks

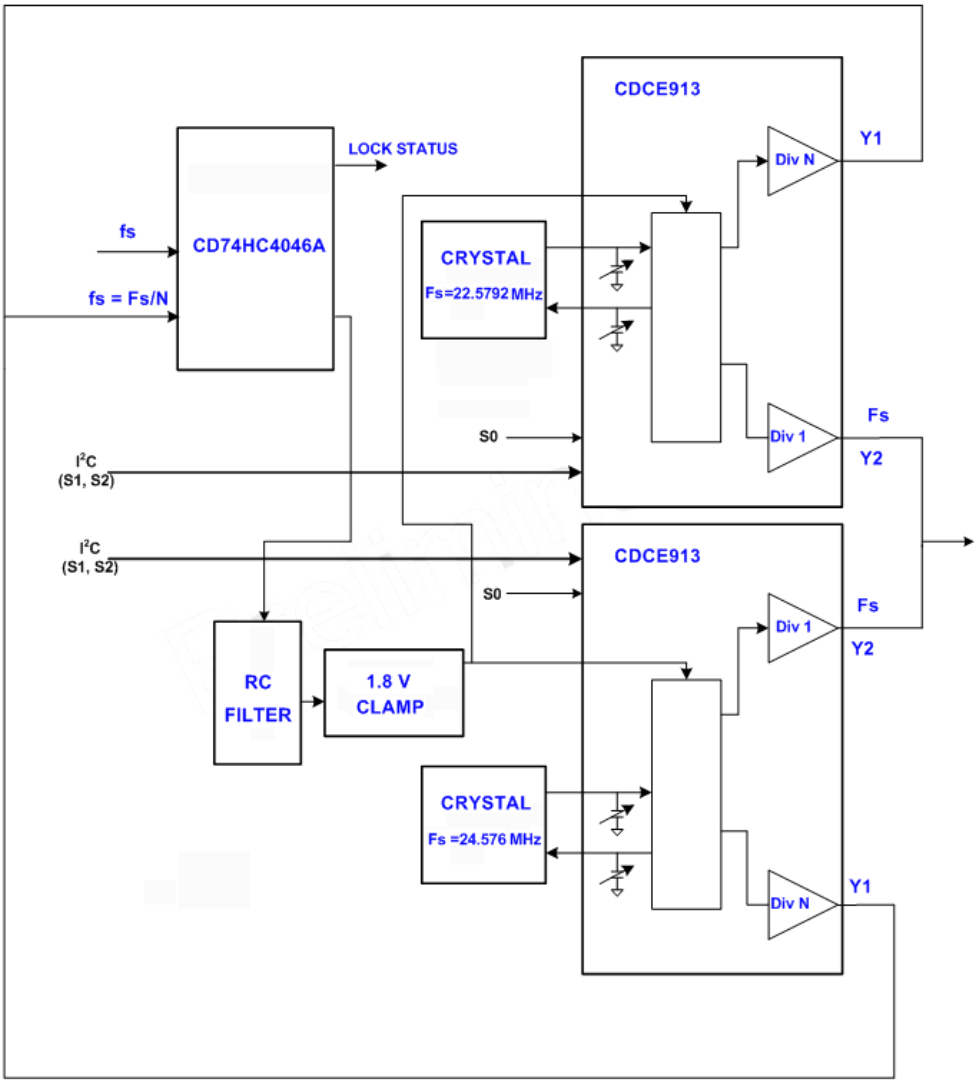
For many audio applications, a 44.1 kHz or 48.0 kHz word clock is available through a common connection. A system clock must be locked to either frequency, but they differ enough that a single crystal can not be pulled far enough to cover both. Using a single CDCE913, only multiples of 44.1 kHz or 48.0 kHz can be generated.

Note: CDCE913 operates in PLL-bypass mode to achieve the best possible jitter performance.

A second CDCE913 device (Figure 14) can be added to Figure 1 so that multiples of 44.1 kHz or 48.0 kHz are synthesized. Each individual CDCE913 has a dedicated crystal for the particular word clock frequency. During operation, only one CDCE913 is active, while the other is powered down through the I^2C bus or control pins. When powered down, the CDCE913 crystal oscillator is disabled and its outputs assume a high-impedance state. This permits the outputs of both CDCE913s to be wired together without device contention. The VCXO control pins are always high-impedance and can also be wired together.

The device's operational mode, active or power down, can be controlled though I^2C or by shared external control pins (S0, S1 and S2). Since the IC pins for these functions are shared, I^2C can not be used simultaneously with the control pins. The S0, S1, and S2 pins functionality is programmable and can be switched between the active and power down modes. S1 and S2 pins are shared with the I^2C bus.

Figure 14. Dual Clocks Generation Block Diagram



Conclusion

Achieving the very best possible performance from today's precision Audio Data converters requires a low-noise, low-jitter system clock. The commonly used PLL circuits typically have too much jitter for multiplying a studio *word clock* to a high frequency system clock. The ultimate in jitter performance is obtained from a crystal oscillator. The CDCE913 provides the amplifier, varactor, prescaler, and buffer elements needed to create a precision VCXO-based PLL. With the addition of an inexpensive, external low-frequency phase detector, multiples of 44.1 kHz or 48.0 kHz can be easily synthesized. If a multiple of 44.1 kHz or 48.0 kHz is required within the same system, a second CDCE913 and its associated crystal can be easily added.

The Phase Noise Plots and jitter measurements indicate that the proposed solution offers a significant improvement in performance over what is otherwise currently available. Though the solution is comprised of a few ICs and passive components, it is very cost effective and capable of generating a high frequency system clock from a low-frequency word clock, while maintaining extremely low phase noise and jitter.

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