Application Report
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Clocking Recommendations for DM6446 Digital Video EVM With Single PLL

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High Speed - Clock Drivers

ABSTRACT

The DM6446 (DaVinci™) Digital Video Evaluation Module (EVM) requires a number of clock frequencies to run the system properly. The current clocking proposal of this EVM consists of a VCXO chip PI6CX100-27W, a PLL chip PLL1705, several voltage level translators, and a few oscillators or crystals. This application report discusses an optimized clocking proposal with Texas Instruments new clock drivers and recommends a more integrated, high-performance, and cost-saving proposal with a minimum number of ICs.

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1 Introduction

The system requires a frequency adjustment capability to synchronize the audio and video clock. The zero-ppm accuracy for video and audio clocks is required. The phase-locked loop (PLL) is also required to generate the audio clock or clocks from the 27-MHz adjusted clock frequency. The 27-MHz adjusted clock is dedicated as a video clock.

Besides the video and audio clocks, either a crystal or an oscillator generates one 27-MHz clock signal for CPLD timer, one 27-MHz signal for system oscillation, one 24-MHz signal for USB, and one 25-MHz Ethernet clock signal.

1.1 Video and Audio Clocks Generation

The current clocking solution in the reference design guide is a multichip-based proposal. The modulated 1.8-V signal (PWM) is converted into a 3.3-V signal, and then this signal is converted into analog control voltage (using an RC filter) before providing the signal to the control input of the VCXO. The VCXO chip PI6CX100-27W receives a PWM signal and adjusts the 27-MHz crystal frequency for the required synchronization.

The PLL chip PLL1705 generates 3.3-V video clock (27 MHz) and audio clock for stereo codec TLV320AIC33 from the 27-MHz synchronized signal.

The voltage level translators (SN74AUC1G125) are used to translate 3.3-V to 1.8-V signals for video and audio clocks.

The PLL1705 multiclock generator can generate audio clock frequencies such as 8.192 MHz, 11.2896 MHz, 12.288 MHz, 16.384 MHz, 16.9344 MHz, 18.432 MHz, 22.5792 MHz, 24.576 MHz, 33.8688 MHz, and 36.864 MHz.

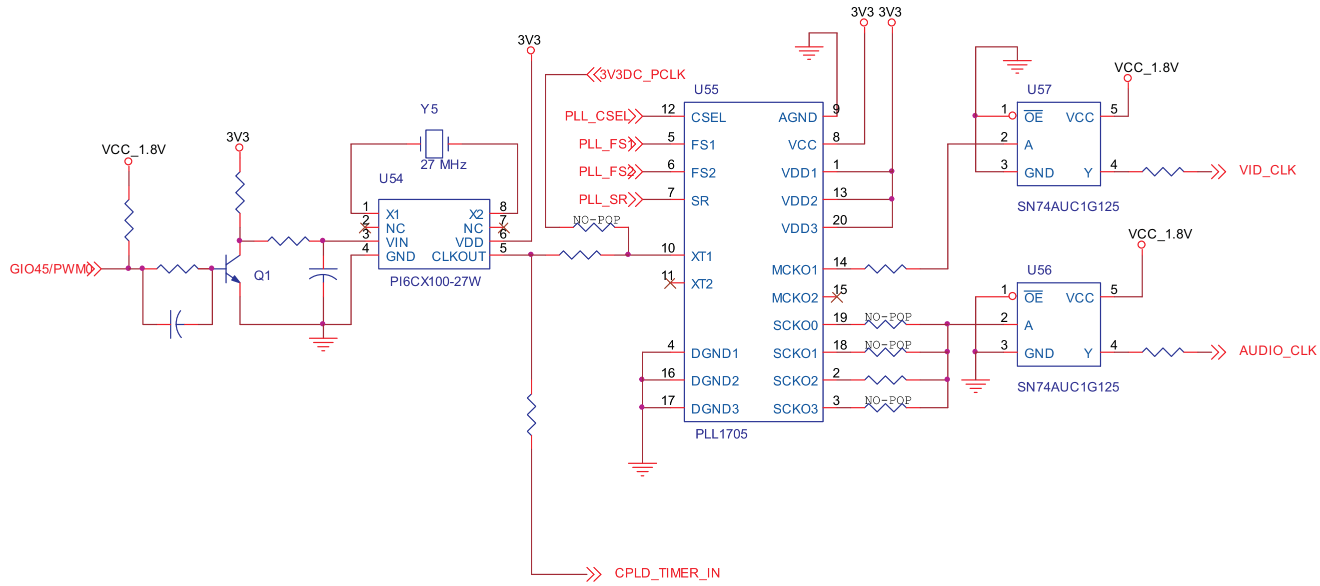

Figure 1. Generating Synchronized Video and Audio Clocks (Current Clocking Proposal With Several ICs)

1.2 Clock Proposal With CDCEL913

The CDCEL913 is a single-PLL-based and the CDCE925 is a two-PLL-based clock synthesizer with VCXO input. The CDCEL925 and the CDCEL913 will be released in the third quarter and fourth quarter of 2007, respectively. CDCE949 is a four-PLL-based device of the same family and is currently available for purchase.

1.3 Single-Chip Solution for Generating Audio and Video Clocks

A single chip is capable of generating the synchronized video and audio clocks for the system.

The CDCEL913 is a single-PLL-based VCXO clock. This PLL can be programmed via the I^2C bus, and all audio frequencies can be generated with 0-ppm error. This device also supports nonvolatile EEPROM, and factory-preprogrammed devices (according to a customer's specification) will be offered to the customers. Using the control pins, one of the several preprogrammed audio frequencies can be selected at the output.

It has three outputs. Two of the outputs (Y1 and Y2) are PLL bypassed and generate a 27-MHz video clock. The Y3 output is from the PLL clock, and it generates an audio clock frequency.

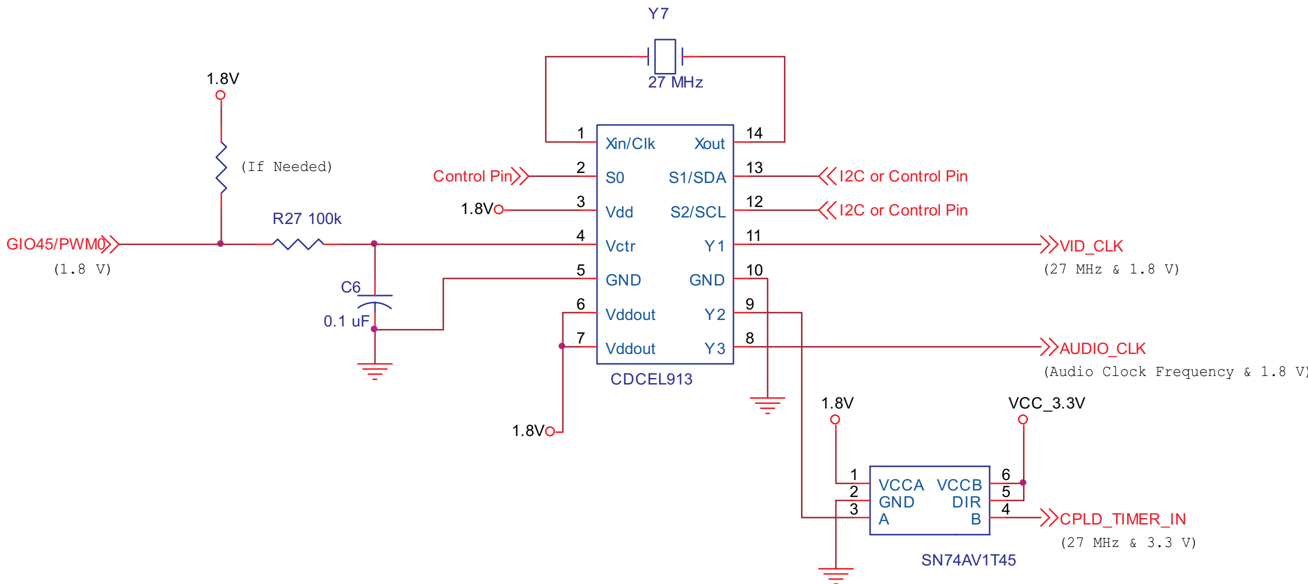

Figure 2. Single-Chip Solution to Generate Synchronized Audio and Video Clock Frequencies

The core supply voltage of the CDCEL913 is 1.8 V. So, a 1.8-V modulation signal can be connected directly to the voltage control pin using the RC filter. This device can generate 1.8-V LVCMOS signal, so that any additional signal translators or buffers are unnecessary for audio and video clocks. Because the core supply voltage is low, it consumes low power compared to 3.3-V devices.

The CPLD_TIMER clock input requires a 3.3-V LVCMOS clock; therefore, an extra voltage level translator (SN74AV1T45) is needed to translate the 1.8-V signal to a 3.3-V signal.

1.4 Two-PLL-Based Clocks Solution to Generate All Required Frequencies

Because three other frequencies (27 MHz, 24 MHz, and 25 MHz) are required and these frequencies must not be synchronized like video and audio clocks, a second PLL CDCE925 can be used with a 27-MHz crystal to generate the rest of the clocks. The jitter performance of the clock driver is good and meets all jitter requirements of DSPs.

If the CPLD_TIMER clock does not need the adjusted clock (like audio and video clock), then one of the outputs of CDCE925 (Y3) can be used to generate a 27-MHz clock. Thus, the requirement for an extra voltage level translator is eliminated.

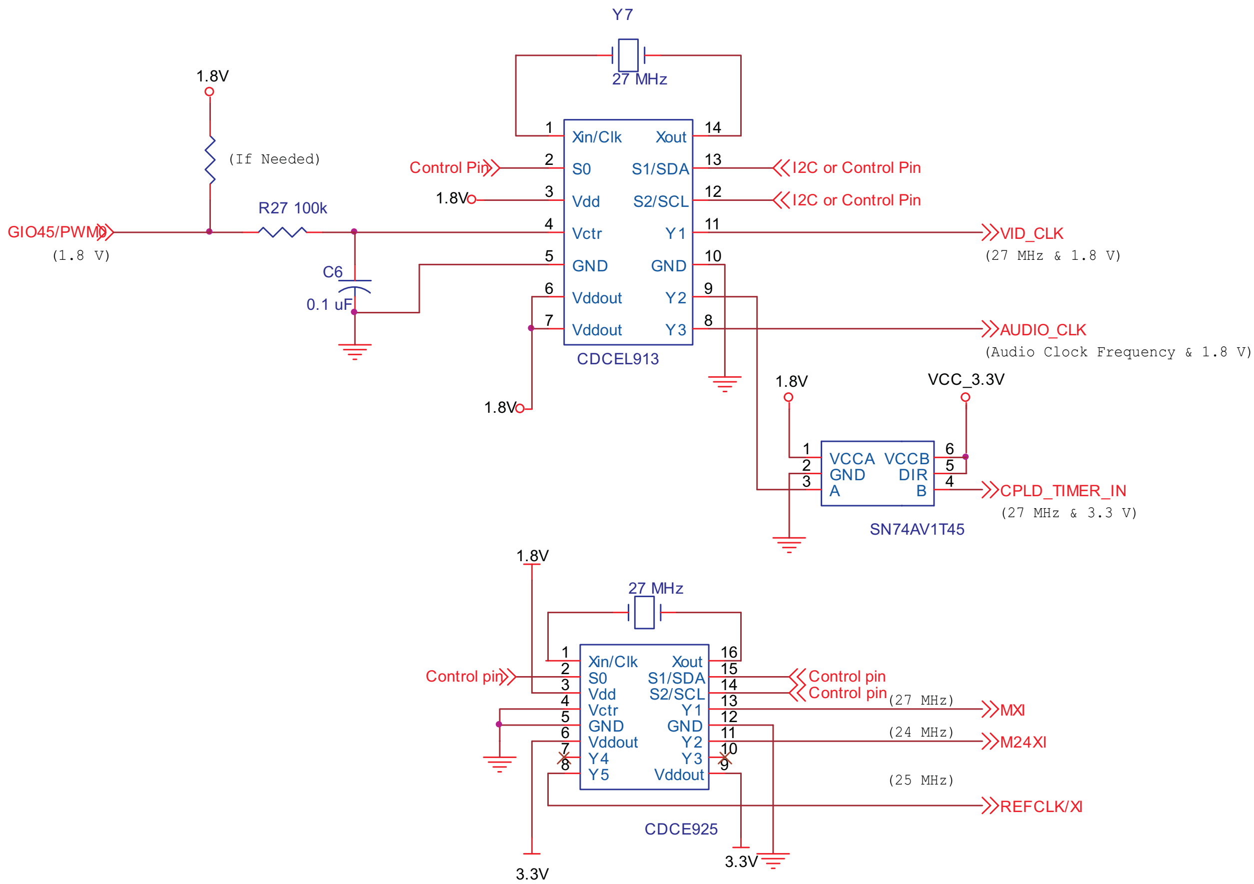

Figure 3. Two-Chip Solution to Generate all Frequencies for this System

Each of the clock outputs (both CDCEL913 and CDCE925) can be enabled or disabled (to LOW or 3-state mode) by using the control pins.

2 Conclusion

The CDCEL913 is offered in a 14-pin TSSOP package. This single, tiny 1.8-V device can replace the functionality of one VCXO chip, one PLL chip, and two voltage level translators to generate synchronized audio and video clocks. Either through a I^{2}C bus or EEPROM, the required frequencies can be generated. This is a simple and cost-saving solution with guaranteed 0-ppm error.

3 References

1. DM6446 (DaVinci™ technology) EVM Information: http://c6000.spectrumdigital.com/davincievm/revd/
2. *CDCE913, CDCEL913, Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V , 2.5-V, and 3.3-V Outputs* data sheet (SCAS849)
3. *CDCE925 , CDCEL925, Programmable 2-PLL VCXO Clock Synthesizer With 1.8-V , 2.5-V, and 3.3-V Outputs* data sheet (SCAS847)