

Recommended Terminations for Differential Inputs of CDCE706/CDCE906

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Clock Drivers

ABSTRACT

This application report describes how differential signals (LVDS, LVPECL, and HSTL) can be connected to CDCE706/CDCE906 differential inputs directly. The wide common-mode voltage and smaller swing required make the devices so versatile that they can receive any differential signal without any complicated coupling and biasing circuits.

1 Introduction

CDCE706/CDCE906 is a three-PLL-based, programmable synthesizer/multiplier/divider with different input clocking options. The CDCE706/906 can accept XTAL input or single-ended or differential input signals. This device can be used as a differential to a single-ended translator with multiplication and division (PLL-based driver) or with division (buffer). The default input selection is XTAL input. The differential inputs can be selected either using SMBus programming or EEPROM. The device has two dedicated supply pins for two banks of the outputs. The output supply voltage can be either 3.3 V or 2.5 V. The outputs also can be inverted. So, different combinations of output buffers are achievable.

1.1 Specifications for Input Clocks

		MIN	NOM	MAX	UNIT
V_{CC}	Device supply voltage	3	3.3	3.6	V
V_{CCOUT1}	Output Y0, Y1 supply voltage	2.3		3.6	V
V_{CCOUT2}	Output Y2, Y3, Y4, Y5 supply voltage	2.3		3.6	V
V_{IL}	Low-level input voltage LVCMOS			$0.3 V_{CC}$	V
V_{IH}	High-level input voltage LVCMOS	$0.7 V_{CC}$			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS		$0.5 V_{CC}$		V
V_I	Input voltage rang LVCMOS	0		3.6	V
$ V_{ID} $	Differential input voltage	0.1			V
V_{IC}	Common-mode for differential input voltage	0.2		$V_{CC} - 0.6$	V
I_{OH}/I_{OL}	Output current (3.3 V)			± 6	mA
	Output current (2.5 V)			± 4	mA
C_L	Output load LVCMOS			25	pF

2 Recommended Differential Input Terminations

The differential input clocks can be connected to CDCE706/906 directly (DC-coupled) with standard termination or with AC-coupling with proper termination and biasing.

2.1 CDCE706/906 With LVDS Clock Driver

Usually, LVDS clock outputs require 100- Ω termination at the receiver end. An LVDS driver provides a minimum 245-mV swing with 1.2-V offset. Both 3.3-V and 2.5-V LVDS drivers can be connected to CDCE706/906 differential input directly.

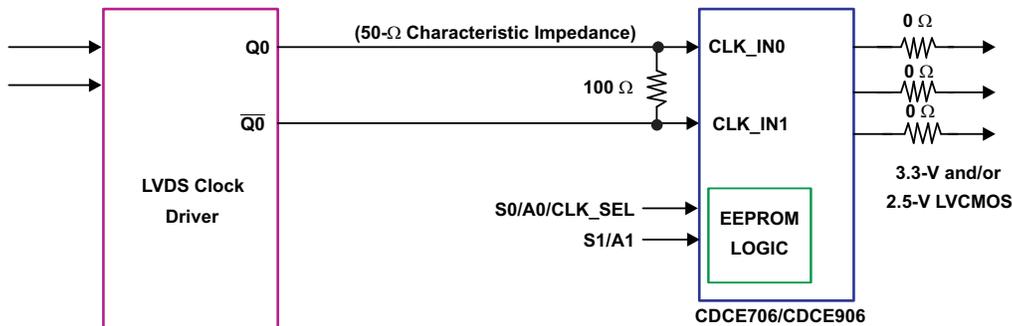


Figure 1. DC-Coupling Between LVDS Driver and CDCE706/906

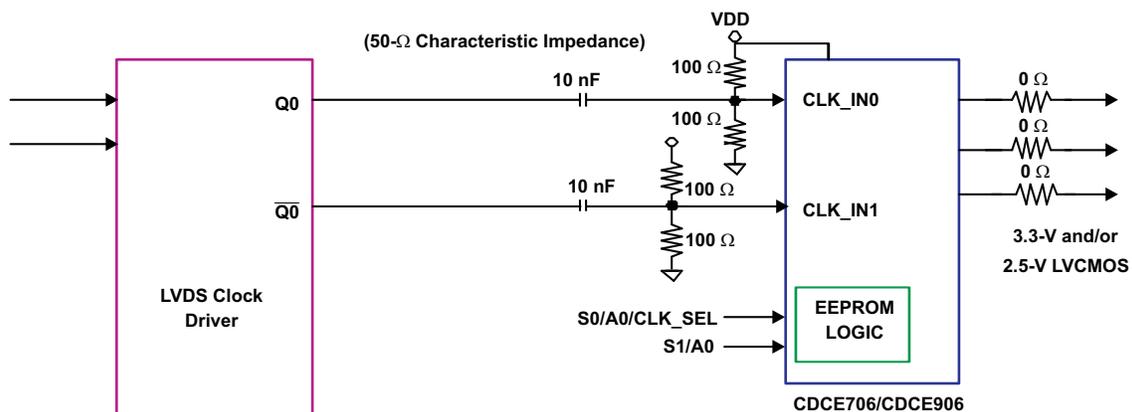


Figure 2. AC-coupling Between LVDS Driver and CDCE706/906

2.2 CDCE706/906 With LVPECL Clock Driver

LVPECL output has open-emitter structure. So, for switching it requires a DC path. The common termination for LVPECL output is 50 Ω to VCC-2 V. Usually, an LVPECL driver provides a minimum 500-mV swing with VCC-1.3-V offset. Both 3.3-V and 2-5 V LVPECL drivers can be connected to CDCE706/CDCE906 directly with DC termination. AC termination is also possible.

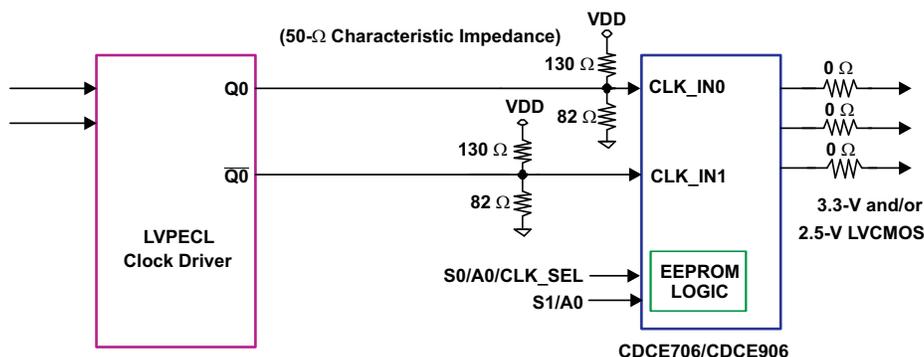


Figure 3. DC-Coupling Between LVPECL Driver and CDCE706/906

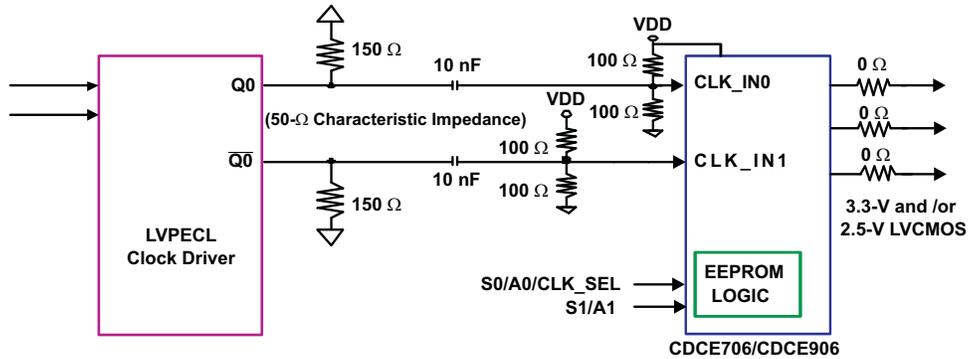


Figure 4. AC-Coupling Between LVPECL Driver and CDCE706/906

2.3 CDCE706/906 With HSTL Clock Driver

An HSTL driver provides a minimum 400-mV swing with 0.75-V offset. So, HSTL outputs can be connected to CDCE706/CDCE906 inputs directly.

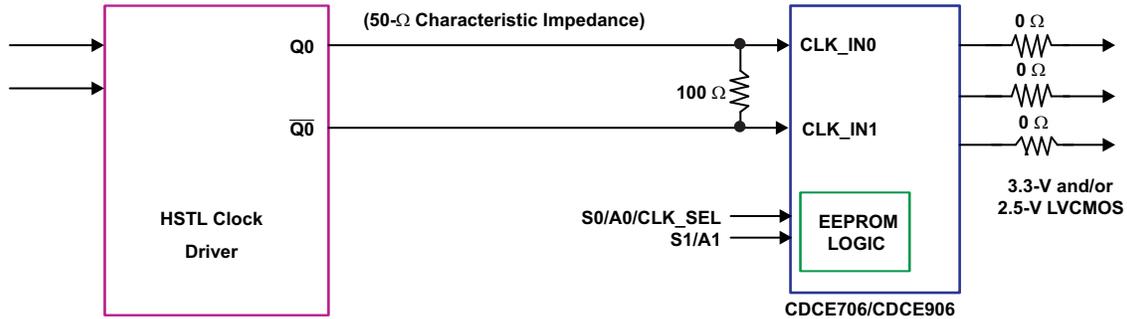


Figure 5. DC Coupling Between HSTL Driver and CDCE706/906

3 Output Jitter Impact With Differential Clock Inputs

The output jitter of CDCE/CDCE906 is low. The typical period jitter is 60 ps. The jitter performance remains same with differential clock inputs as well as single ended input (assuming both differential and single ended inputs have same jitter characteristics)

4 Inverted Outputs From CDCE706/CDCE906

Each of the six outputs can be individually inverted. So, three pseudo-differential pairs can be generated out of six outputs. As there is a slight mismatch between the rise and fall times, the cross-point does not occur at the middle.

5 Conclusion

As CDCE706/CDCE906 accepts a wide range of common-mode voltages (0.2 V – 2.6 V) and differential inputs can work with only a 100-mV swing, these devices can be an excellent differential to single-ended translators with or without using the PLLs.

5.1 References

1. CDCE706, Programmable 3-PLL Clock Synthesizer/ Multiplier/ Divider data sheet ([SCAS815](#))
2. CDCE906, Programmable 3-PLL Clock Synthesizer/ Multiplier/ Divider data sheet ([SCAS814](#))

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