DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM

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ABSTRACT

This report describes various methods of interfacing different logic levels. The focus is dc-coupling between the following differential signaling: LVPECL (low-voltage positive-referenced emitter coupled logic), LVDS (low-voltage differential signals), HSTL (high-speed transceiver logic), and CML (current-mode logic). The report discusses sixteen various interface cases between the aforementioned differential signaling levels.

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1 AC-Coupling

DC-coupling is used in a system when there is a need for a wide bandwidth, or when dc-unbalanced code is used. Both interfaces must have the same ground potential on the same board or system. DC-coupling directly connects the components together without any coupling capacitors. Among the advantages of dc-coupling are: simple board design, no dc-wander issues, and it is useful in all coded-data streams including SONET and NRZ data applications. One disadvantage of dc-coupling is that it requires careful power supply design. Figure1, Table 1, and Table 2 provide the I/O levels for these differential signals.

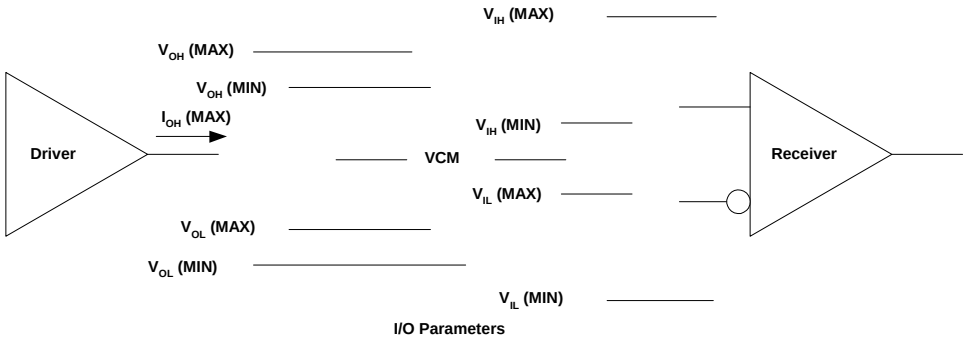


Figure 1. Input and Output Parameters

Table 1. Typical LVPECL, LVDS, HSTL, and CML Outputs

Output	LVPECL	LVDS	HSTL	CML
V_{OH} (Min)	2.275 V	1.249	VDDQ[1] - 0.4	V_{CC}[2]
V_{OL} (Max)	1.68 V	1.252	0.4	V_{CC} - 0.4 V

Table 2. Typical LVPECL, LVDS, CML, and HSTL Input Levels

Input	LVPECL	LVDS	HSTL	CML
V_{IH} (Min)	2.135 V	1.249	VRef + 0.2	V_{CC}
VRef or VCM	2	1.2	0.75	V_{CC} - 0.2 V
V_{IL} (Max)	1.825 V	1.252	VRef -0.2	V_{CC} - 0.4 V
V_{ID} (Min)	310 mV	200 mV	400 mV	400 mV

[1] VDDQ = 1.5 V ±10%
[2] V_{CC} = 3.3 V ±10%

Table 3. Interface Table

		TO			
		LVPECL	**LVDS**	**CML**	**HSTL**
FROM	**LVPECL**	See Figure 3	See Figure 4 or Figure 5	See Figure 6 or Figure 7	See Figure 8
	LVDS	See Figure 9 or Figure 10	See Figure 11 or Figure 12	See Figure 13	See Figure 14
	CML	See Figure 15	See Figure 16 or	See Figure 17	See Figure 18
	HSTL	See Figure 19	See Figure 20	See Figure 21	See Figure 22

1.1 LVPECL

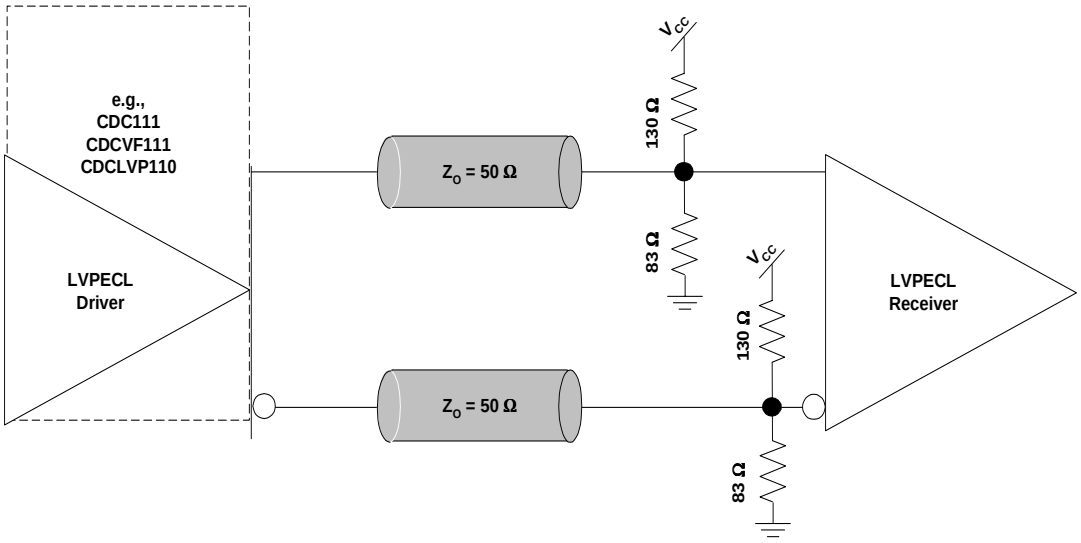


Figure 2. LVPECL to LVPECL

PECL and LVPECL are normally terminated though 50 Ω to (V_{CC} - 2 V). Most systems normally do not have dual power supplies of both 3.3 V and 1.3 V; therefore Figures 2 and Figure 3 show alternative methods to terminate LVPECL output signals. The pullup and pulldown combination terminates the 50-Ω transmission line and establish the LVPECL common-mode voltage of 2 V at the receiver.

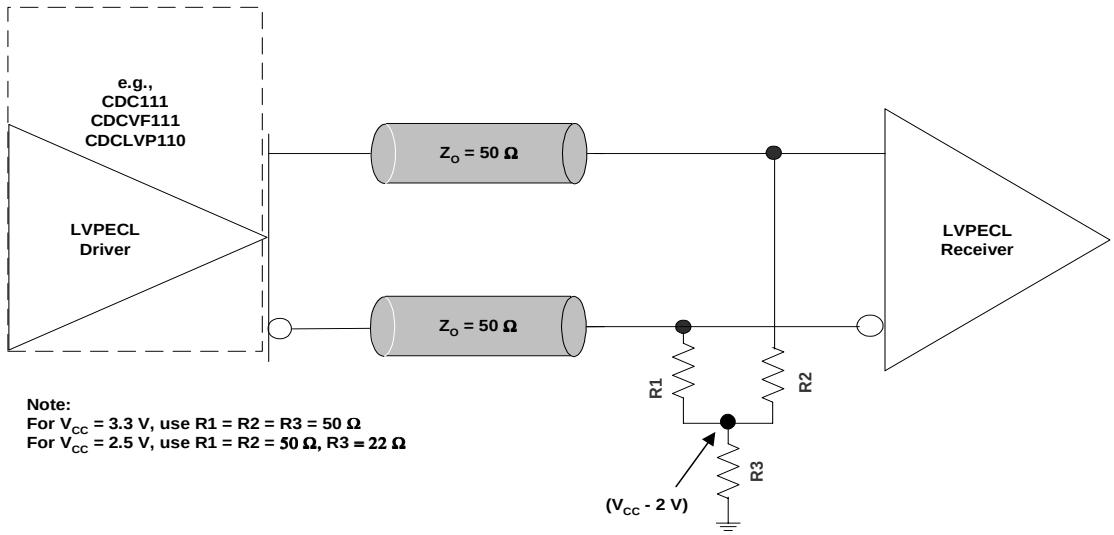


Figure 3. LVPECL to LVPECL

The Y-termination in Figure 3 is another alternative to LVPECL termination where a VTT supply is not readily available. This scheme saves one resistor over the scheme in Figure 2.

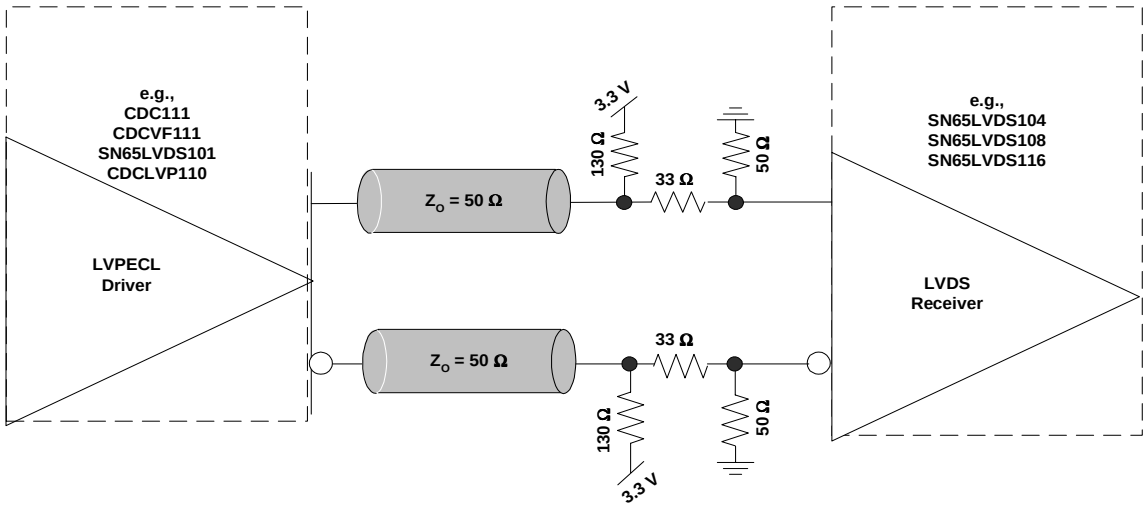


Figure 4. LVPECL to LVDS

The 33-Ω resistor is usually required when the LVPECL output is too high for the LVDS receiver input stage. For the LVDS receivers listed above, it is not required and Figure 5 is recommended.

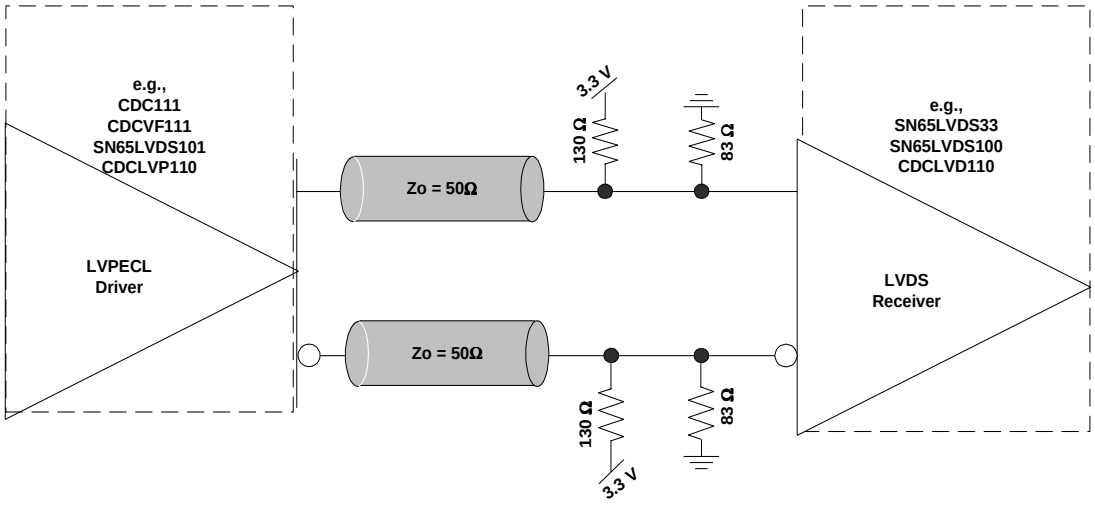


Figure 5. LVPECL to LVDS

Most LVDS receivers are capable of accepting LVPECL signals and it is not necessary to attenuate the LVPECL signal prior to the LVDS receiver. This is due to the wide common-mode range of the LVDS receivers listed above.

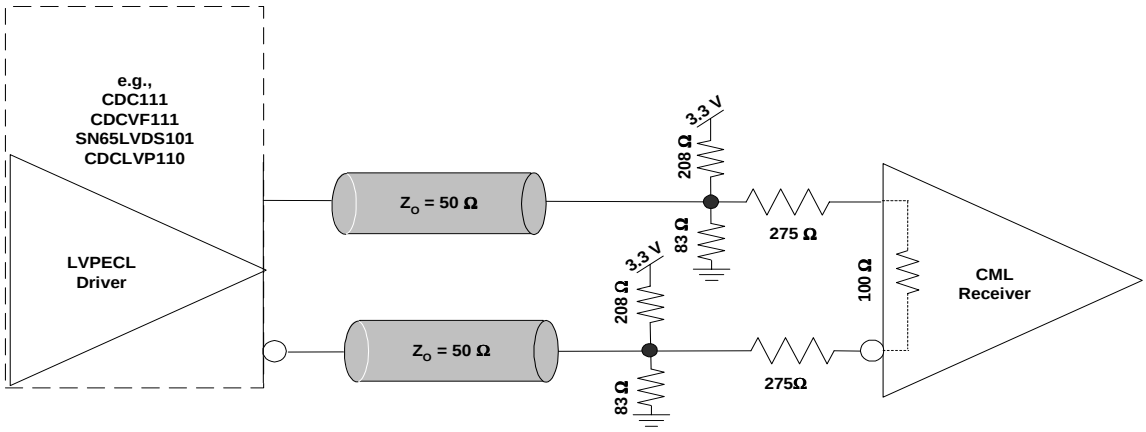


Figure 6. LVPECL to CML

The most widely used method of translating from LVPECL to CML is through ac-coupling. AC-coupling is recommended for dc-balanced signals. AC-coupling generates base-line wander in high-speed serial data transmission such as SONET and NRZ encoded data (non dc-balanced). Therefore, dc-coupling is recommended for such data streams. For detailed derivation, see the SCAA056.

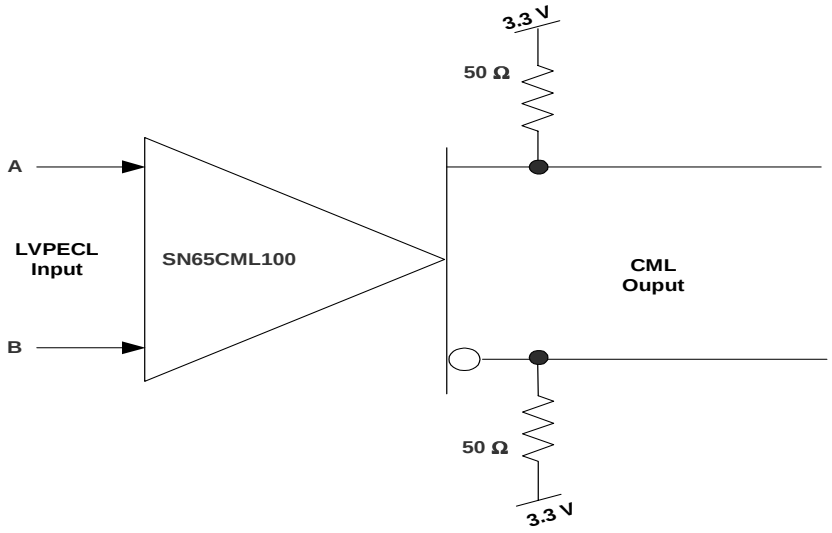
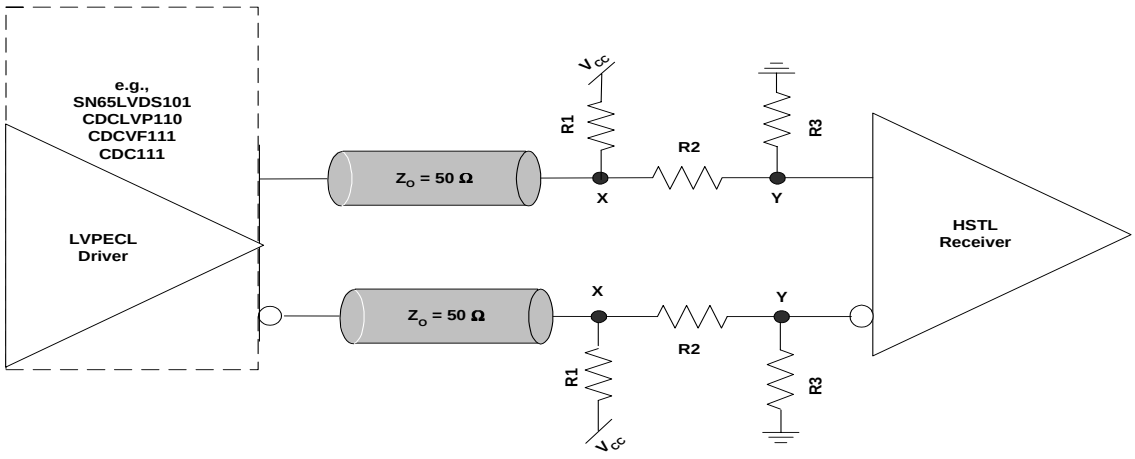


Figure 7. LVPECL to CML Converter

The SN65CML100, in Figure 7, can be used as an LVPECL to CML converter. The 50-Ω pullup resistors are required to bias the SN65CML100 outputs as well as terminate the transmission line. In most cases, the two 50-Ω resistors are included in the CML receiver input stage and therefore are not required.



Note:
For V_{CC} = 3.3 V, use R1 = 127 Ω, R2 = 35 Ω, R3 = 48 Ω
For V_{CC} = 2.5 V, use R1 = 100 Ω, R2 = 40 Ω, R3 = 60 Ω

Figure 8. LVPECL to HSTL

1.2 LVDS

The resistors R1 in parallel with (R2+R3) should match the characteristic impedance (Z_O = 50 Ω) of the transmission line. At point Y in Figure 8, the ratio of R3 to the sum of (R1+R2+R3) should be chosen to set the HSTL common-mode voltage (VCM = 0.75 V). At point X, the LVPECL common-mode voltage is 2 V, which is the voltage across R1 compared to the sum of all three resistors (R1+ R2+R3).

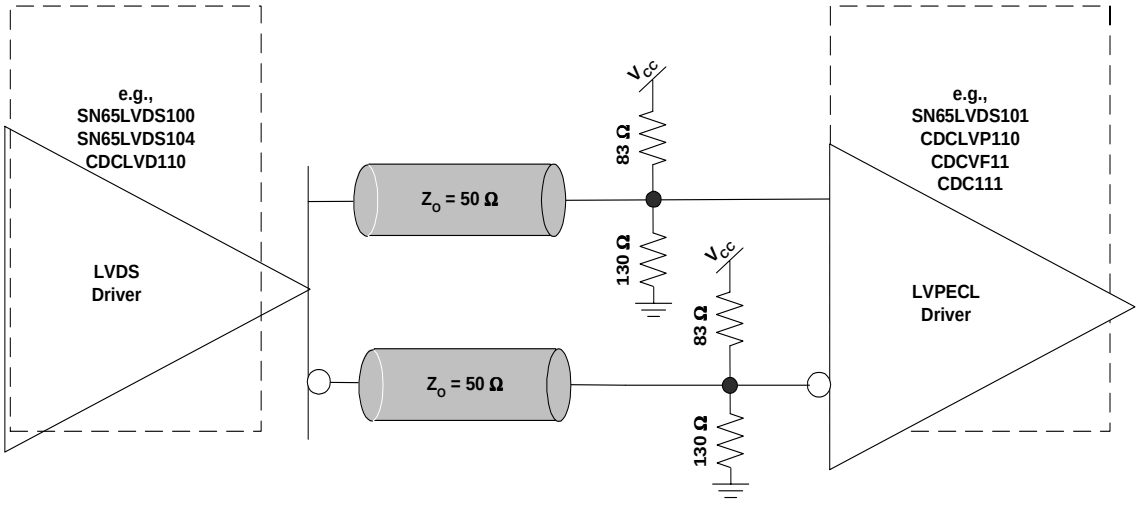


Figure 9. LVDS to LVPECL

The Thevenin equivalent of the 83 Ω and 130 Ω, in Figure 9, matches the 50-Ω transmission line impedance as well as sets the common-mode voltage (VCM = 2 V) for the LVPECL receiver.

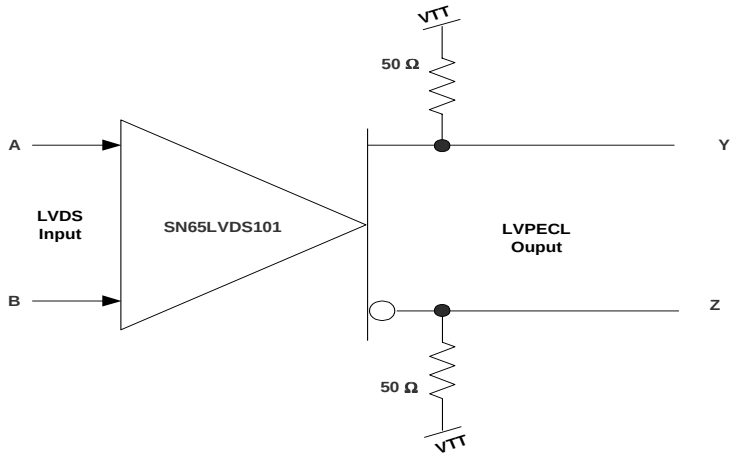


Figure 10. LVDS to LVPECL

The SN65LVDS101, in Figure 10, can be used as an LVDS to LVPECL converter. The 50-Ω pullup resistors are required to bias and terminate the LVPECL outputs to VTT (V_{CC} – 2 V). If the termination voltage, VTT is not available then, the Thevenin equivalent of the 83 Ω and 130Ω, as in Figure 9 is recommended.

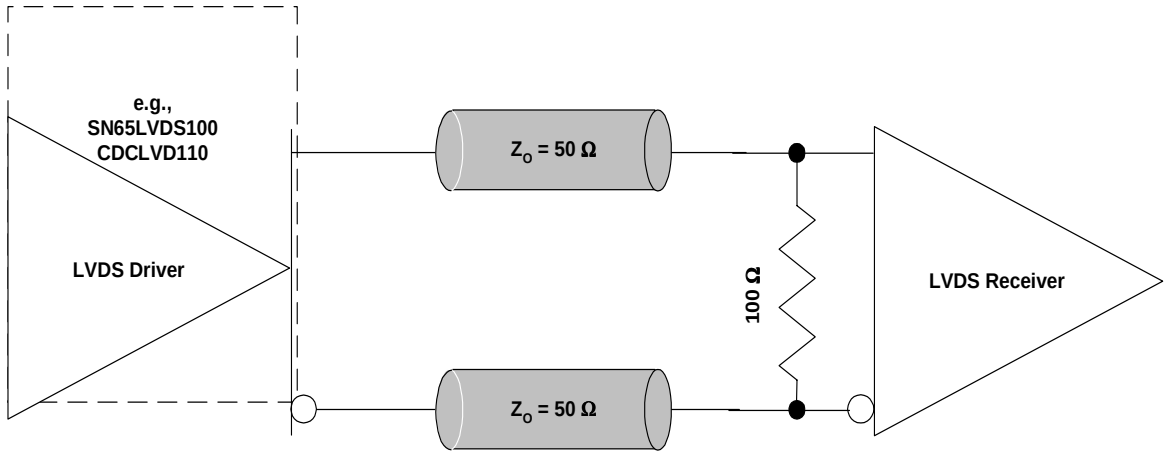


Figure 11. LVDS to LVDS Without On-Chip Termination

Figure 11 is the most commonly used termination for LVDS signals. The 100-Ω external resistor terminates the differential impedance of the transmission line assuming the LVDS receiver does not include an on-chip termination. The designer could also replace the 100-Ω termination with two 50-Ω resistors and tie the mid-point with a capacitor (10 nF) to GND in order to terminate any unbalanced noise within the differential transmission line as well as correct for line-length mismatches.

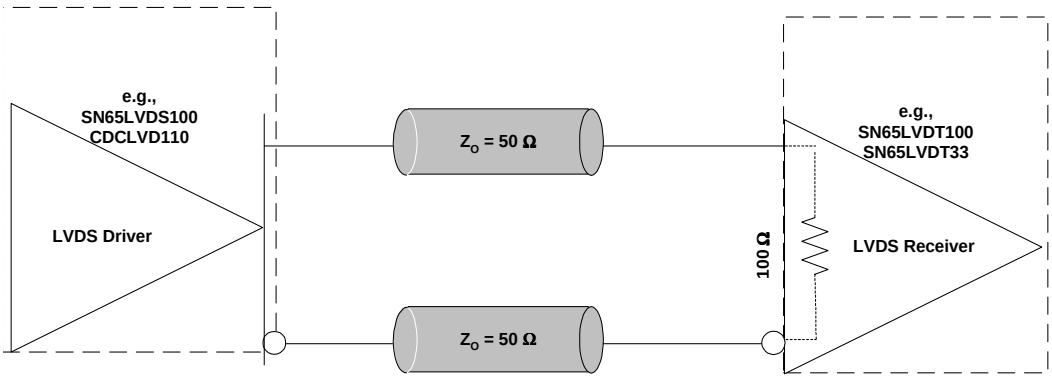


Figure 12. LVDS to LVDS With On-Chip Termination

In Figure 12, the LVDS receiver includes a 100-Ω on-chip resistor; therefore no external termination is needed.

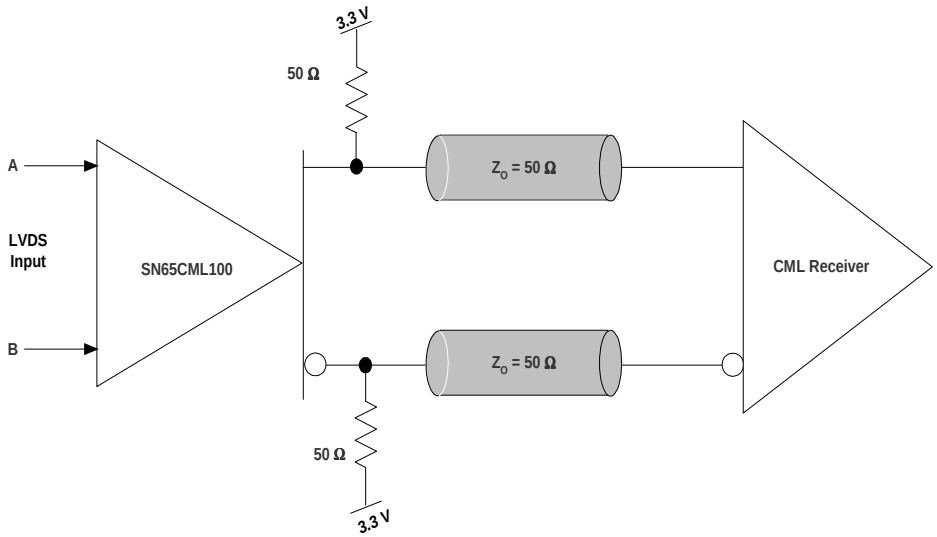
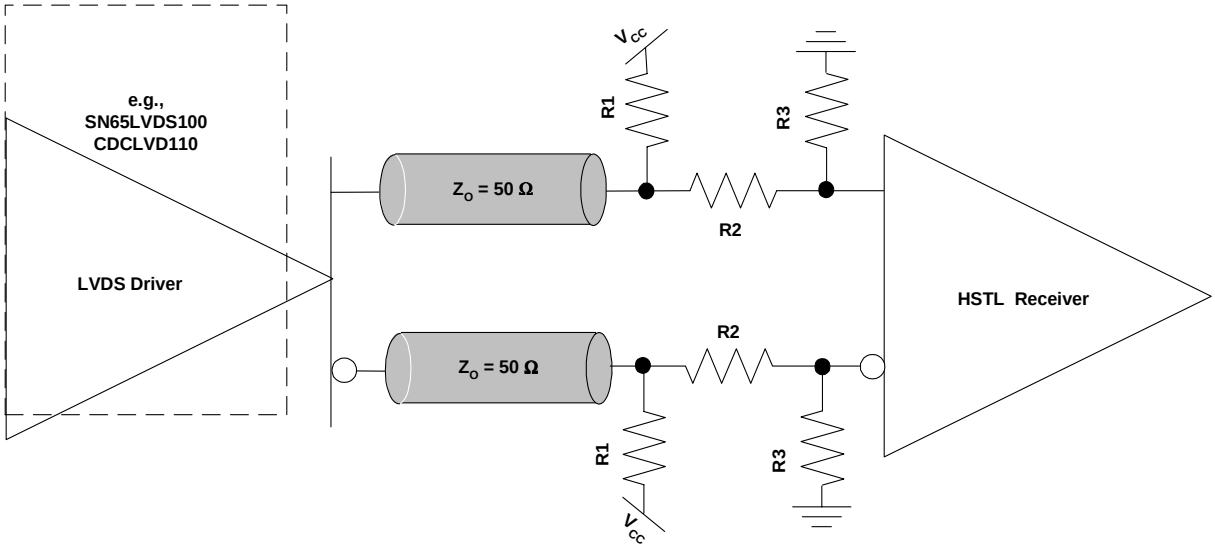


Figure 13. LVDS to CML Converter

Most CML receivers have 50 Ω included on their input stage and external termination is not required. The 50-Ω pullup resistors are required to bias the SN65CML100 and termination the transmission line.



Note:
For V_{CC} = 3.3 V, use R1 = 140 Ω, R2 = 30 Ω , R3 = 50 Ω
For V_{CC} = 2.5 V, use R1 = 100 Ω, R2 = 36 Ω , R3 = 60 Ω

Figure 14. LVDS to HSTL

At the output of the LVDS driver, the ratio of (R2+R3) to the sum of all three resistors (R1+R2+R3) is the same ratio of VCM = 1.2 V to V_{CC}. The ratio of R3 to the sum (R1+R2+R3) must be equal to the ratio 0.75: V_{CC}. Furthermore; R1// (R2+R3) should match the transmission line impedance, Z_O = 50 Ω. Solving these equations result in the values as in Figure 14 for V_{CC} of 3.3 and 2.5 respectively.

1.3 CML

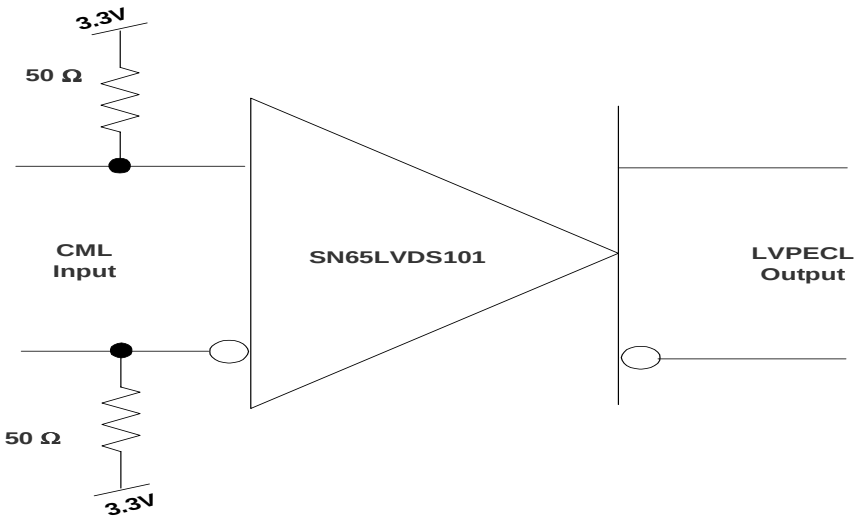


Figure 15. CML to LVPECL Translator

Commonly, ac-coupling is recommended when driving LVPECL with CML. The SN65LVDS101 has a wide common-mode range and can accept CML while providing an LVPECL output.

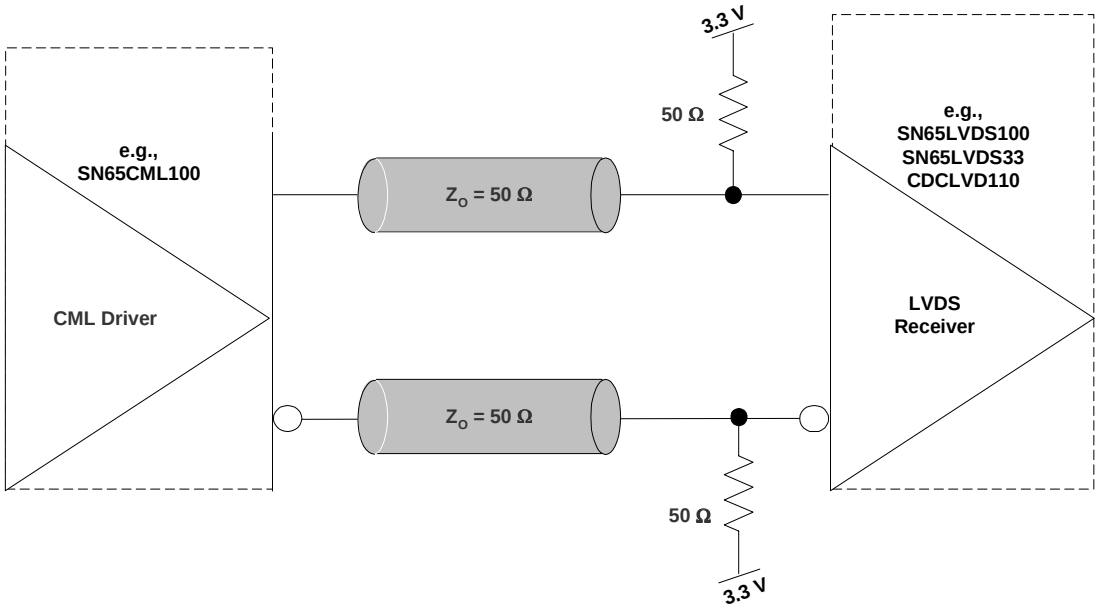


Figure 16. CML to LVDS

Generally, ac-coupling is recommended when driving LVDS receiver with CML. If the LVDS receiver has a wide common-mode range that can accept a CML input (common-mode range must go to V_{CC} rail), then a dc-coupled connection is a direct connection. The 50-Ω pullup resistors are required to bias the SN65CML100 and terminate the transmission line.

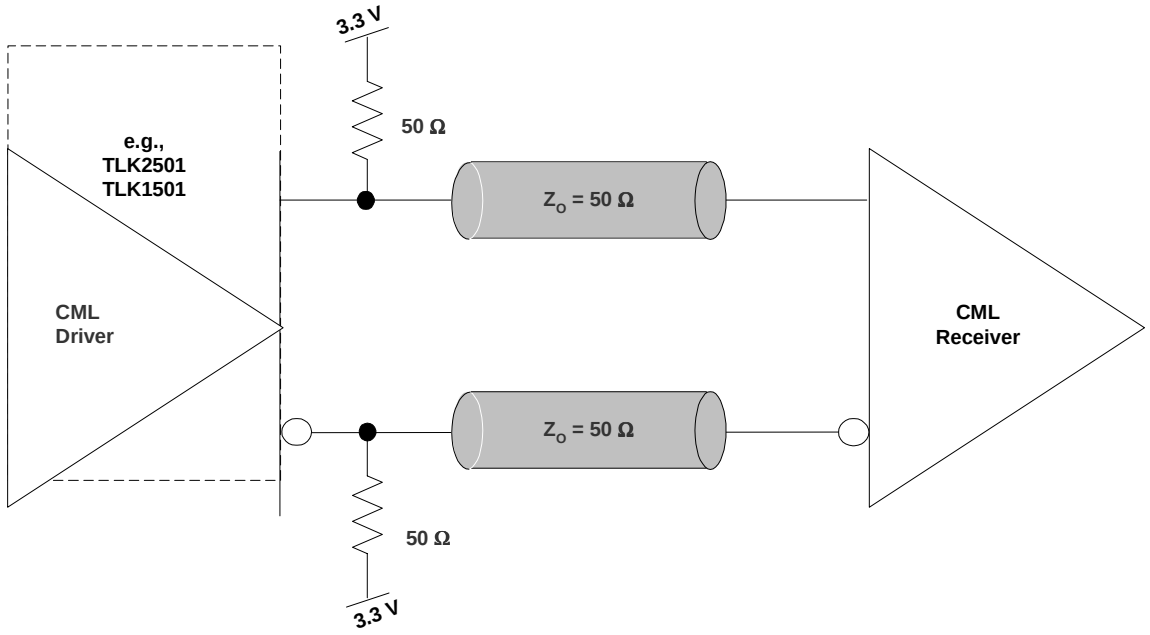
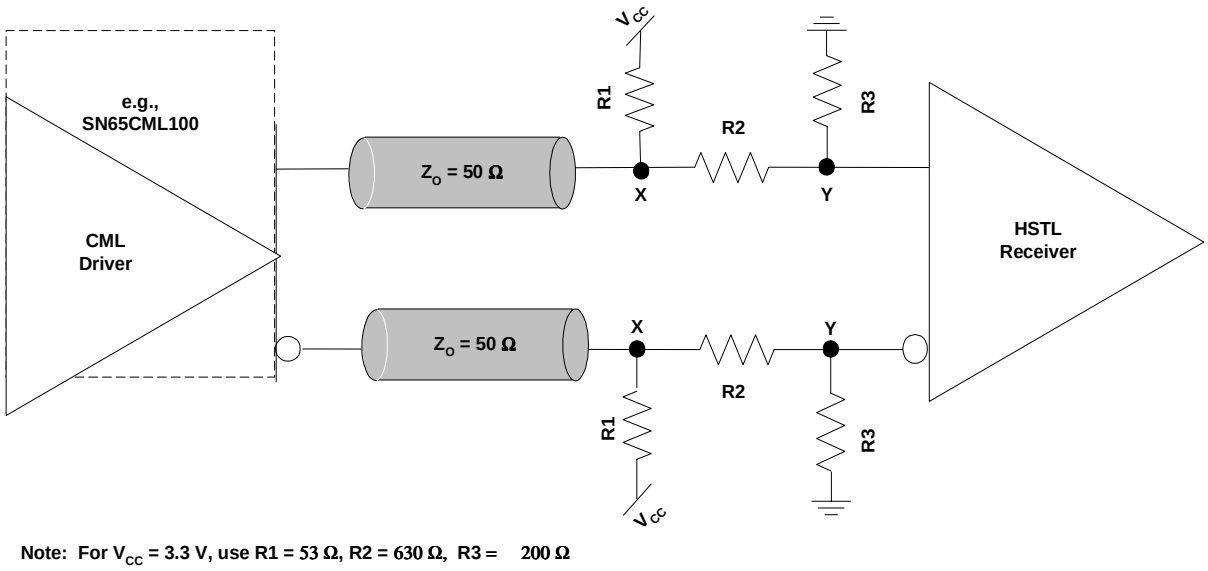


Figure 17. CML to CML

If both the CML driver and receiver have the same V_{CC} supply voltage and on-chip pullup resistors, then a direct connection can be made without external components. If the output stage does not provide an internal 50-Ω pullup resistor (TLK1501), then 50-Ω pullup resistors are required at the transmitter output or at the receiver input. The 50-Ω pullup resistors (see Figure 17) could also be moved to the receive end instead. In addition to the 50-Ω pullup at the source, a 100-Ω line end termination could be implemented at the receiver to terminate the line-impedance at both ends of the link.



Note: For V_{CC} = 3.3 V, use R1 = 53 Ω, R2 = 630 Ω, R3 = 200 Ω

Figure 18. CML to HSTL

In Figure 18, the resistor network R1, R2, and R3 provides proper termination. The network also provides level shifting from CML to HSTL. Using the I/O tables, the following equations are used to solve for R1, R2, and R3. First, (R2+R3)/(R1+R2+R3) = 3.1/3.3. Second, R3/(R1+R2+R3) = 0.75/3.3. Finally, R1||(R2+R3) = Z0 = 50 Ω.

1.4 HSTL

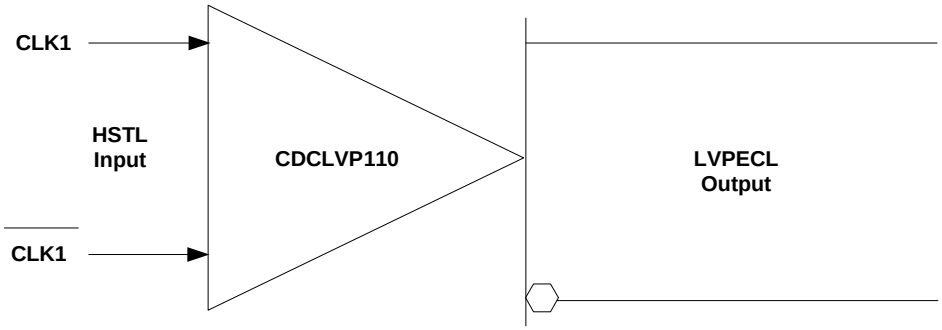


Figure 19. HSTL to LVPECL Converter

The CDCLVP110 in Figure 14 has dual inputs for either HSTL (CLK1 pair is optimized for HSTL levels) or LVPECL inputs (CLK0 pair accepts LVPECL). In both cases, the CDCLVP110

provides LVPECL outputs.

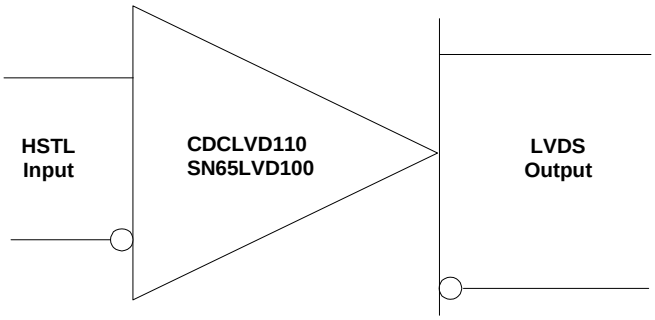


Figure 20. HSTL to LVDS

HSTL signals are usually terminated to (VTT =Vref = 0.75 V). Since most LVDS compatible receivers accept a 200-mV signal swing anywhere between 0 V and 2.4 V; then the HSTL signal is well within the LVDS receiver input range. The typical HSTL signal swing is 400 mV (minimum), 1.1 V (maximum) this amplitude is compatible with the LVDS receiver. The SN65LVDS100 requires a 3.3-V supply, while the CDCLVD110 is 2.5-V LVDS driver/receiver.

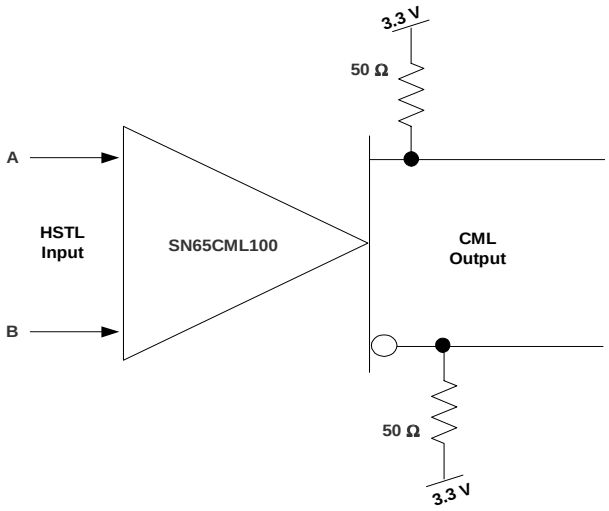


Figure 21. HSTL to CML Translator

The wide common-mode inputs range (0 V to 2.4 V) of the SN65CML100 accepts HSTL levels. The 50-Ω resistors are required to bias the SN65CML100 and terminate the transmission line. Impedance.

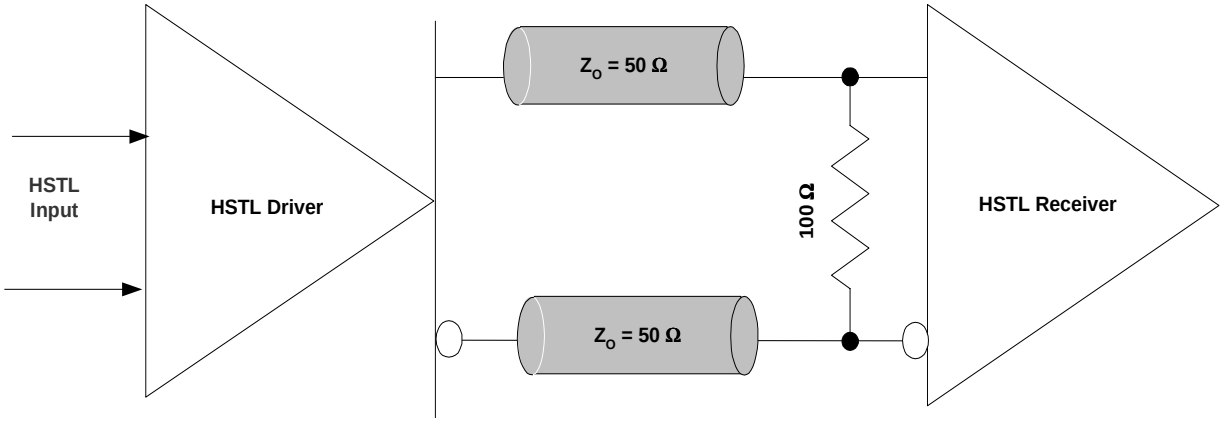


Figure 22. HSTL to HSTL

HSTL signals are usually terminated 50-Ω to VTT (typically VTT = 0.75 V). When VTT is not available, an alternative is a 100-Ω differential termination.

2 References

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