AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML

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ABSTRACT

This report provides a quick reference of ac-coupling techniques for interfacing between different logic levels. The four differential signaling levels found in this report are low-voltage positive-referenced emitter coupled logic (LVPECL), low-voltage differential signals (LVDS), high-speed transceiver logic (HSTL), and current-mode logic (CML). From these four differential signaling levels, 16 interface cases are provided.

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1 AC-Coupling

AC-coupling is used to change the common-mode voltage level when interconnecting different physical layers. A simple example is shown in Figure 1.

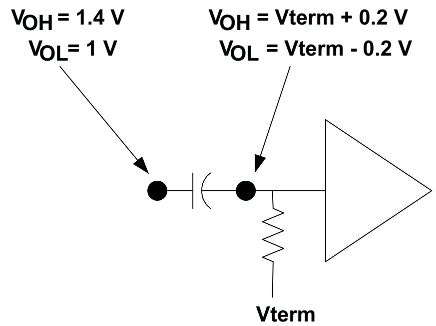


Figure 1. AC-Coupling to Shift Common-Mode Voltage

The capacitor in Figure 1 removes the dc component of the signal (common-mode voltage), while the ac component (voltage swing) is passed on. The resistor to Vterm in Figure 1 represents the biasing structure used to set the common-mode voltage on the receiver side of the ac-coupling capacitor. Throughout this document the capacitor value is 10nF and the biasing structure is either part of the internal biasing of the receiver or an external resistor pull-up and/or pull-down network.

In high-speed applications, ac-coupling is only recommended for dc-balanced signals. AC coupling generates base-line wander in high-speed serial data transmission which is non-dc balanced. Examples of dc-balanced signals are 50% duty cycle clocks, Manchester-coded data, and ANSI fiber channel 8B/10B encoded data.

The more common physical layers (PHYs) that appear in the telecom industry are LVDS, LVPECL, HSTL, and CML. In order to interface these different PHYs, it is important to understand the input and output levels of each. The output and input levels for each of the PHYs are found in Table 1 and Table 2 respectively, and the output and input levels are illustrated in Figure 2.

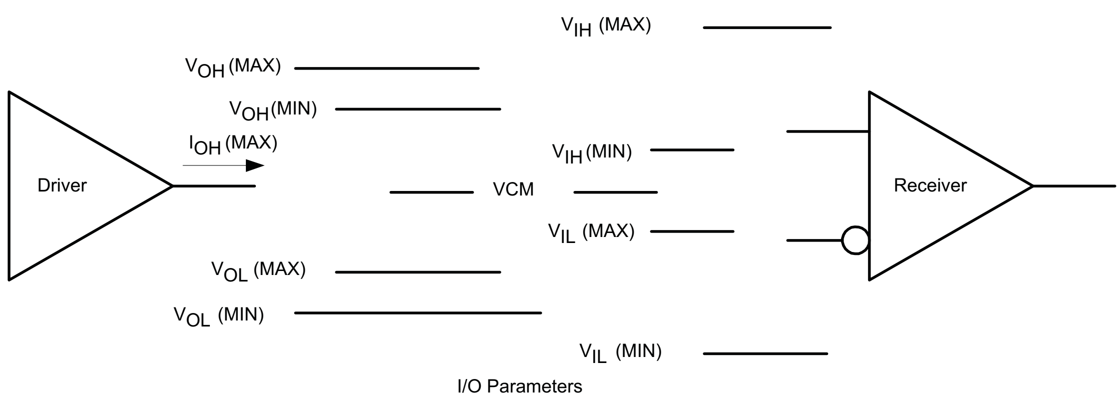


Figure 2. Input and Output Parameters

Table 1. Typical LVPECL, LVDS, HSTL, and CML Outputs

OUTPUT	LVPECL	LVDS	HSTL	CML
V_{OH} (Min)	2.275 V	1.249	VDDQ[(1)]–0.4	V_{CC} [(2)]
V_{OL} (Max)	1.68 V	1.252	0.4	V_{CC} – 0.4 V

(1) VDDQ = 1.5 V ±10%.
(2) VCC = 3.3 V ±10%

Table 2. Typical LVPECL, LVDS, CML, and HSTL Input Levels

INPUT	LVPECL	LVDS	HSTL	CML
V_{IH} (Min)	2.135 V	1.249	V_{Ref} + 0.2	V_{CC}
V_{Ref} or V_{CM}	2	1.2	0.75	V_{CC} – 0.2 V
V_{IL} (Max)	1.825 V	1.252	V_{Ref} – 0.2	V_{CC} – 0.4 V
V_{ID} (Min)	310 mV	200 mV	400 mV	400 mV

The only standardized PHY is LVDS (TIA/EIA-644A); therefore, the interface circuits in this document are only recommended for devices that coincide with the values in Table 1 and Table 2 . The devices listed as examples in each interface circuit have been verified in bench testing with 10nF ac-coupling capacitors.

Table 3. Interface Table

FROM		TO		
	LVPECL	LVDS	CML	HSTL
LVPECL	See Figure 3 or Figure 4	See Figure 5	See Figure 6 or Figure 7	See Figure 8
LVDS	See Figure 9 or Figure 10	See Figure 11 or Figure 12	See Figure 13 or Figure 14	See Figure 15
CML	See Figure 16 or Figure 17	See Figure 18or Figure 19	See Figure 20	See Figure 21 or Figure 22
HSTL	See Figure 23 or Figure 24	See Figure 25 , Figure 26, or Figure 27	See Figure 28	See Figure 29

1.1 LVPECL

The 150-Ω resistor is used to bias the LVPECL output (at V_{CC} – 1.3 V) as well as provide a dc current path for the source current. The pull-up and pull-down combination terminates the 50-Ω transmission line and establishes the LVPECL common-mode voltage of 2 V at the receiver.

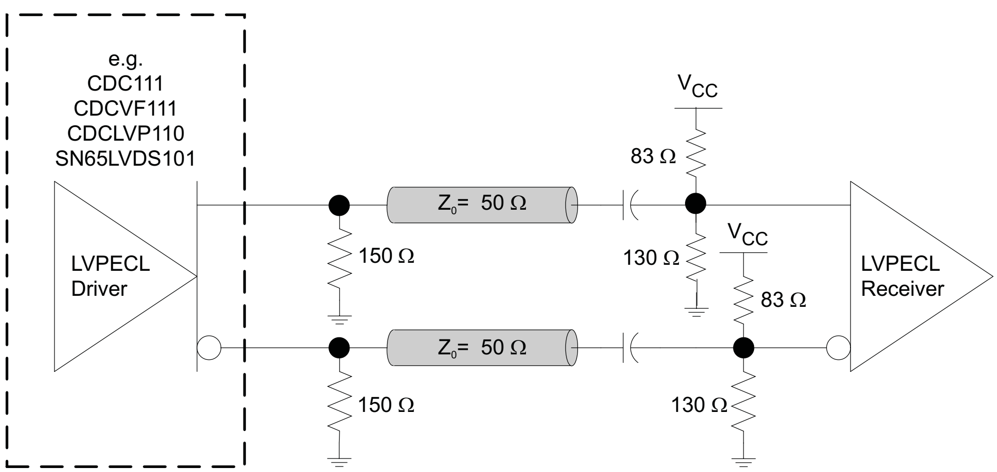


Figure 3. LVPECL to LVPECL

Once again, the 150-Ω resistors are used to bias the LVPECL output (at V_{CC} – 1.3 V) and provide a dc-current path for the source. The split termination with a capacitor is useful in eliminating common-mode noise manifested as differential skew between the true and complementary signals. The VBB output is provided on most LVPECL receivers.

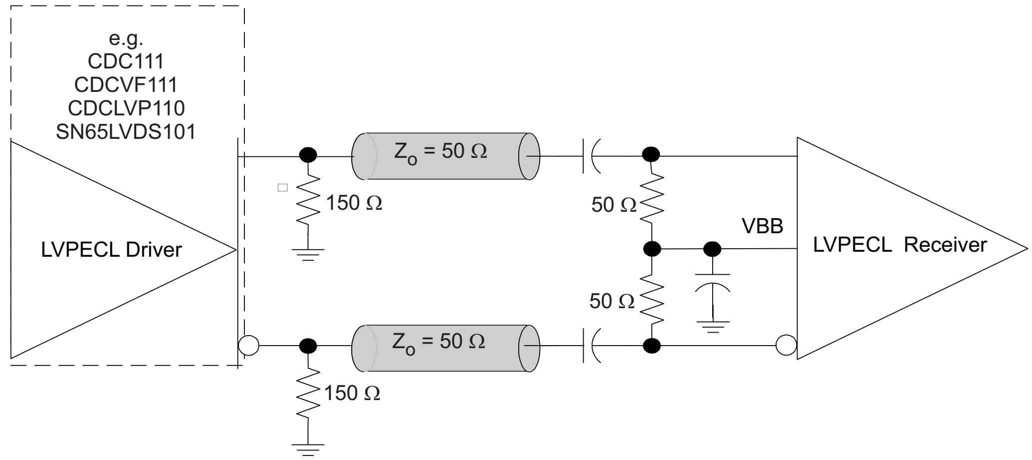


Figure 4. LVPECL to LVPECL

The 150-Ω resistor is used to dc-bias the LVPECL output (at V_{CC} – 1.3 V) as well as provide a dc current path for the source current. The external 100Ω is used to terminate the differential 100-Ω transmission line impedance as well as provide sufficient signal swing to drive the wide common-mode LVDS receivers. The two 10kΩ resistors set the receiver common-mode voltage to 1.65V, which is within the common-mode voltage range of an LVDS receiver (see TIA/EIA-644). For LVDS receivers with integrated 100-. termination the external 100-Ω resistor in Figure 5 is not required (e.g., SN65LVDT33, SN65LVDT100, and SN65LVDT122).

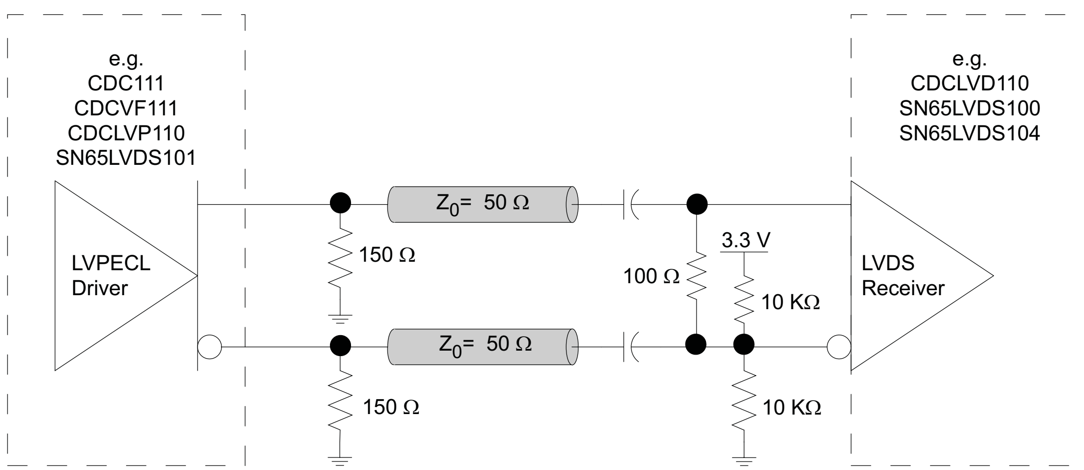


Figure 5. LVPECL to LVDS

In Figure 6, there are two resistors, the 150Ω (R-bias) and Ra. The 150-Ω resistor is required to dc-bias the LVPECL outputs prior to ac-coupling. The value of R-bias ranges from 140Ω to 240Ω. In the case where the differential LVPECL output is larger than what the CML receiver can tolerate, then Ra should be used to attenuate the LVPECL output such that it meets the input voltage required for the CML receiver.

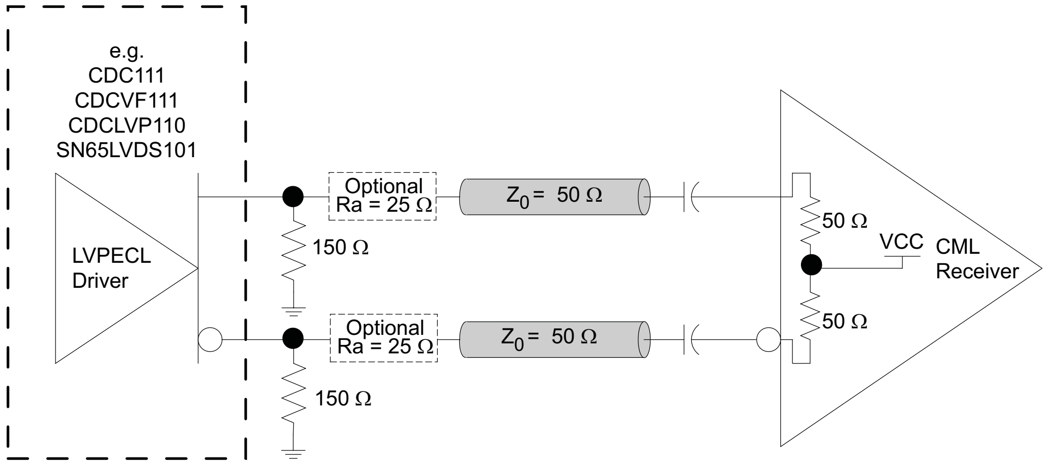


Figure 6. LVPECL to CML

For example, if the LVPECL output swing is 750 mV and the required CML receiver input is 400 mV, then the attenuation factor is 0.68, which requires Ra ≅ 23Ω. In Figure 6 the CML receiver is assumed to be self-biased.

The SN65CML100 in Figure 7 can be used as an LVPECL to CML converter. The 50-Ω pull-up resistors are required to bias the SN65CML100 outputs. The coupling capacitors on the inputs (optional, but shown for completeness) are used assuming that the LVPECL source is properly terminated.

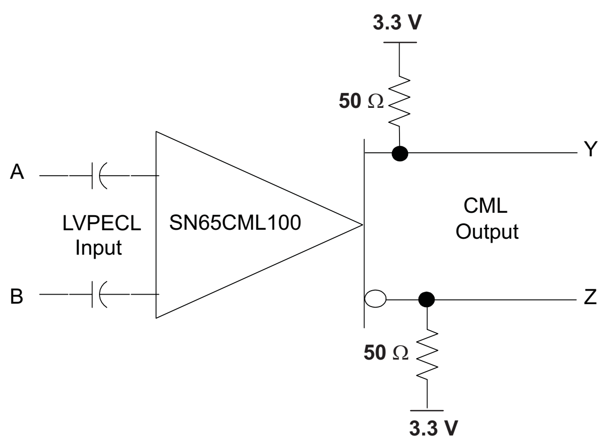


Figure 7. LVPECL to CML Converter

The 150-Ω resistor is used to bias the LVPECL output (at V_{CC}–1.3 V) as well as provide a dc current path for the source. The equivalent 50-Ω. Thevenin resistors of R1 and R2 are used to terminate the trace impedance as well as to set the common-mode voltage (VCM = 0.75 V) for the HSTL receiver, Figure 8.

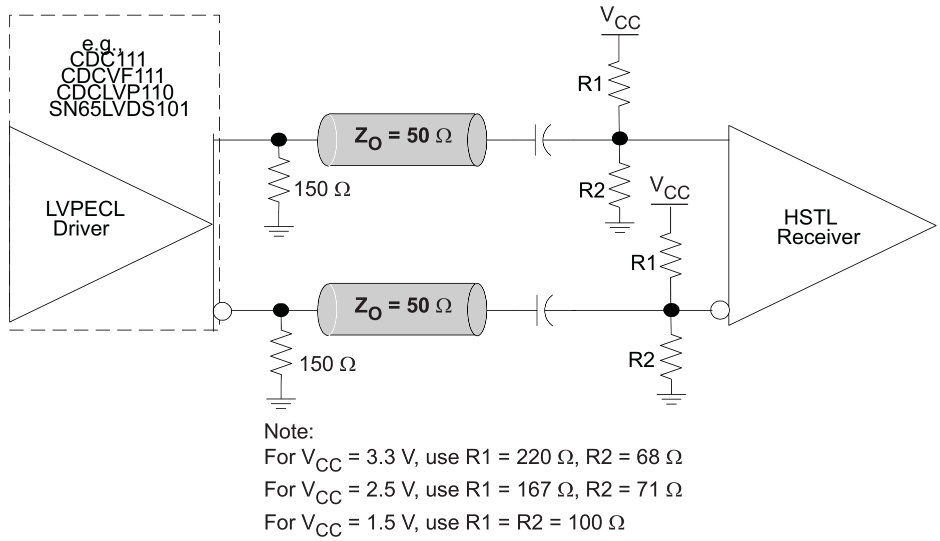


Figure 8. LVPECL to HSTL

The Thevenin equivalent of the 83Ω and 130Ω in Figure 9, matches the 50-Ω transmission line impedance as well as sets the common-mode voltage (VCM = 2 V) for the LVPECL receiver.

1.2 LVDS

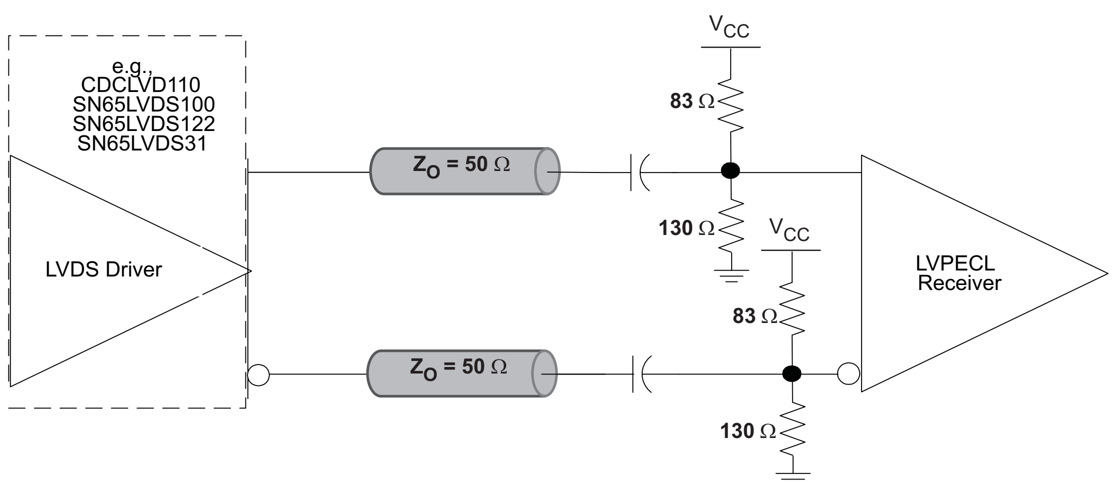


Figure 9. LVDS to LVPECL

Figure 10 is recommended when VBB is available on the LVPECL receiver. The split termination with the capacitor to ground is useful in eliminating common-mode noise manifested as differential skew between the true and complementary signals.

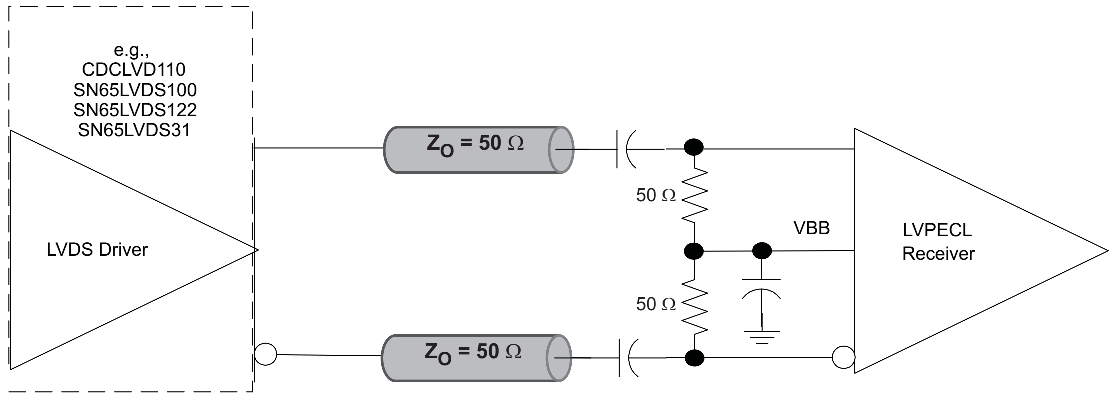


Figure 10. LVDS to LVPECL

In Figure 11 is a combination of the more common 100-Ω termination and ac-coupling. It also assumes that the LVDS receiver does not include on-chip termination.

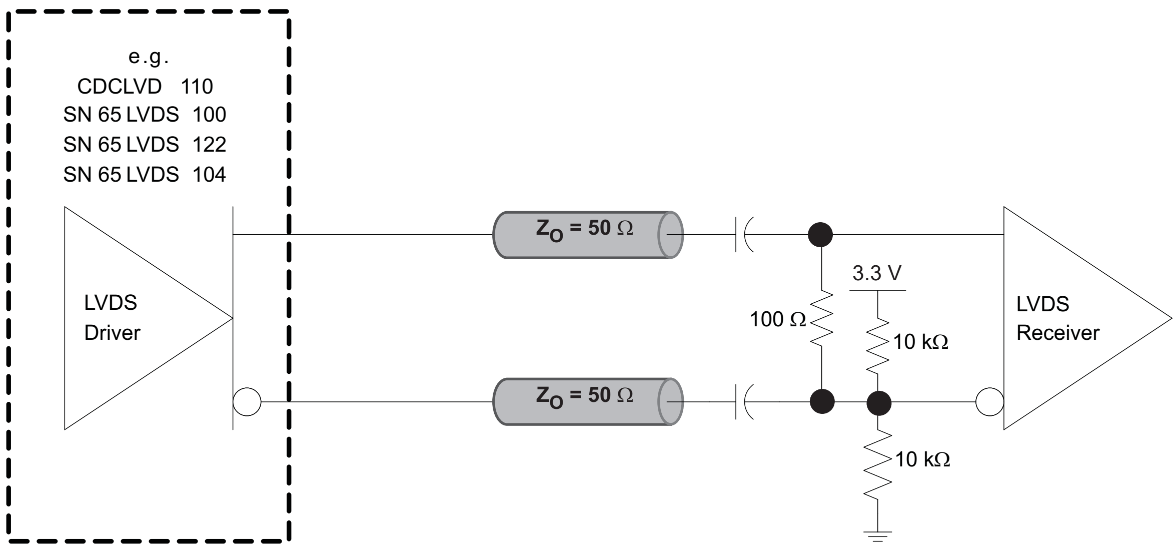


Figure 11. LVDS to LVDS

Figure 12 has an advantage over Figure 11 of correcting for (differential) skew mismatch between the true and complementary signals. Both Figure 11 and Figure 12 assume that the LVDS receiver is self-biased.

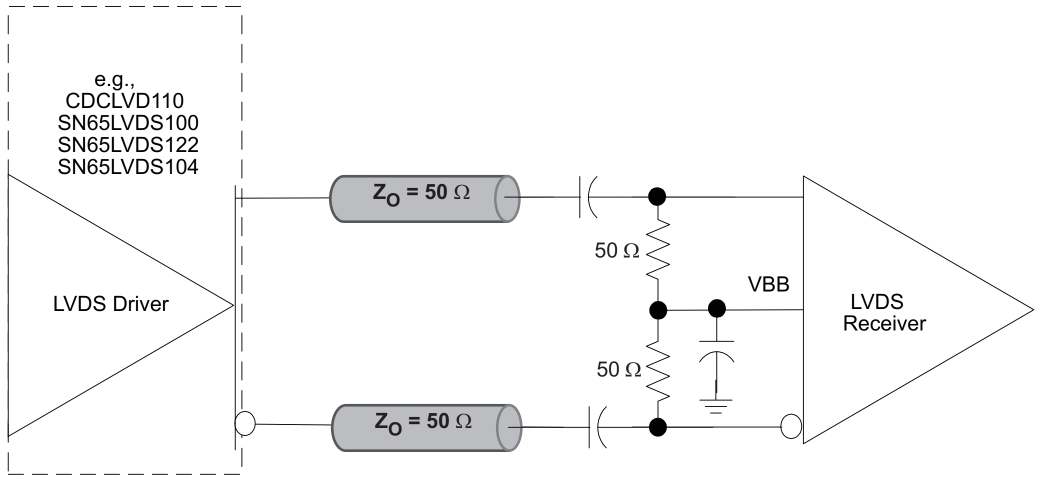


Figure 12. LVDS to LVDS

Most CML receivers have an on-chip termination, and there is no need for additional resistors to terminate the transmission line. The two 10-kΩ resistors are only required if the CML receiver is not self-biased and may vary form one vendor to another; see the manufacturer's data sheet for details.

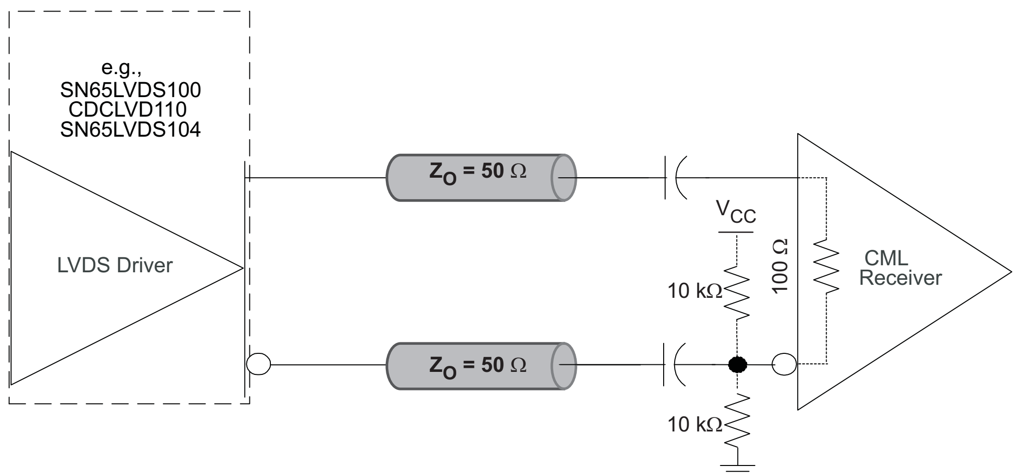


Figure 13. LVDS to CML

The SN65CML100 has a wide-common mode receiver, which allows the device to be used as an LVDS to CML translator. Two 50-Ω pull-up resistors are required to terminate the trace and bias the SN65CML100 output stage, as shown Figure 14. Figure 14 implies that the LVDS input is properly terminated.

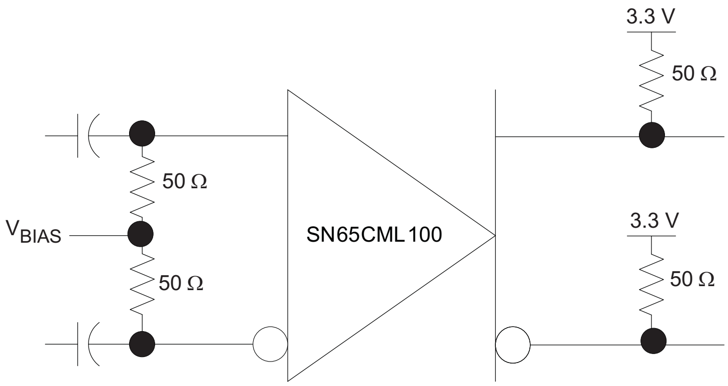
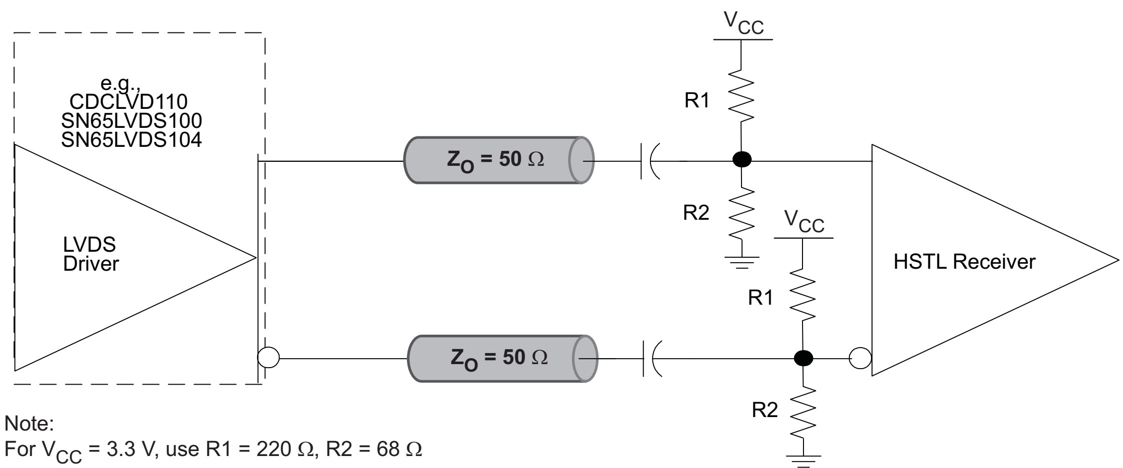


Figure 14. LVDS to CML Translator

The value of the two resistors, R1 and R2 depends on the receiver supply voltage and the common-mode voltage range of the receiver. If the HSTL receiver has a 1.5-V supply, then R1 and R2 are 100Ω each (50Ω equivalent) to terminate the trace. For other supply voltages (see the note in Figure 15) R1 and R2 should be chosen such that their parallel combination matches the transmission line and the mid-point is set to the common-mode of the HSTL receiver (VCM = 0.75 V).



Note:
For V_{CC} = 3.3 V, use R1 = 220 Ω, R2 = 68 Ω
For V_{CC} = 2.5 V, use R1 = 167 Ω, R2 = 71 Ω
For V_{CC} = 1.5 V, use R1 = R2 = 100 Ω

Figure 15. LVDS to HSTL

1.3 CML

The 50-Ω pull-up resistors are used to dc-bias the CML outputs and provide a source termination to match the transmission line. Figure 16 assumes that the LVPECL input stage is self-biased.

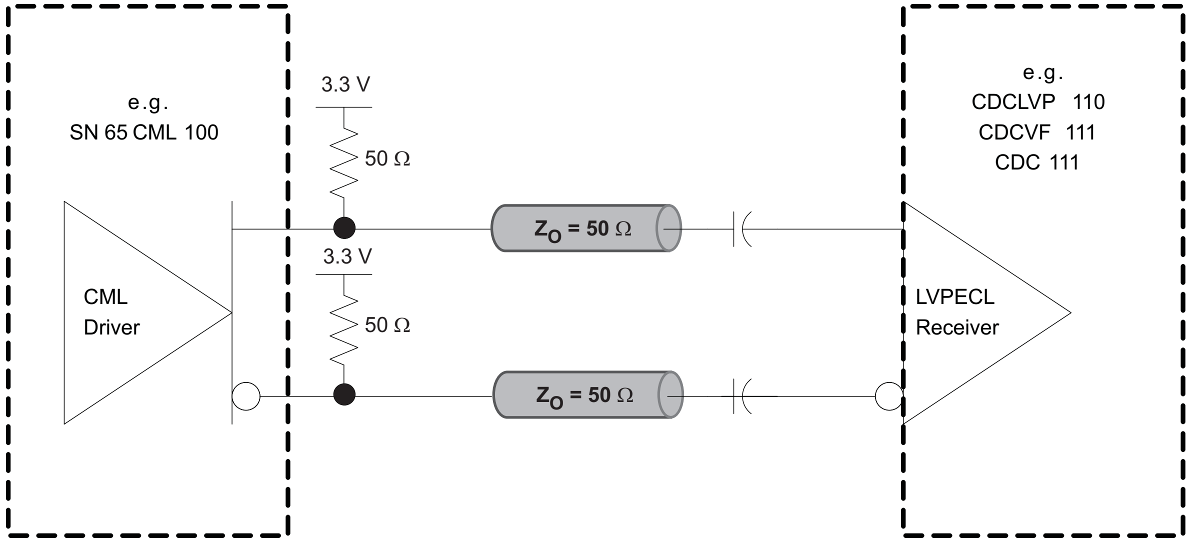


Figure 16. CML to LVPECL

The 50-Ω pull-up resistors are required for the SN65CML100 to bias and source-terminate the transmission line. R1 in Figure 17 should be larger than 50Ω in case the CML output stage losses, in addition to the PCB losses, are too high to meet the minimum differential input voltage (VID) swing requirement of the LVPECL input stage.

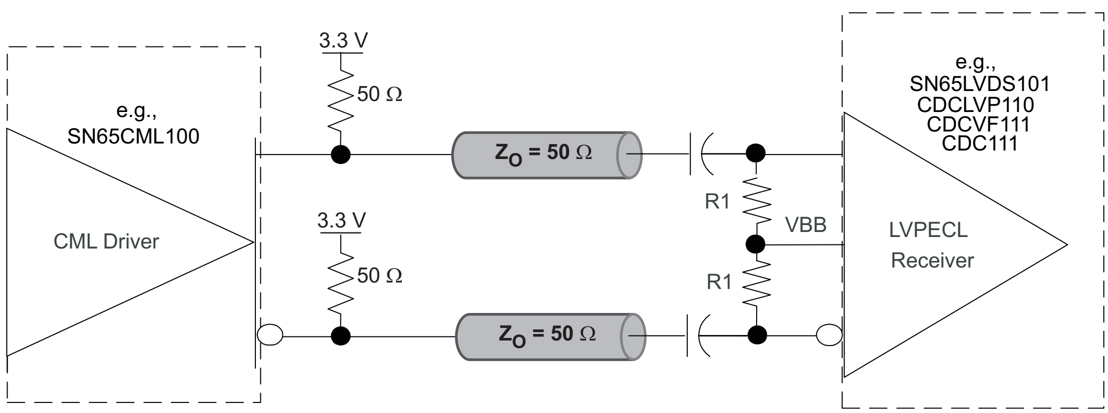


Figure 17. CML to LVPECL

The 50-Ω pull-up resistors are used to dc-bias and source-terminate the SN65CML100 outputs. The LVDS receiver has a wide input common-mode range (between 0 V and 2.4 V), that is, the receiver can accept any signal within the common-mode range and a differential swing of at least 100 mV. Figure 18, assumes a self-biased LVDS receiver.

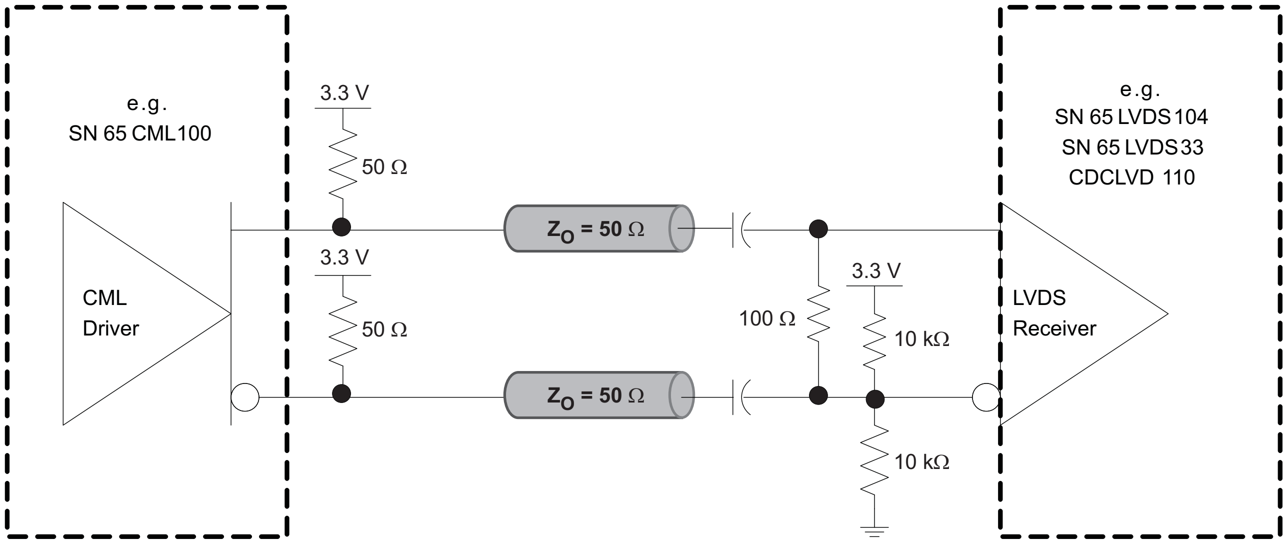


Figure 18. CML to LVDS

The 50-Ω pull-up resistors are required for the SN65CML100 to bias and source-terminate the transmission line. R1 in Figure 19 should be larger than 50Ω in case the CML output stage losses, in addition to the PCB losses, are too high to meet the minimum (voltage input differential (VID) swing requirement of the LVDS input stage. Figure 19 assumes an internally generated bias voltage pin (VBB) is available.

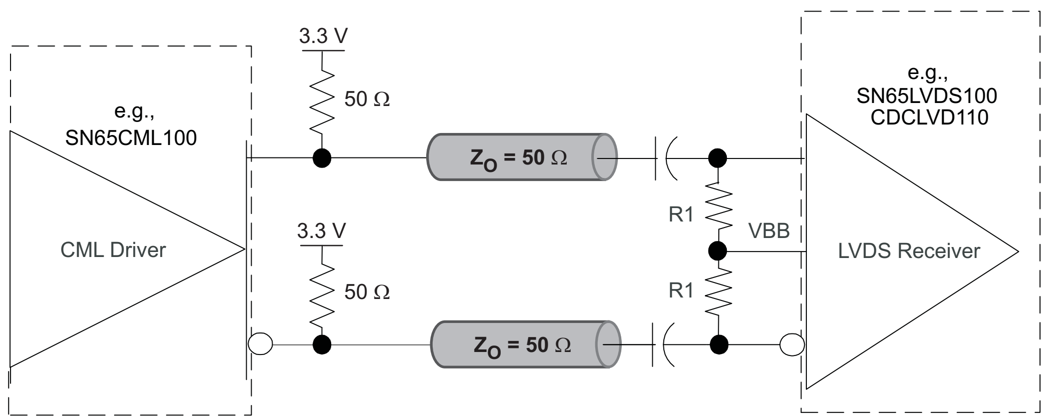


Figure 19. CML to LVDS

CML comes in many distinctions; therefore, termination and bias structures are not applicable to all CML drivers and receivers. The 50-Ω pull-up resistors, in Figure 20, are required to dc-bias the SN65CML100 and source-terminate the transmission line, while other CML drivers have integrated 50-Ω pull-up resistors, which do not require the external 50-Ω pull-up resistors.

The two 10-kΩ resistors are only required if the CML receiver is not self-biased and may vary from one vendor to another; see the manufacturer's data sheet for details.

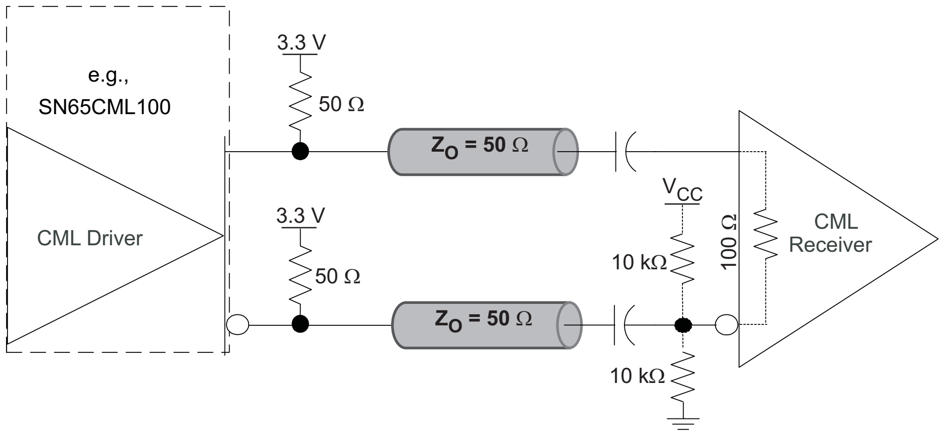
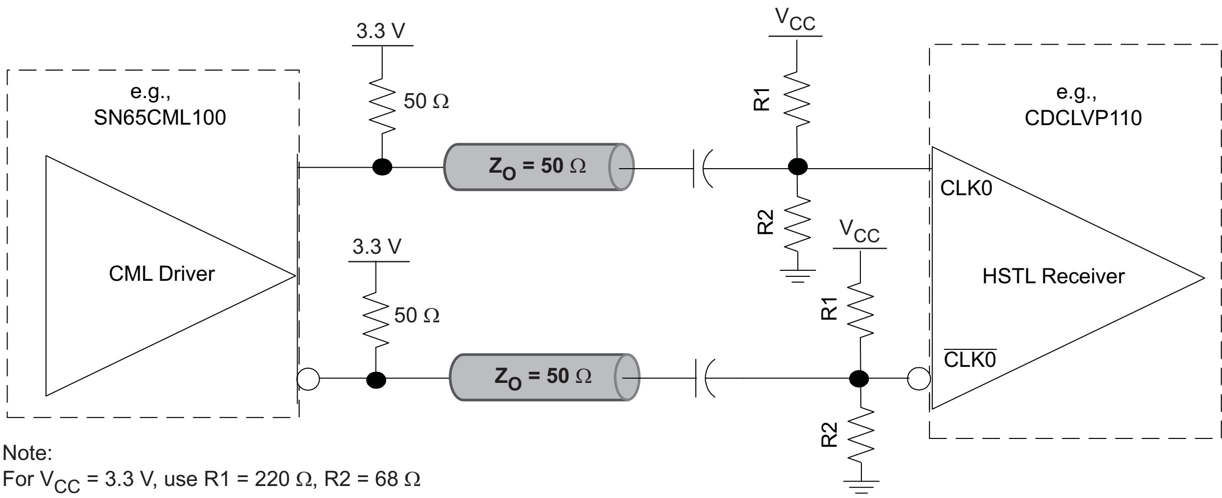


Figure 20. CML to CML

In Figure 21, the 50-Ω pull-up resistors are required to dc-bias the SN65CML100 outputs. The parallel combination of R1 and R2 are used to set the HSTL common-mode voltage (VCM = 0.75 V).



Note:
For V_{CC} = 3.3 V, use R1 = 220 Ω, R2 = 68 Ω
For V_{CC} = 2.5 V, use R1 = 167 Ω, R2 = 71 Ω
For V_{CC} = 1.5 V, use R1 = R2 = 100 Ω

Figure 21. CML to HSTL

The 50-Ω pull-up resistors are required to dc-bias the SN65CML100 outputs. The split termination with the capacitor is useful in eliminating common-mode noise manifested as differential skew between the true and complementary signals. VBB output may be provided by HSTL receiver. R1 in Figure 22 should be larger than 50Ω when the CML output stage and the PCB losses are too high to meet the minimum voltage input differential (VID) swing requirement of the HSTL input stage.

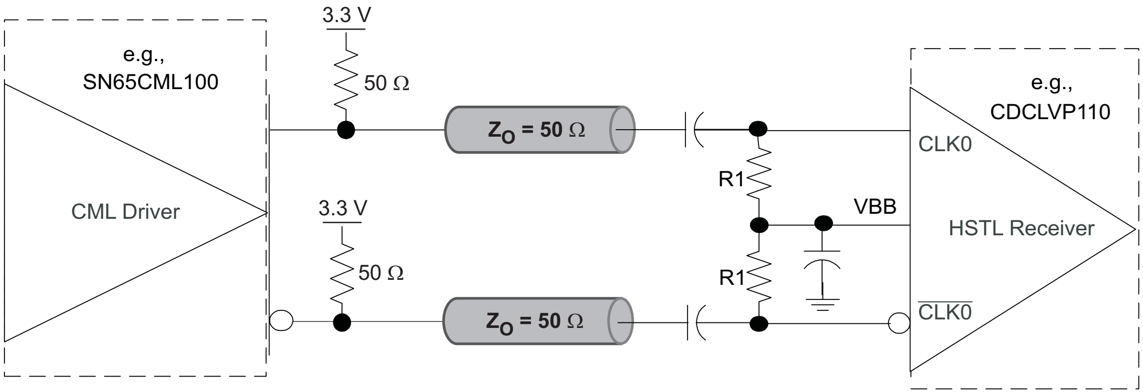


Figure 22. CML to HSTL

1.4 HSTL

In Figure 23, the split 50-Ω resistors are used to terminate the trace impedance as well as set the common-mode voltage (VCM = 2) for the LVPECL receiver. The split termination with the capacitor is useful in eliminating common-mode noise manifested as differential skew between the true and complementary signals. VBB output is provided on most LVPECL receivers.

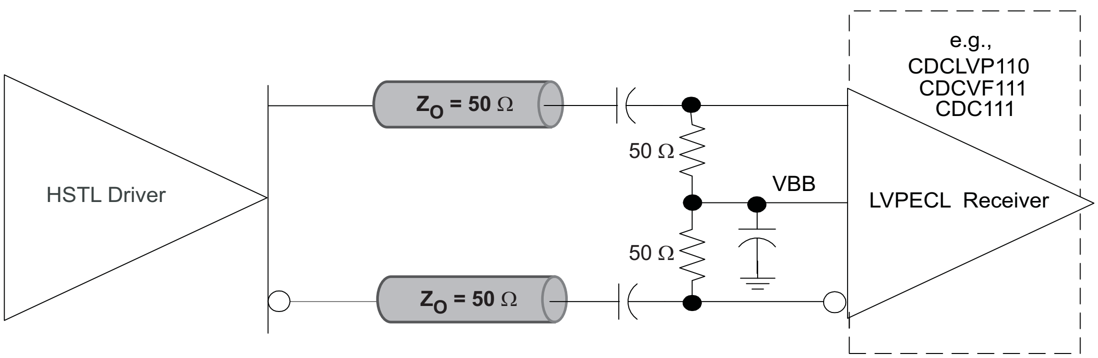


Figure 23. HSTL to LVPECL

The CDCLVP110 has a dual input that can accept either HSTL (CLK1 pair) or LVPECL input (CLK0 pair) levels and provide LVPECL output signals. The ac-coupling capacitors are not required for the CDCLVP110; nevertheless, they are included for completeness. The device functions properly without the coupling capacitors since the input stage of the CLK1 pair is optimized for HSTL input levels.

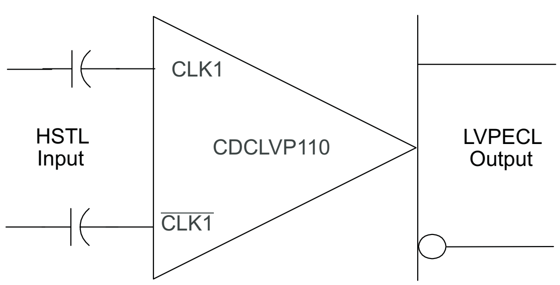


Figure 24. HSTL to LVPECL Converter

HSTL signals are usually terminated to (VTT = Vref = 0.75 V). Since most LVDS compatible receivers accept a 200-mV signal swing anywhere between 0 V and 2.4 V, then the HSTL signal is well within the LVDS receiver input range. The typical HSTL signal swing is 400 mV (minimum), 1.1 V (maximum) this amplitude is easily accepted by the LVDS receiver. The SN65LVDS100 requires a 3.3-V supply, while the CDCLVD110 is 2.5-V LVDS driver/receiver.

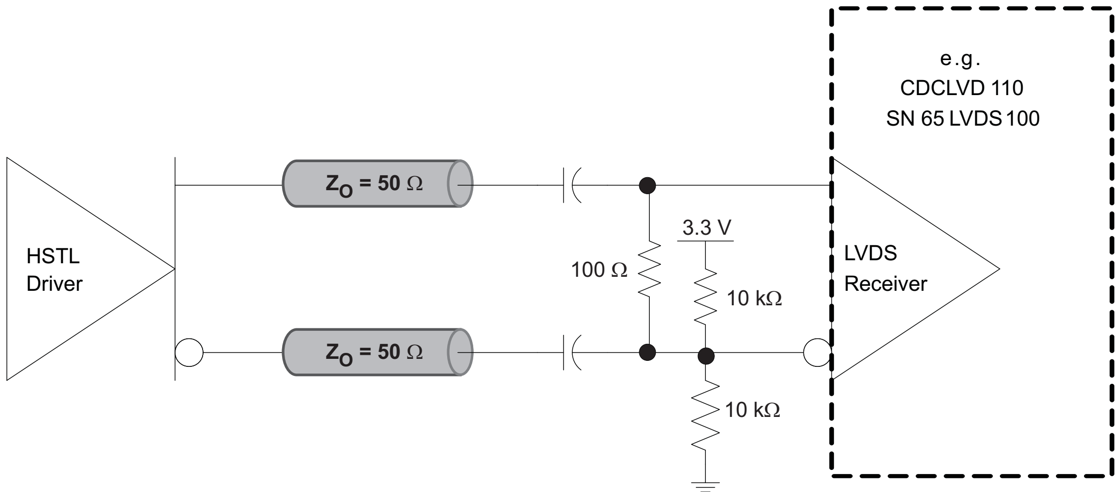


Figure 25. HSTL to LVDS

The split termination with capacitor in Figure 26 is recommended over Figure 25 in eliminating common-mode noise manifested as differential skew between the true and complementary signals. VBB output is provided on both the CDCLVD110 and the SN65LVDS100.

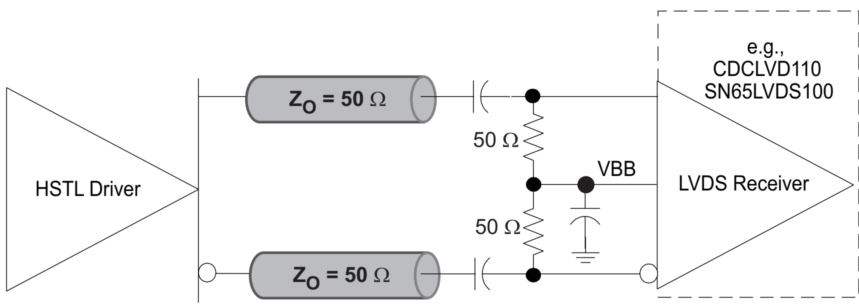


Figure 26. HSTL to LVDS

Both the SN65LVDS100 (3.3-V supply) and the CDCLVD110 (2.5-V supply) have wide input common-mode ranges and are capable of translating form HSTL to LVDS signaling levels.

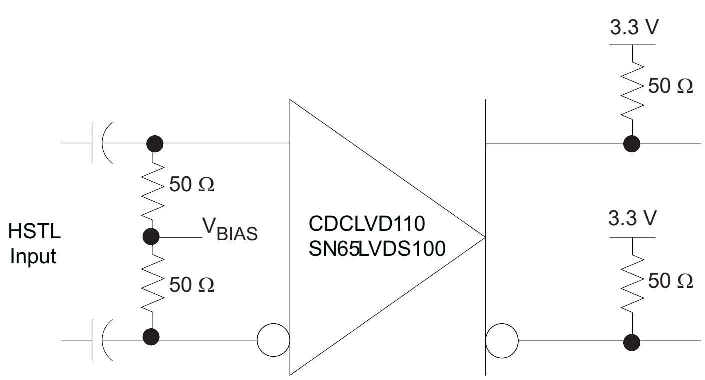


Figure 27. HSTL to LVDS Converter

The wide common-mode inputs range (0 V to 2.4 V) of the SN65CML100 can accept HSTL levels. If the 100-Ω .resistor is not included on-chip, then it should be added externally in order to match the transmission line impedance for proper termination. The two 10-kΩ resistors are only required if the CML receiver is not self-biased and may vary form one vendor to another, see the manufacturer's data sheet for details.

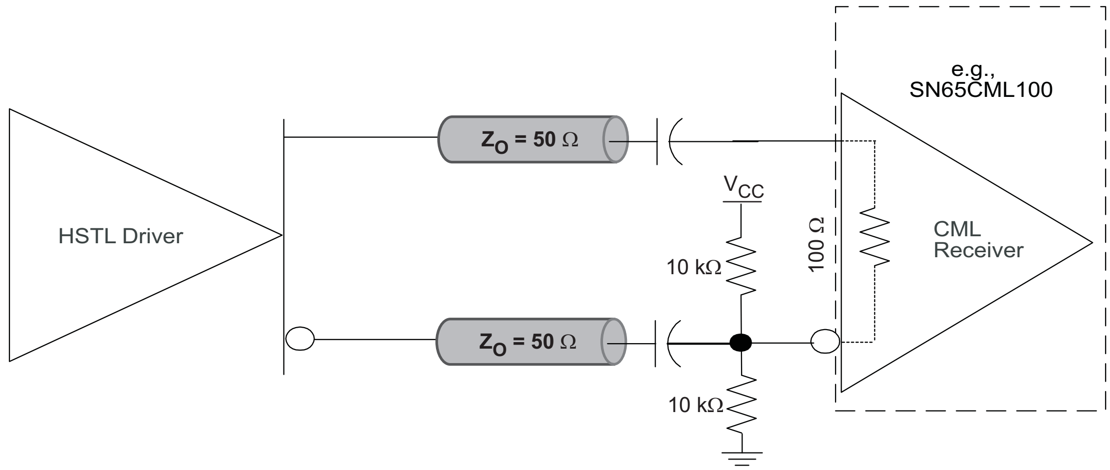


Figure 28. HSTL to CML

HSTL signals are terminated to VTT (typically 0.75 V). An alternative is 100Ω across the differential pair or a split 50Ω on each leg.

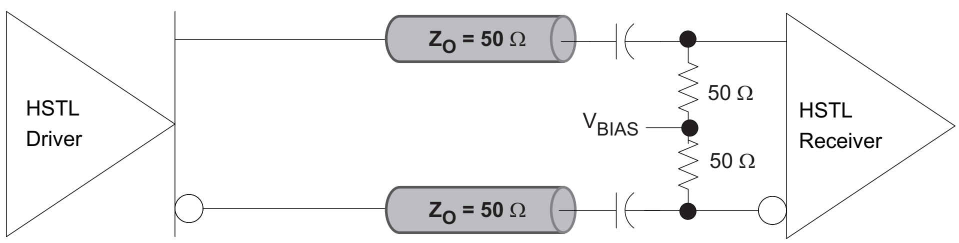
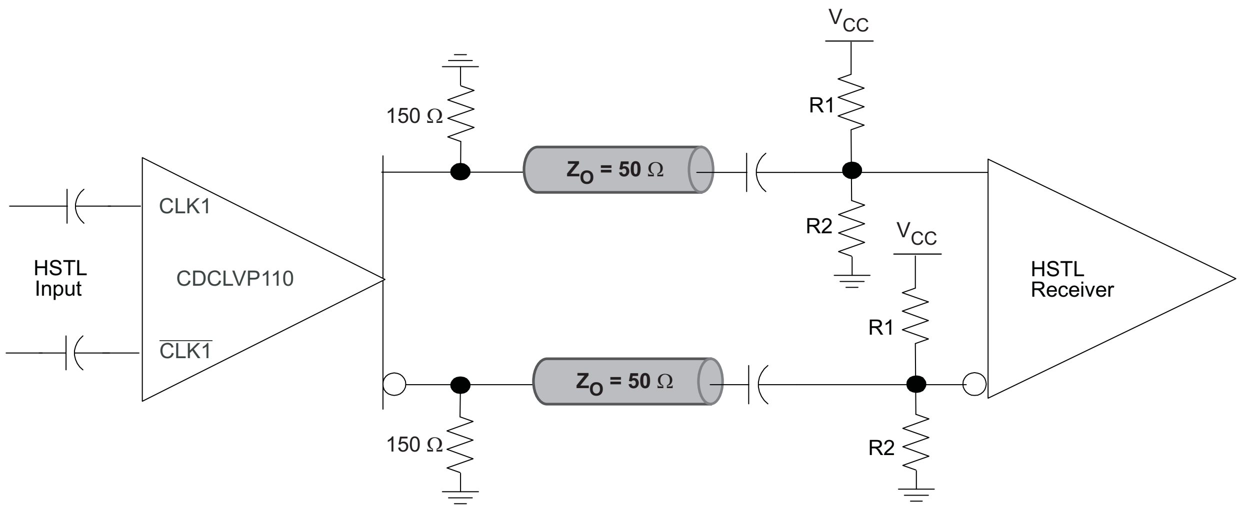


Figure 29. HSTL to HSTL

HSTL signals are usually terminated to (VTT = Vref = 0.75 V). The CDCLVP110 has a dual input that can accept either HSTL or LVPECL input levels and provide LVPECL output signals. The 150-Ω resistor is used to bias the LVPECL output (at VCC-1.3 V) as well as provide a dc current path for the source. The equivalent 50-Ω Thevenin resistors of R1 and R2 are used to terminate the trace impedance (the LVPECL output) and to set the common-mode voltage (VCM = 0.75 V) for the HSTL receiver.



Note:
For V_{CC} = 3.3 V, use R1 = 220 Ω, R2 = 68 Ω
For V_{CC} = 2.5 V, use R1 = 167 Ω, R2 = 71 Ω
For V_{CC} = 1.5 V, use R1 = R2 = 100 Ω

Figure 30. HSTL to LVPECL to HSTL Using the CDCLVP110

If the HSTL receiver has a 1.5-V supply, then R1 and R2 are 100 . each (equivalent 50Ω) to match the trace impedance. For other supply voltages, R1 and R2 should be chosen such that their parallel combination matches the transmission line and the midpoint is set to the common mode of the HSTL receiver (VCM = 0.75 V).

2 References

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6. CDCLVP110 data sheet, Texas Instruments (SCAS683)
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