Application Note

LDO Thermal Performance Improvements Enable Die Size Reduction

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ABSTRACT

This application note covers a thermal exploration into the decreasing LDO die and package size of Texas Instruments low-dropout regulators (LDO). Additionally, an overview on thermal resistance, FET description and design, as well as LDO thermal performance are provided. This application note covers thermal resistance results of transitioning from a 2.68mm^2 die size to a 0.75mm^2 die size, otherwise viewed as a 72% decrease in die area.

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Trademarks

1 Introduction

LDO package thermal limitations are a key factor when determining the functionality of a device. Many applications require a device to handle large differences between the input and output voltage, leading to a significant increase in junction temperature, T_J, due to the power dissipated, P_D, in the system. High junction temperature can affect the lifetime reliability and accelerate common failures (*LDOs Thermal Performance in Small SMD Packages*, application note). Additionally, the region of operation of the LDO can become limited due to thermal shutdown being triggered from a rise in T_J. Consequently, the device can become unable to perform as intended. Reducing the thermal resistance, $R_{\Theta JA}$, is critical to extending device lifetime and operation. The thermal resistance is a measure of a package's ability to dissipate heat to the ambient environment ,T_A , which is typically calculated using Equation 1.

$$R_{\Theta JA} = (T_J - T_A) / P_D \quad (1)$$

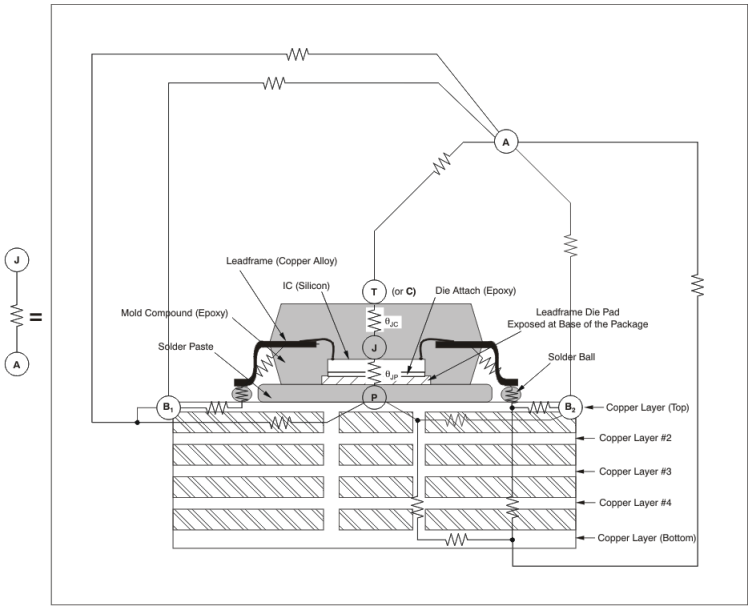

Figure 1-1. Thermal Resistance Network

Additionally, the LDO die size can contribute to thermal limitations. By spreading the same amount of heat over a smaller area, peak temperature and the resulting $R_{\Theta JA}$ parameter can increase. A well designed die can efficiently spread heat generated by power dissipation of the LDO. In a LDO, the pass FET is the main source of heat in the device. The die helps to distribute and spread heat throughout the bulk of the silicon. Heat is then transferred to the path of least thermal resistance or the path with the highest thermal conductivity. In a package with a large thermal pad, heat flows through the silicon die to the *die attach* material. After reaching the die attach material, heat transfers to the thermal pad, and then to the PCB, where the heat finally flows to the ambient, otherwise known as the external environment.

Thermal performance can also be impacted through the LDO's pass FET design. A properly laid out pass FET can maximize the FET area, perimeter, and aspect ratio to spread the heat across a larger area through the bulk of the silicon die.

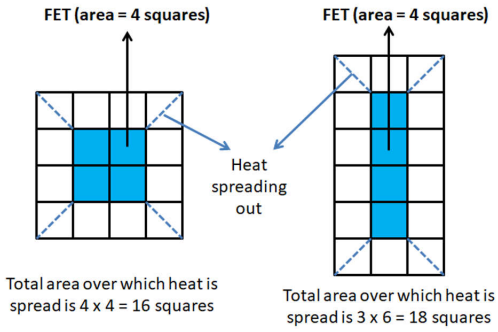

Figure 1-2. FET Redesign to Allow for Greater Heat Dissipation

When redesigning a LDO to reduce the die size, alternate FET shapes can modify the electrical performance. The thermal performance can be optimized to make sure that the electrical performance of the LDO still meets data sheet specifications. Ultimately, the TPS74801 die area was decreased by over 72% while also maintaining the $R_{\Theta JA}$ specification, which has allowed for an improved ability to maintain device thermal specification and accuracy.

2 Simulation and Measurement Results

There are multiple properties of an LDO which influence thermal performance, including the following:

1. Shape and area of the pass FET
2. Shape and area of the die
3. Die thickness
4. Die attach thickness
5. Die attach conductivity
6. Mold compound conductivity
7. Metal layer deposition

With the preceding discussion in mind, the TPS748 die (Figure 2-1) was redesigned (Figure 2-2) to reduce the die area by 72% while maintaining nearly identical thermal performance.

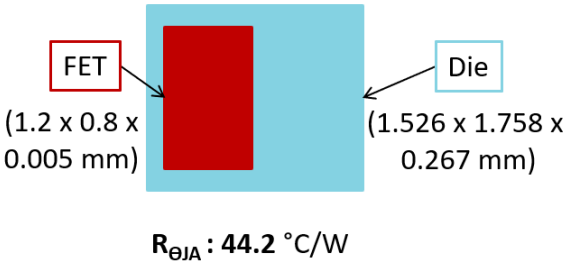

Figure 2-1. Legacy Die of TPS748

For the redesigned TPS748, the die attach and mold compound were improved and incorporated into the design.

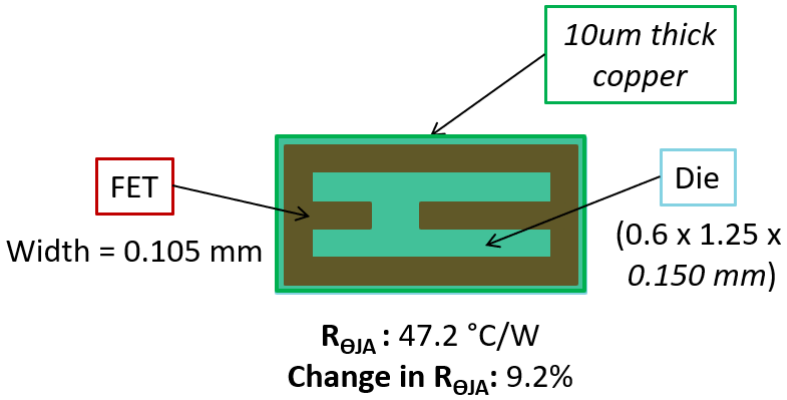

Figure 2-2. New Die of TPS748

2.1 Measurements

Measurements were taken using the TPS74801EVM-177 at an ambient temperature, T_A , of 25°C. Measurements were conducted comparing the legacy TPS748 design and the new TPS748 design, using test methodologies described in *Measuring the Thermal Impedance of LDOs in Situ*.

Table 2-1. Legacy Die vs. New Die Thermal Performance: V_{IN} and V_{BIAS} = 3V

Conditions	Legacy Die	New Die
V_{OUT}	1.2V	1.2V
I_{OUT}	1A	1A
Power Dissipated (P_D)	1.8W	1.8W
Ambient Temperature (T_A)'	132.8°C	122.6°C

Table 2-2. Legacy Die vs. New Die Thermal Performance: V_{IN} and V_{BIAS} = 4V

Conditions	Legacy Die	New Die
V_{OUT}	1.2V	1.2V
I_{OUT}	1A	1A
Power Dissipated (P_D)	2.8W	2.8W
Ambient Temperature (T_A)"	115.3°C	101.9°C

Using the following junction to ambient thermal resistance equation stated in the *Measuring the Thermal Impedance of LDOs in Situ,* paper:

Legacy die:

$$R_{\theta JA} = \frac{T_A' - T_A''}{P_D'' - P_D'} = \frac{132.8°C - 115.3°C}{(4V - 1.2V) \times 1A - (3V - 1.2V) \times 1A} = 17.5\frac{°C}{W} \quad (2)$$

New die:

$$R_{\theta JA} = \frac{T_A' - T_A''}{P_D'' - P_D'} = \frac{122.6°C - 101.9°C}{(4V - 1.2V) \times 1A - (3V - 1.2V) \times 1A} = 20.7\frac{°C}{W} \quad (3)$$

Finally, thermal camera imaging was used to measure the case temperature for both the legacy and new devices. Both devices with the VSON package were placed on the EVM. The test conditions were Vout = 1.2V, Vin = 2.2V, Vbias = 2.7V, and Iout =1.5A (for example, Power Dissipation =1.5W), and after maintaining this for 30 minutes, thermal camera imaging was done as shown in Figure 2-3 and Figure 2-4. Maximum case temperatures were measured as 71°C and 69°C for the legacy and new device respectively.

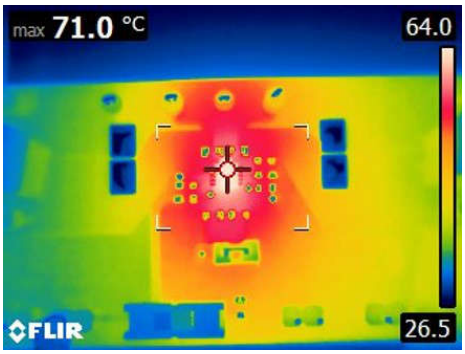

Figure 2-3. Thermal Camera Shot Legacy TPS748 Device

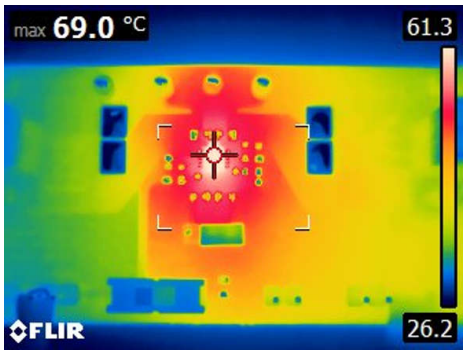

Figure 2-4. Thermal Camera Shot Redesigned TPS748 Device

Now using equation 8 stated in the Semiconductor and IC Package Thermal Metrics paper, $T_J = T_C + (\psi_{JT} \times \text{Power})$, and ψ_{JT} values mentioned in the data sheet, T_J can be calculated as 72.05°C for the legacy die and 75.3°C for the new die.

3 Summary

The die reduced by 72% with only a modest change to the thermal resistance, 44.2°C/W for the legacy die versus 47.2°C/W for the new die using a JEDEC standard layout. An EVM, which represents a more accurate layout to the test methodologies stated in *Measuring the Thermal Impedance of LDOs in Situ*, was used to capture the $R_{\Theta JA}$ value. The test metholodies showed similar results for $R_{\Theta JA}$ between the legacy die and new die, 17.5°C/W for the legacy die versus 20.7°C/W for the new die. ψ parameters are intended to, by the JEDEC committee, accurately estimate the junction temperature given by a board thermal measurement. Thermal images were captured of the legacy and new TPS748 LDO. While using the ψ_{JT} parameters, the junction temperature between the legacy and new die correlated to the JEDEC simulations and EVM measurements, 72.05°C for the legacy die and 75.3°C for the new die. Ultimately, the thermal performance of the legacy and new TPS748 LDO devices are comparable.

4 References

- Texas Instruments, *LDOs Thermal Performance in Small SMD Packages*, application note.
- Texas Instruments, *TPS748 1.5A, Low-Dropout Linear Regulator With Programmable Soft-Start*, data sheet.
- Texas Instruments, *Semiconductor Packaging Assembly Technology*, application note.
- Texas Instruments, *Measuring the Thermal Impedance of LDOs in Situ*, application note.
- Texas Instruments, *TPS74701EVM-177, TPS74801EVM-177 Evaluation Module*.

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