Technical White Paper

Parallel LDO Architecture Design Using Ballast Resistors

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ABSTRACT

Low-dropout regulators (LDO) are required in many applications because compared to switching converters they are inherently low noise while maintaining a low cost and simple solution. In applications where board space and output voltage tolerance are both at a premium, LDOs present a compelling design choice over switching converters as the later will often need large magnetics or capacitor banks to filter out the ripple voltage. Unfortunately using a single LDO for the supply is not always possible and it is now common to see engineers place 5-10 LDO's in parallel. Designers need a method to determine how many parallel LDO's are required to meet not just the system load current and load voltage, but thermals, system noise, and system PSRR requirements as well. This paper presents a method to calculate the optimum ballast resistance and minimum number of parallel LDO's required to meet a series of system requirements.

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Trademarks

1 Introduction

Paralleling LDO's using ballast resistors have been discussed in the industry for many years. Traditionally, the analysis techniques that have been developed are limited to two parallel LDO's, and ballast resistance calculations are limited to current imbalance of the LDOs. More recently Texas Instruments published a technical white paper to enable parallel designs of any number of LDOs while also meeting the load voltage [see reference 4]. A detailed discussion on key system specifications (such as temperature, PSRR, noise, and dropout voltage) is missing entirely from the literature.

Modern systems require parallel LDO designs to meet more than just additional load current and methods to accurately design with more than two parallel LDO's must be developed. Many engineers want to use 5-10 parallel LDO's to meet their system requirements such as noise, load voltage, temperature, dropout, and PSRR. We must be able to derive the minimum number of parallel LDO's required to meet these system specifications based on a worst-case analysis. This technical white paper will provide a new mathematical foundation to answer these questions. From this, we can support a new generation of designs which may parallel any number of LDO's required to meet the system noise, load voltage, load current, temperature, dropout, and PSRR specifications.

2 System Architecture Design – How Many Parallel LDO's are Required?

The following definitions are used in this white paper:

I_{LOAD}	System Load Current
n	Number of parallel LDOs
V_{IN}	Input Voltage
V_{OUT}	Output Voltage
Headroom Voltage	V_{IN} - V_{OUT}
V_{DROP}	Dropout Voltage = Minimum headroom voltage required to regulate V_{OUT}
$I_{LDO\_MAX\_DROPOUT\_LIM}$	The limited current each LDO can provide from the available headroom voltage
$I_{LDO\_MAX\_TEMP\_LIM}$	The limited current each LDO can provide before exceeding the specified T_J limit
I_{LDO_MAX}	The maximum rated current of the LDO
I_{LDO_PSRR}	The maximum output current for a single LDO that meets the specified PSRR specification, as shown in the PSRR measurements

2.1 Noise

LDO's generate noise which can be modeled as a noise source, e_{O_single}. When placing LDO's in parallel, each noise source is uncorrelated to the rest of the noise sources. The system noise e_{O_target} then is reduced by the square root of the number of parallel LDO's. Thus the number of parallel LDO's required to meet a system noise density requirement is:

$$n \geq \left(\frac{e_{O\_single}}{e_{O\_target}}\right)^2 \quad (1)$$

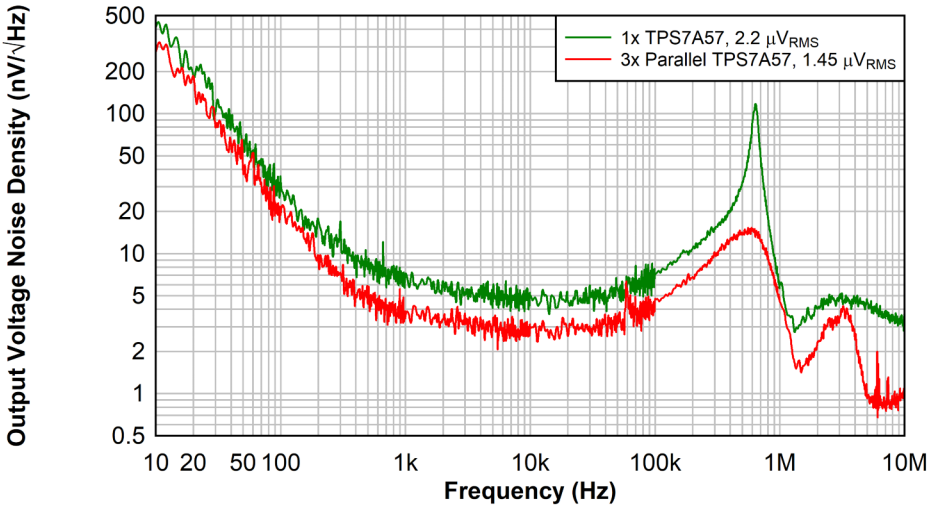
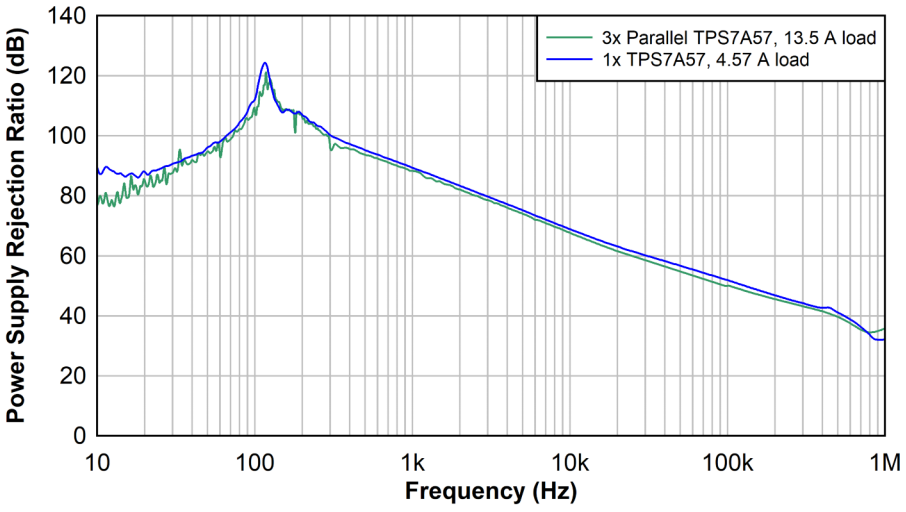


Figure 2-1. Output Voltage Noise Density vs. Frequency

2.2 PSRR

If the input voltage is held constant, then the PSRR of an LDO goes down as load current goes up. By paralleling LDOs the load current is shared among each LDO which raises the system PSRR when using the same input voltage. When LDOs are paralleled using ballast resistors, the only increase in power dissipation is the small loss contributed by the ballast resistance. To assess how many parallel LDOs are needed to meet the system requirements, first determine the PSRR required in the system. Then review the LDO data sheet to estimate how much current a single LDO can provide with your system's headroom while still meeting the system PSRR specification (I_{LDO_PSRR}). Finally, divide the total system load current, I_{LOAD}, by $I_{LDO_PSRR}$to obtain the number of parallel LDOs, *n*, required to meet the system PSRR specification.

$$n = \frac{I_{LOAD}}{I_{LDO\_PSRR}} \tag{2}$$



V_{IN}= 1.05 V, V_{OUT} = 0.75 V

Figure 2-2. PSRR vs. Frequency and I_{OUT} for 3x Parallel TPS7A57 and 1x Single TPS7A57

2.3 Specifications That Limit the Maximum LDO Current

The LDO output current is limited based on the dropout (or headroom) voltage, the junction temperature of the device, or the maximum rated current of the LDO. Here we provide the equations that determine how much

current an LDO can provide based on the available headroom and junction temperature. The actual LDO output current will be the minimum value of Equation 3, Equation 4 or I_{LDO_MAX}. This is used to set the minimum R_B.

2.3.1 Dropout (or Available Headroom Voltage)

An LDO requires a minimum amount of headroom voltage to properly regulate V_{OUT} and still provide the desired load current, however this headroom voltage is not always available. By paralleling LDO's we can spread the load across multiple LDO's and thus we can operate with less headroom. If we assume that the data sheets dropout vs I_{OUT} curve is linear, we can approximate the maximum current an LDO can provide to the load without entering dropout. The maximum current an LDO can provide is either Equation 3 or the full rated current I_{LDO_MAX} listed in the data sheet.

$$I_{LDO\_MAX\_DROPOUT\_LIM} = \left(\frac{V_{DROP}}{V_{IN} - V_{OUT}}\right) I_{LDO\_MAX} \tag{3}$$

2.3.2 Temperature

As load currents increase, the LDO power dissipation and junction temperature will rise. At elevated temperatures the LDO may enter thermal shutdown. By making some basic calculations using V_{IN}, V_{OUT}, the ambient temperature T_A, the maximum desired junction temperature T_J, and the thermal impedance T_{JA}, we can obtain a maximum current each LDO is allowed to provide. The maximum current an LDO can provide is either Equation 4 or the full rated current I_{LDO_MAX} listed in the data sheet.

$$I_{LDO\_MAX\_TEMP\_LIM} = \frac{\left(\frac{T_{J,max} - T_A}{T_{JA}}\right)}{(V_{IN} - V_{OUT})} \tag{4}$$

2.4 Load Current (I_{LOAD}) and Load Voltage (V_{LOAD})

The load voltage and load current analysis for parallel LDOs using ballast resistors is discussed in detail in [see reference 4]. To recap, the number of parallel LDO's required to provide the system load current I_{LOAD} is a function of the parameters in Equation 5 and Equation 6, or when V_{OUT} and R_B are identical for each LDO, Equation 7. Additional limitations exist on the available current per LDO as described in Specifications That Limit the Maximum LDO Current.

$$I_{OUT\_n} = \frac{V_{OUTn} - V_{LOAD}}{R_{Bn}} + \frac{V_{En}}{R_{Bn}} \tag{5}$$

$$I_{LOAD} = \sum_{n=1}^{n} \frac{V_{OUTn} - V_{LOAD} + V_{En}}{R_{Bn}} \tag{6}$$

$$I_{OUT\_n} = \frac{I_{LOAD} - \left(\sum_{n=1}^{n} \frac{V_{En}}{R_B}\right)}{n} + \frac{V_{En}}{R_B} \tag{7}$$

The number of parallel LDO's required to provide the system load voltage is a function of the parameters in Equation 8.

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{Bn}}} \tag{8}$$

Through some additional mathematics and worse case analysis we can derive the optimum ballast resistance needed to minimize the number of parallel LDO's required while simultaneously meeting the load current and load voltage requirements. The resulting formulas have been placed into an easy to use software tool available for download, see reference 5.

3 System V_{LOAD} and Current Sharing Simulation of Parallel LDOs using Ballast Resistors

After the designer has selected R_B and the number of parallel LDOs required using the down-loadable software tool [see reference 5], a system simulation can be performed to assess a statistical analysis of the current sharing and V_{LOAD}. The simulation can also provide a statistical assessment of the total DC accuracy of the system. Cadence for TI is an excellent resource for these simulations which we will use for these examples. A complete review and tutorial of Cadence for TI is beyond the scope of this white paper, if desired please see references 6 and 7 for additional guidance on this software simulator.

Consider the example parallel LDO system shown below in Figure 3-1 which is a screen image of the software tool. The load current is 8 A with 20 mV of allocated load regulation due to the additional ballast resistor. 4 m-ohms is the optimum ballast resistance and two parallel TPS7A57 LDOs are used to supply the total load current. The TPS7A57 reference voltage tolerance is ± 1% and the error voltage is ± 2 mV. Thus we expect an upper limit to be 759.5 mV. Including tolerance on V_{REF} and the 20 mV of additional load regulation, we expect a minimum voltage of 722.5 mV. In all cases the output current of each LDO should remain below 5 A.

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A57

LDO Specifications				
Parameter	Value	Units	Optional User Entry	Units
V_E, high	2	mVdc		mVdc
V_E, low	-2	mVdc		mVdc
Thermal Impedance T_{JA}	21.9	°C / W		°C / W

Parallel LDO System Requirements				
Parameter	Value	Units		
T_A	25	°C	25	°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	1.25	Vdc		Vdc
V_{OUT}	0.75	Vdc		Vdc
Allowable load regulation	0.02	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	2.45	µVrms		µVrms
Total System Load:	8	A	8	A
Minimum Ballast Resistance needed	0.8	mΩ		
Optimum Ballast Resistance	3.94356	mΩ		
Ballast Resistance Selected	4	mΩ	4	mΩ
	N =			
Minimum number of parallel LDO's required:	2			

Figure 3-1. Parallel LDO Worst Case Analysis using 2x TPS7A57

Figure 3-2 shows how to model this system in PSpice. We apply voltage sources to model the output voltage (V15) and the error voltages of each LDO (V13 and V14). We use standard resistors for the ballast resistor (Rb1 and Rb2) and a constant current source for the load current (I27).

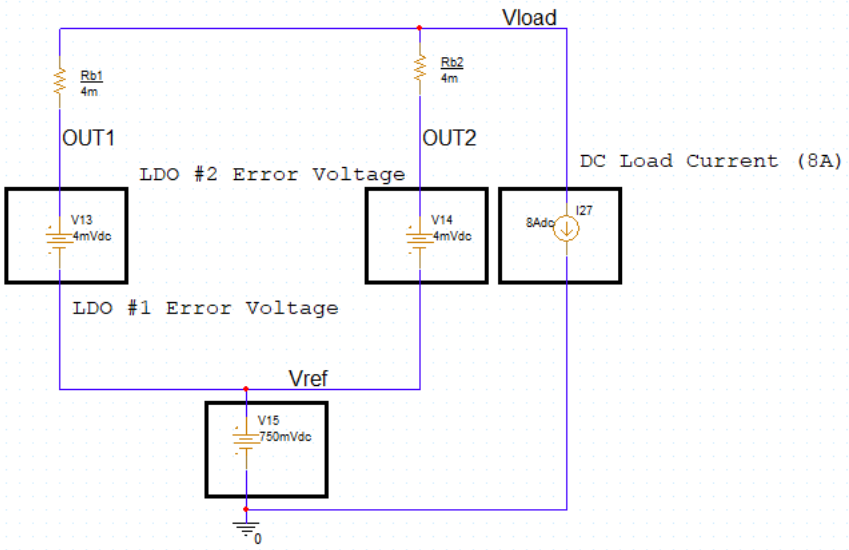


Figure 3-2. Spice Simulation Schematic of Two Parallel LDOs

Unfortunately, traditional spice models cannot apply a tolerance to voltage sources or current sources, so we must modify this simulation model. We divide our component tolerances by 6 in the Spice model as typically at least 6 standard deviations will fit in the manufacturer tolerance specification. Limit functions are used to prevent the tails of the Gaussian distribution from exceeding limits which would cause the components to be screened out during manufacturer production. Finally, 1% tolerance resistors are used for the ballast resistance.

A modified model to simulate the maximum I_{OUTn} should keep I_{LOAD} at its maximum value while placing tolerances on all other components in the simulation (Figure 3-3). To be clear, I_{LOAD} = 8 A during the monte carlo simulation. The simulation results for I_{OUT1} and I_{OUT2} are provided in Figure 3-2 and Figure 3-2. A summary of these results against the design requirements are provided in Table 3-1.

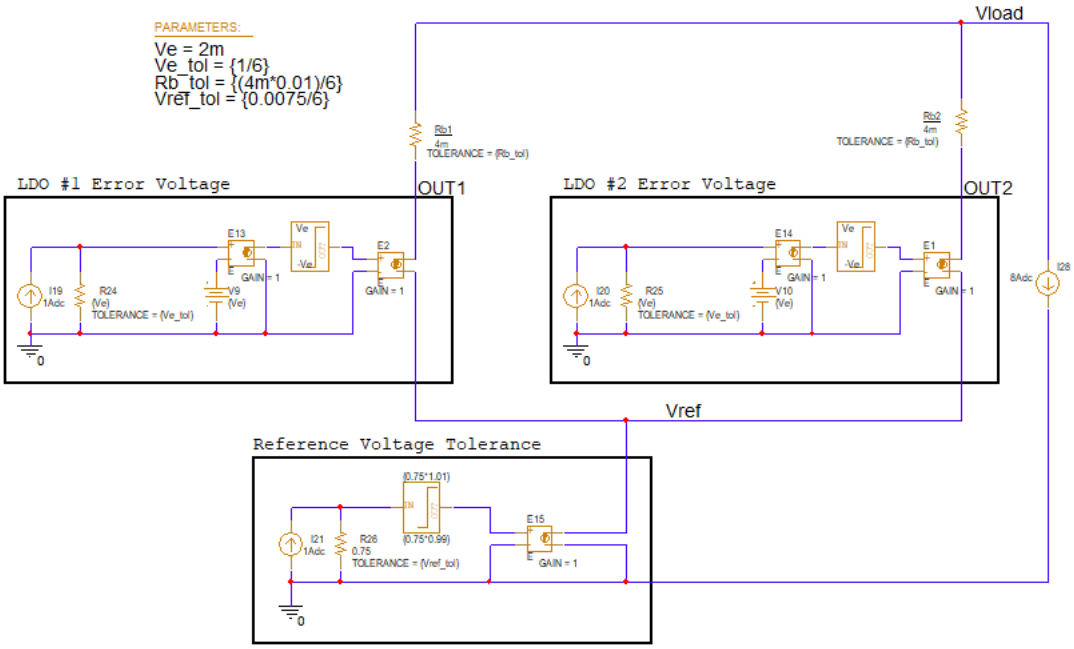


Figure 3-3. Modified PSpice Schematic to Simulate the I_{OUTn} Distribution of Two Parallel LDOs

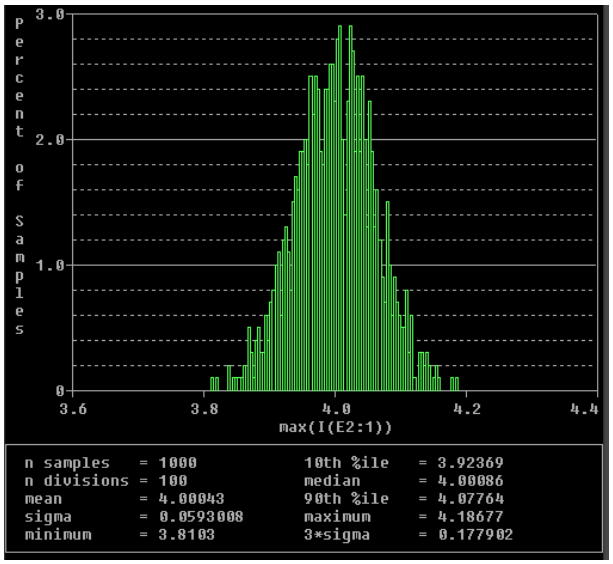


Figure 3-4. I_{OUT1} Simulation Results

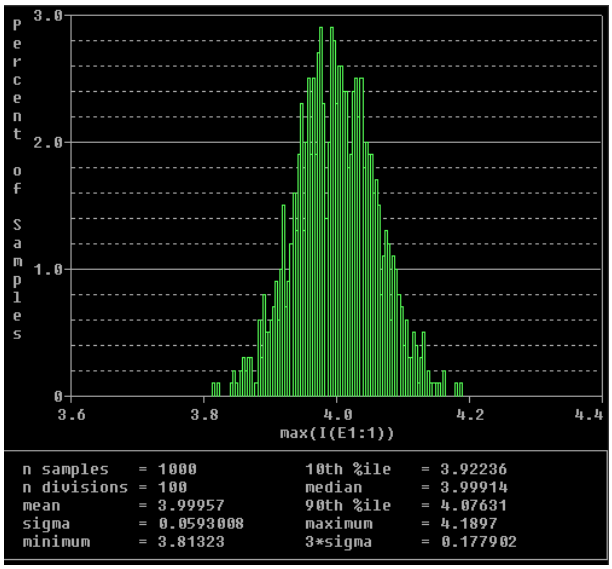


Figure 3-5. I_{OUT2} Simulation Results

Table 3-1. I_{OUTn} Monte Carlo Simulation with I_{LOAD} = 8 A

Parameter	Median Value	Sigma	Statistical Results (+/- 6 sigma)	Requirement(1)
I_{OUT1}	4.00086 A	59.3 mA	4.360 A / 3.645 A	<= 5 A
I_{OUT2}	3.99914 A	59.3 mA	4.355 A / 3.643 A	<= 5 A

(1) I_{OUTn} must not enter current limit, thus the requirement for the TPS7A57 is 5 A or less.

A modified model to simulate V_{LOAD} will include all tolerances as well as the full range of I_{LOAD} (Figure 3-2). The simulation results for V_{LOAD} is provided in Figure 3-2 and a summary of these results against the design DC accuracy specification is provided in Table 3-2.

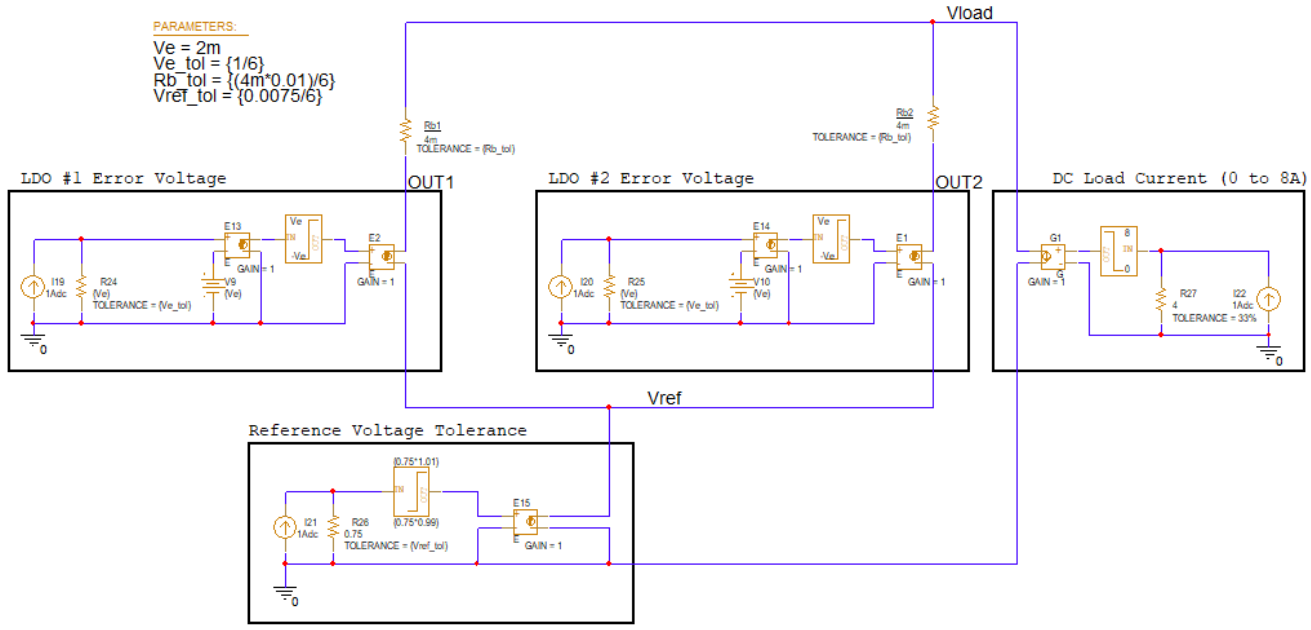


Figure 3-6. Modified PSpice Schematic to Simulate the V_{LOAD} Distribution of Two Parallel LDOs

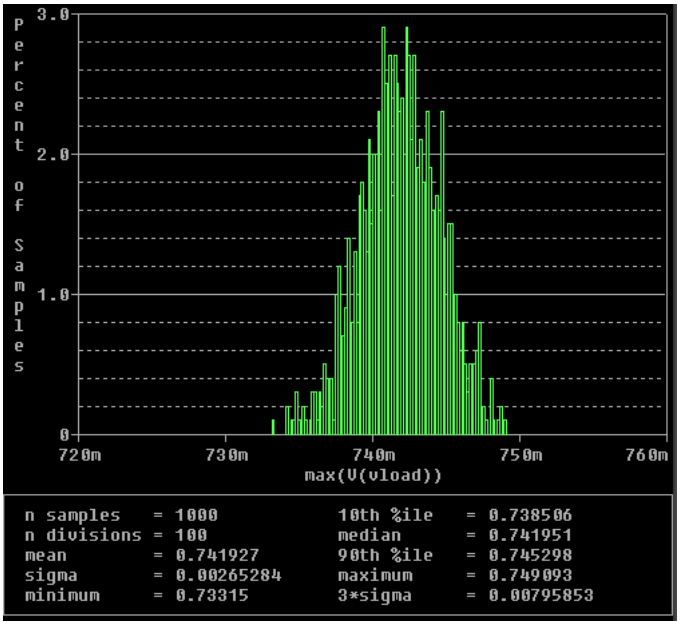


Figure 3-7. V_{LOAD} Simulation Results

The worst case limits are the minimum and maximum V_{LOAD} as calculated from V_{REF}, the error voltage and the increase in load regulation due to the ballast resistors. When I_{LOAD} = 0 A, V_{LOAD} can be as high as 0.75 V × 1.01 + 2 mV = 759.5 mV. When I_{LOAD} = 8 A, V_{LOAD} can be as low as 0.75 V × 0.99 - 20 mV = 722.5 mV. The software tool performs a worst case analysis which includes the 2 mV error voltage on the 20 mV load regulation system specification. Thus, we do not need to subtract another 2 mV from 722.5 mV.

In this example, the worst case limits are outside of the ± 6 sigma statistical results. For designs where V_{LOAD} has a tight tolerance requirement, it is common to set the DC accuracy to be 742.05 mV ± 15.95 mV (which is the same as 742.05 mV ± 2.15%). The extra +1.5 mV / - 3.6 mV can be reallocated to another system specification such as load transient or line transient analysis.

Table 3-2. V_{LOAD} DC Accuracy versus the System Specification

Parameter	Median Value	Sigma	Statistical Results (± 6 sigma)	Worst Case Limits
V_{LOAD}	742 mV	2.653 mV	758 mV / 726.1 mV	< 759.5 mV and > 722.5 mV

4 Examples

4.1 TPS7A94

Consider the following system power requirements: V_{IN} = 5 V, V_{OUT} = 4 V, and I_{LOAD} = 2.5 A. The system noise requirement is 0.275 uV_{RMS}, we need the PSRR to be at least 10 dB at 1 MHz, and the additional load regulation can be as high as 40 mV. We select the TPS7A94 LDO to be paralleled to meet the ultra low noise system specification. We enter these system requirements into the system architecture calculator [see reference 5]. As shown in Figure 4-1 we need at least 3 parallel TPS7A94 LDOs to meet these system requirements.

These results do not include PSRR, which must be assessed separately. A review of the TPS7A94 data sheet reveals plenty of margin in the PSRR curves to the system 10 dB requirement at 1 MHz. Thus the PSRR specification will not change the results in Figure 4-1. If desired, a statistical analysis on V_{LOAD} and I_{OUTn} can be completed as discussed in Section 3.

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A94				
LDO Specifications				
Parameter	Value	Units	Optional User Entry	Units
V_E, high	2	mVdc		mVdc
V_E, low	-2	mVdc		mVdc
Thermal Impedance T_{JA}	46.1	°C / W		°C / W
Parallel LDO System Requirements				
Parameter	Value	Units		
T_A	25	°C		°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	5	Vdc		Vdc
V_{OUT}	4	Vdc		Vdc
Allowable load regulation	0.04	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	0.275	µVrms	0.275	µVrms
Total System Load:	2.5	A		A
Minimum Ballast Resistance needed	4	mΩ		
Optimum Ballast Resistance	40.49872	mΩ		
Ballast Resistance Selected	40.49872	mΩ		mΩ
	N =			
Minimum number of parallel LDO's required:	3			

Figure 4-1. Parallel LDO System Requirement Analysis using the TPS7A94 LDO

4.2 TPS7A47xx

Consider the following system power requirements: V_{IN} = 15 V, V_{OUT} = 12 V, and I_{LOAD} = 2.5 A. The system noise requirement is 4.67 uV_{RMS}, we need the PSRR to be at least 50 dB at 1 MHz, and the additional load regulation can be as high as 60 mV. The application requires high reliability and may operate above 125 C in the future, so an extended performance (-EP) device with an operating junction temperature of 150 C is desired. We select the TPS7A47 LDO to be paralleled to meet the mid Vin, high reliability and increased thermal specifications. We enter these system requirements into the system architecture calculator [see reference 5]. As shown in Figure 4-2 we need at least 3 parallel TPS7A47 LDOs to meet these system requirements.

These results do not include PSRR, which must be assessed separately. A review of the TPS7A47 data sheet reveals plenty of margin in the PSRR curves to the system 50 dB requirement at 1 MHz. Thus the PSRR specification will not change the results in Figure 4-2. If desired, a statistical analysis on V_{LOAD} and I_{OUTn} can be completed as discussed in Section 3.

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A47xx				
LDO Specifications				
Parameter	Value	Units	Optional User Entry	Units
V_E, high	4	mVdc		mVdc
V_E, low	-4	mVdc		mVdc
Thermal Impedance T_{JA}	32.5	°C / W		°C / W
Parallel LDO System Requirements				
Parameter	Value	Units		
T_A	25	°C		°C
Maximum T_J per LDO	150	°C	150	°C
V_{IN}	15	Vdc		Vdc
V_{OUT}	12	Vdc		Vdc
Allowable load regulation	0.06	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	4.67	µVrms		µVrms
Total System Load:	2.5	A		A
Minimum Ballast Resistance needed	8	mΩ		
Optimum Ballast Resistance	61.06544	mΩ		
Ballast Resistance Selected	61.06544	mΩ		mΩ
	N =			
Minimum number of parallel LDO's required:	3			

Figure 4-2. Parallel LDO System Requirement Analysis using the TPS7A47 LDO

4.3 TPS7A57

Consider the following system power requirements: V_{IN} = 1.2 V, V_{OUT} = 0.9 V, I_{LOAD} = 13.5 A, and the ambient temperature is 85 C. The system noise requirement is 2.45 uV_{RMS}, we need the PSRR to be at least 45 dB at 500 kHz, and the additional load regulation can be as high as 20 mV. We select the TPS7A57 LDO to be paralleled to meet the high load current specification. We enter these system requirements into the system architecture calculator [reference 5]. As shown in Figure 4-3 we need at least 4 parallel TPS7A57 LDOs to meet these system requirements.

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A57				
LDO Specifications				
Parameter	Value	Units	Optional User Entry	Units
V_E, high	2	mVdc		mVdc
V_E, low	-2	mVdc		mVdc
Thermal Impedance T_{JA}	21.9	°C / W		°C / W
Parallel LDO System Requirements				
Parameter	Value	Units		
T_A	85	°C		°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	1.2	Vdc	1.2	Vdc
V_{OUT}	0.9	Vdc	0.9	Vdc
Allowable load regulation	0.02	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	2.45	µVrms		µVrms
Total System Load:	13.5	A		A
Minimum Ballast Resistance needed	0.8	mΩ		
Optimum Ballast Resistance	4.142507	mΩ		
Ballast Resistance Selected	4	mΩ	4	mΩ
	N =			
Minimum number of parallel LDO's required:	4			

Figure 4-3. Parallel LDO System Requirement Analysis using the TPS7A57 LDO

These results do not include PSRR, which must be assessed separately. Upon review of the TPS7A57 data sheet Figure 6-6 (repeated below in Figure 4-3), we must limit the average LDO current to be 4 A maximum to meet the PSRR specification. Thus we need at least 13.5 A / 4 A = 3.375 LDOs or 4 LDOs to meet the PSRR requirement. This is the same result as the number of parallel LDOs needed to meet the other system requirements, therefore the PSRR specification will not change the results in Figure 4-3. If desired, a statistical analysis on V_{LOAD} and I_{OUTn} can be completed as discussed in Section 3.

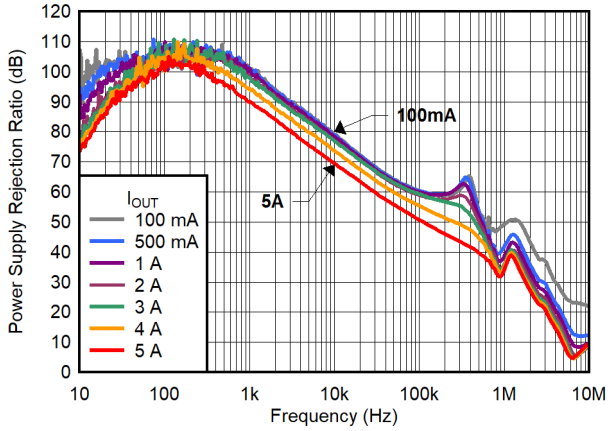


Figure 4-4. TPS7A57 PSRR vs Frequency and I_{OUT} for CP Enabled, No Bias

5 References

1. Texas Instruments, *TPS7A57 5-A, Low-VIN (0.7 V), Low-Noise (2.1μV_{RMS}), High-Accuracy (1%), Ultra-Low Dropout (LDO) Voltage Regulator*, data sheet
2. *Texas Instruments, "TPS7A4701-EP 36-V, 1-A, 4 μV_{RMS}, RF LDO Voltage Regulator*, data sheet
3. Texas Instruments, *5-A, low-input-voltage, low-noise, high-accuracy low-dropout (LDO) voltage regulator*
4. Texas Instruments, *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors*, white paper
5. Texas Instruments, *Parallel Low-Dropout (LDO) Calculator*
6. *Cadence website*
7. Texas Instruments, *PSPICE-FOR-TI* website

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