Functional Safety Information

TPS746-Q1 Functional Safety FIT Rate, FMD and Pin FMEA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS746-Q1 (DRV and DRB packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the adjustable version with open-drain, power-good functional block diagram for reference.

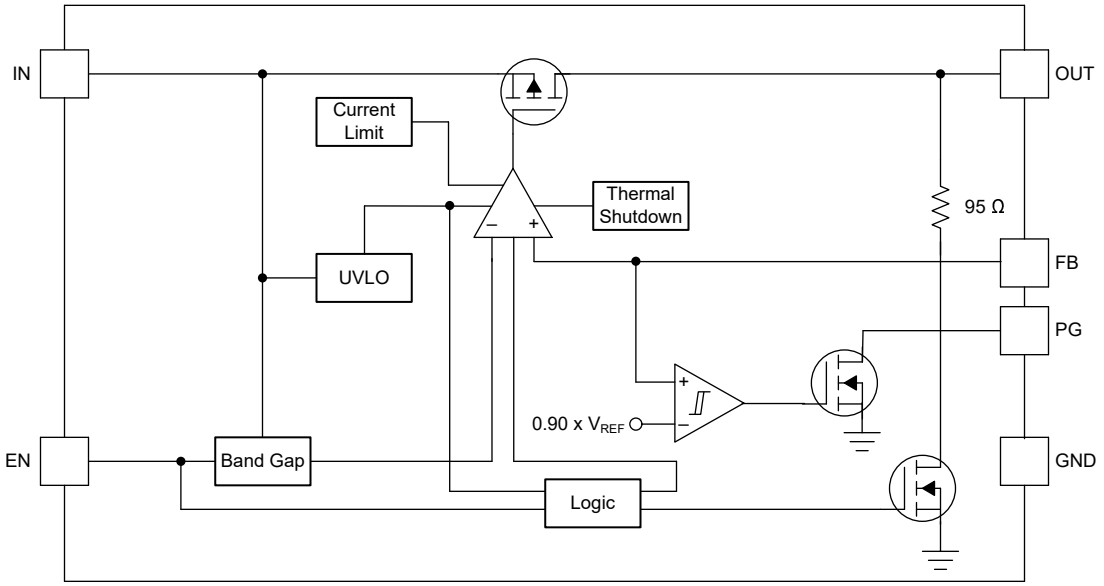

Figure 1-1. Adjustable Version With Open-Drain Power-Good

Figure 1-2 shows the adjustable version with push-pull, power-good functional block diagram for reference.

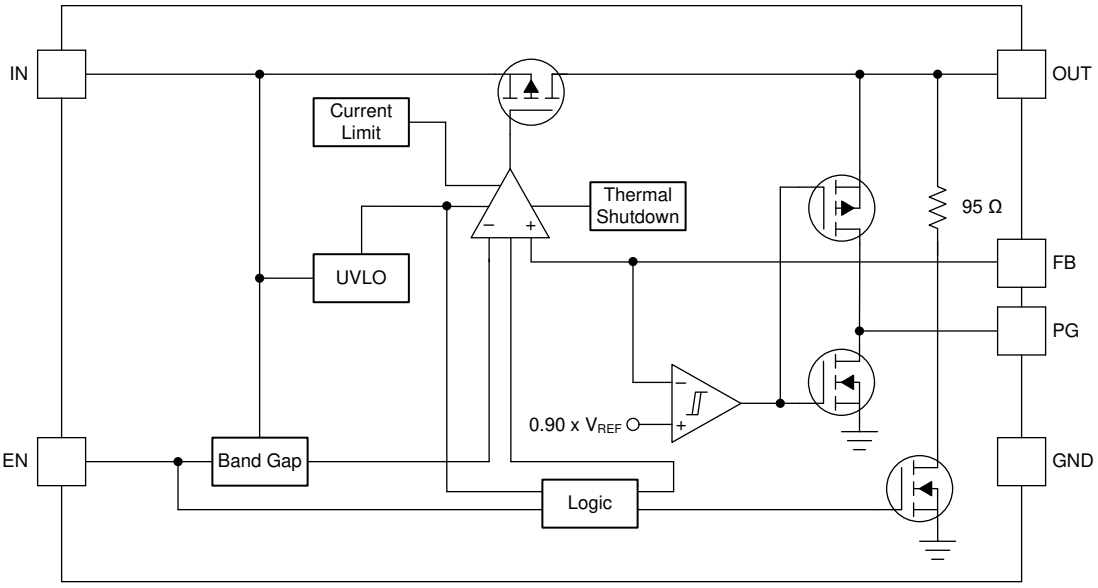

Figure 1-2. Adjustable Version With Push-Pull Power-Good

Figure 1-3 shows the fixed voltage version with open-drain, power-good functional block diagram for reference.

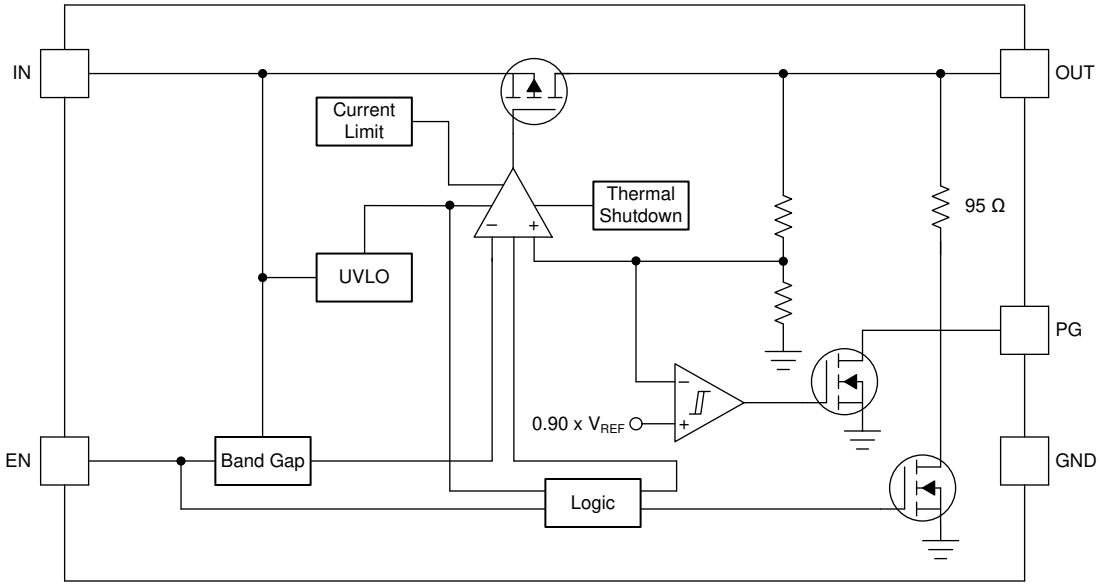

Figure 1-3. Fixed Voltage Version With Open-Drain Power-Good

Figure 1-4 shows the fixed voltage version with push-pull, power-good functional block diagram for reference.

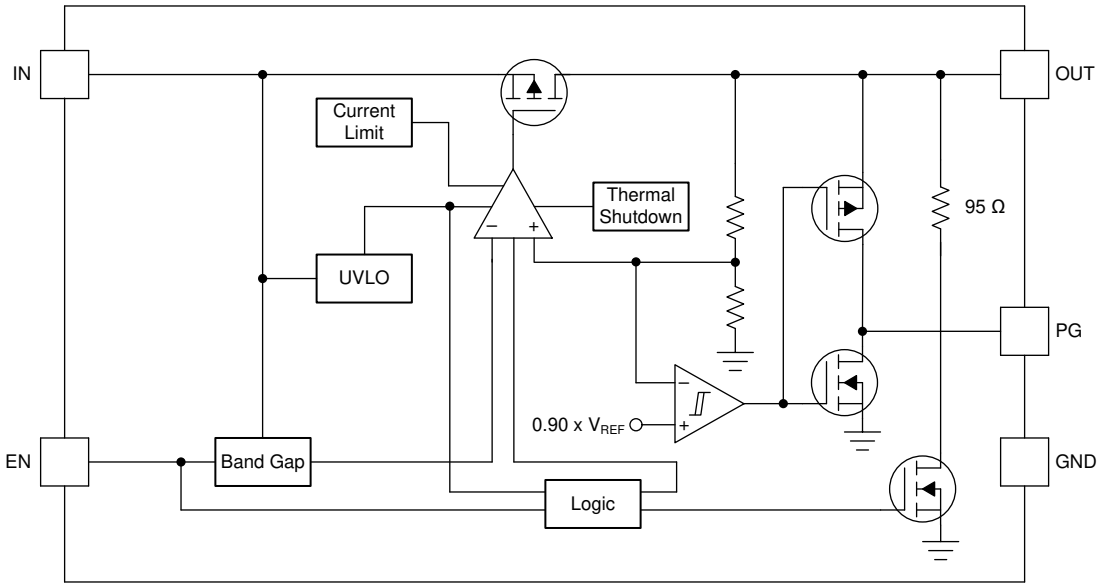

Figure 1-4. Fixed Voltage Version With Push-Pull Power-Good

The TPS746-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DRV Package

This section provides functional safety failure in time (FIT) rates for the DRV package of the TPS746-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	5
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 350 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DRB Package

This section provides functional safety failure in time (FIT) rates for the DRB package of the TPS746-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 350 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS746-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN}).	15%
V_{OUT} not in specification (voltage or timing).	60%
V_{OUT} low (no output).	15%
PG false trigger, fails to trigger.	5%
Short circuit any two pins.	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS746-Q1 (DRV and DRB packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 DRV Package

Figure 4-1 and Figure 4-2 show the TPS746-Q1 pin diagram (adjustable and fixed) for the DRV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS746-Q1 data sheet.

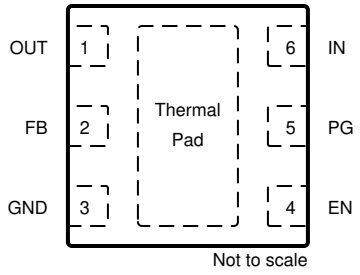

Figure 4-1. Pin Diagram (Adjustable TPS746-Q1 DRV Package)

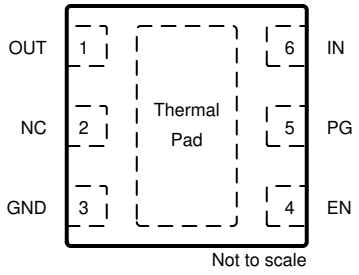

Figure 4-2. Pin Diagram (Fixed TPS746-Q1 DRV Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	The output voltage is near or at ground. The device enters current limit. The device may cycle in and out of thermal shutdown depending on power dissipation.	B
FB/NC	2	(Adjustable output.) The device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass transistor is driven on as hard as possible. (Fixed output.) No effect.	B, D
GND	3	—	D
EN	4	The device turns off.	B
PG	5	The PG function does not work.	D
IN	6	No output voltage. Input supply can be 0 V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage is disconnected from the load.	B
FB/NC	2	(Adjustable output.) Error amplifier input is left floating, output voltage is not equal to set voltage. (Fixed output.) No effect.	B, D
GND	3	The device may be disabled.	B
EN	4	The device may be disabled.	B
PG	5	The PG function does not work.	D
IN	6	No output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Short to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	FB/NC (pin 2)	(Adjustable output.) V_{OUT} is set to V_{FB} = 0.55 V. (Fixed output.) No effect.	B, D
FB/NC	2	GND (pin 3)	(Adjustable output.) The device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass transistor is driven on as hard as possible. (Fixed output.) No effect.	B, D
GND	3	EN (pin 4)	The output is forced off, V_{OUT} is 0 V.	B
EN	4	PG (pin 5)	The device stays off.	B
PG	5	IN (pin 6)	The PG function does not work.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	The output is not regulated. $V_{OUT} = V_{IN}$.	B
FB/NC	2	(Adjustable output.) The FB pin is damaged if V_{IN} is higher than 2 V. (Fixed output.) No effect.	A, D
GND	3	No output voltage. Either input supply is at 0 V, or the input fuse is blown.	B
EN	4	The output is forced on regardless of the enable signal.	B
PG	5	The PG function does not work.	D
IN	6	No effect.	D

4.2 DRB Package

Figure 4-3 and Figure 4-4 show the TPS746-Q1 pin diagram (adjustable and fixed) for the DRB package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS746-Q1 data sheet.

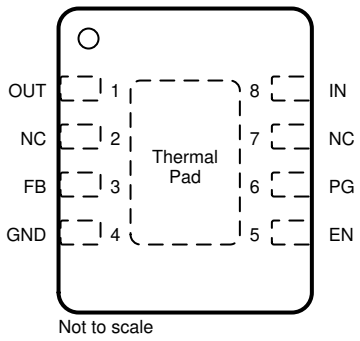

Figure 4-3. Pin Diagram (Adjustable TPS746-Q1 DRB Package)

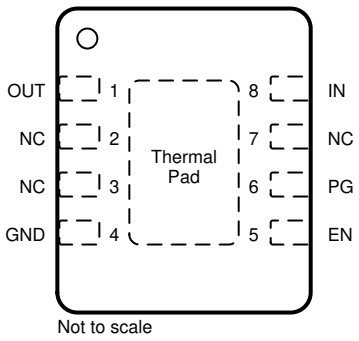

Figure 4-4. Pin Diagram (Fixed TPS746-Q1 DRB Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	The output voltage is near or at ground. The device enters current limit. The device may cycle in and out of thermal shutdown depending on power dissipation.	B
NC	2	Improved thermal performance.	D
FB/NC	3	(Adjustable output.) The device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass transistor is driven on as hard as possible. (Fixed output.) No effect.	B, D
GND	4	—	D
EN	5	The device turns off.	B
PG	6	The PG function does not work.	D
NC	7	Improved thermal performance.	D
IN	8	No output voltage.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage is disconnected from the load.	B
NC	2	No effect.	D
FB/NC	3	(Adjustable output.) The error amplifier input is left floating, the output voltage is not equal to set voltage. (Fixed output.) No effect.	B, D
GND	4	The device may be disabled.	B
EN	5	The device may be disabled.	B
PG	6	The PG function does not work.	D
NC	2	No effect.	D
IN	8	No output voltage.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Short to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	NC (pin 2)	Reduced thermal performance.	D
NC	2	FB/NC (pin 3)	No effect.	D
FB/NC	3	GND (pin 4)	(Adjustable output.) The device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass transistor is always on. (Fixed output.) No effect.	B/D
GND	4	EN (pin 5)	The output is forced off, V_{OUT} is 0 V.	B
EN	5	PG (pin 6)	The device stays off.	B
PG	6	NC (pin 7)	No effect.	D
NC	7	IN (pin 8)	Reduced thermal performance.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	The output is not regulated. $V_{OUT} = V_{IN}$.	B
NC	2	No effect.	D
FB/NC	3	(Adjustable output.) The FB pin is damaged if V_{IN} is higher than 2 V. (Fixed output.) No effect.	A, D
GND	4	No output voltage. Either input supply is at 0 V, or input fuse is blown.	B
EN	5	The output is forced on regardless of enable signal.	B
PG	6	The PG function does not work.	D
NC	7	No effect.	D
IN	8	No effect.	D

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