Functional Safety Information

TPS3850-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS3850-Q1 (VSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

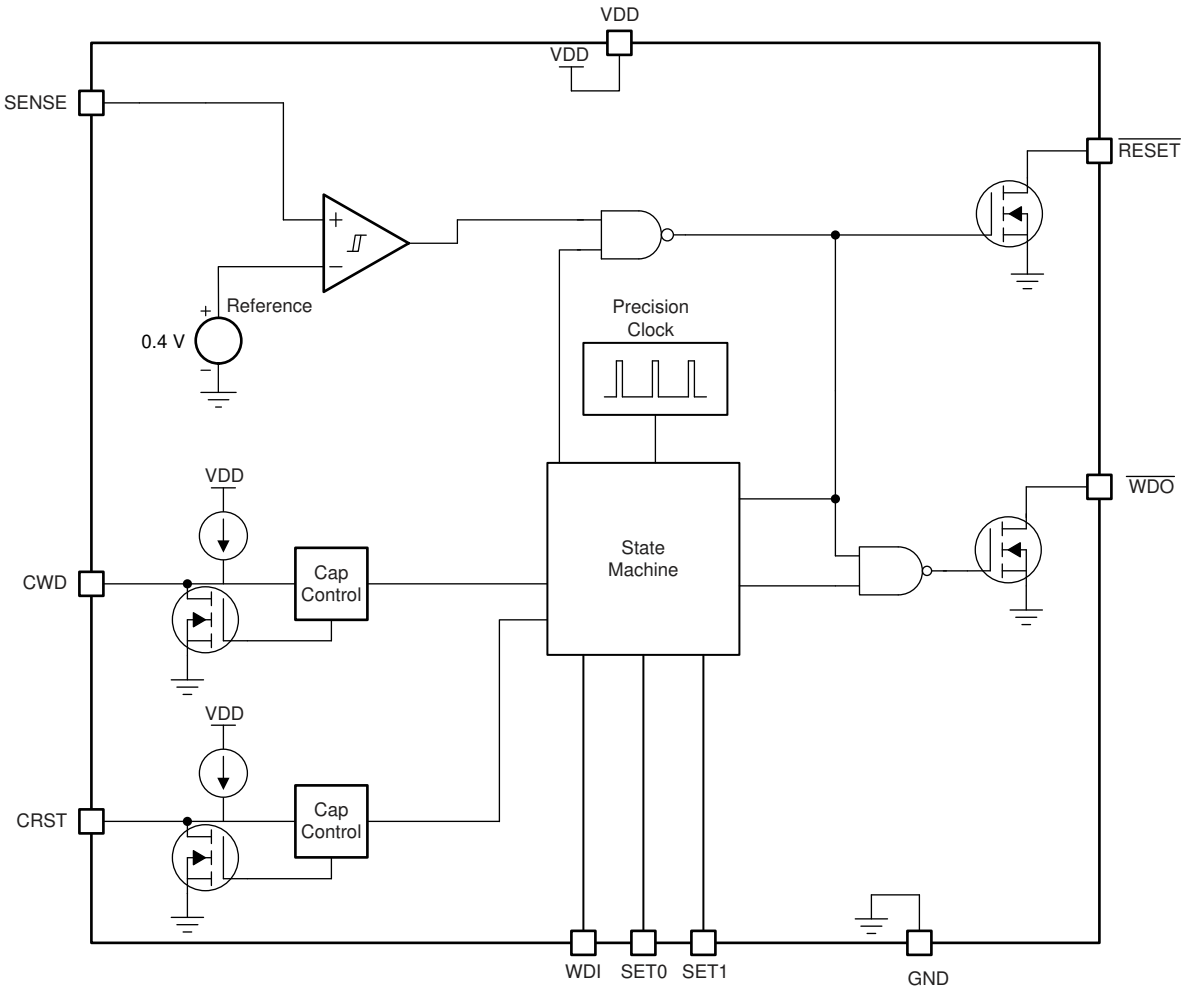

Figure 1-1. Functional Block Diagram

TPS3850-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the VSON package of TPS3850-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.0 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3850-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
$\overline{\text{RESET}}$ (or $\overline{\text{WDO}}$) fails to trip	10%
$\overline{\text{RESET}}$ (or $\overline{\text{WDO}}$) false trip	10%
$\overline{\text{RESET}}$ trip outside specification (voltage or time)	30%
$\overline{\text{WDO}}$ trip outside specification (voltage or time)	50%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3850-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDD = 3.3 V
- SENSE = 5 V
- RESET pulled-up to VDD unless stated otherwise

Figure 4-1 shows the TPS3850-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS3850-Q1 data sheet.

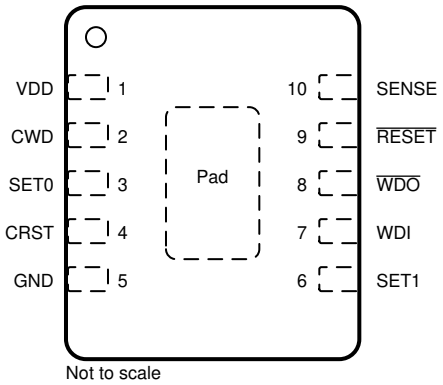

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No device damage, but loss of functionality	B
CWD	2	No damage to device, but this is an undefined operating condition. $\overline{\text{WDO}}$ tends to be high	C
SET0	3	No damage to device, but this is an undefined operating condition	C
CRST	4	No damage to device, but this is an undefined operating condition. $\overline{\text{RESET}}$ tends to be low	C
GND	5	Normal Operation	D
SET1	6	No damage to device, but this is an undefined operating condition	C
WDI	7	No damage to device, but this is an undefined operating condition. Watchdog functionality may not be available	B
$\overline{\text{WDO}}$	8	No damage to device, but this is an undefined operating condition. Watchdog functionality may not be available	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ pin is always asserted low.	D
SENSE	10	$\overline{\text{RESET}}$ pin is always asserted low.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device will not function	B
CWD	2	Sets watchdog timeout to factory programmed 1.6 seconds	C
SET0	3	SET0 logic is undefined and the watchdog configuration is undefined	C
CRST	4	Configures reset delay to the "NC" value, see the Timing Requirements Table 6.6	C
GND	5	Device will not function	B
SET1	6	SET1 logic is undefined and the watchdog configuration is undefined	C
WDI	7	$\overline{\text{WDO}}$ will continuously trigger when the watchdog timeout expires if the watchdog is enabled	C
$\overline{\text{WDO}}$	8	Open-drain output requires pull-up resistor to function, $\overline{\text{WDO}}$ will always be logic low	C
$\overline{\text{RESET}}$	9	Open-drain output requires pull-up resistor to function, $\overline{\text{RESET}}$ will be logic low	C
SENSE	10	$\overline{\text{RESET}}$ (Output) will be "low", $\overline{\text{WDO}}$ is high impedance state	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	CWD	Potential device damage that affects functionality	A
CWD	2	SET0	Watchdog timeout and configuration undefined	C
SET0	3	CRST	Reset delay and watchdog configuration undefined. Device will not function correctly	C
CRST	4	GND	$\overline{\text{RESET}}$ (Output) will be low and device will not function	B
GND	5	SET1	Normal operation, configures SET1 pin as "low" and configures the watchdog. See datasheet for configuration information.	C
SET1	6	WDI	Watchdog configuration is undefined, $\overline{\text{WDO}}$ will continuously trigger when the watchdog timeout expires if the watchdog is enabled	C
WDI	7	$\overline{\text{WDO}}$	$\overline{\text{WDO}}$ will continuously trigger when the watchdog timeout expires if the watchdog is enabled	C
$\overline{\text{WDO}}$	8	$\overline{\text{RESET}}$	Normal operation, $\overline{\text{WDO}}$ and $\overline{\text{RESET}}$ logically OR together so that if a watchdog or reset fault occurs, the common output will trigger	C
$\overline{\text{RESET}}$	9	SENSE	$\overline{\text{RESET}}$ (Output) will be "low", $\overline{\text{WDO}}$ is high impedance state	C
SENSE	10	VDD	Normal operation, VDD is monitored via the SENSE pin	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Normal	D
CWD	2	Potential device damage that affects functionality	A
SET0	3	Normal operation, configures SET0 to logic high	C
CRST	4	Not recommend because of excess current draw, User should use a resistor from CRST to VDD if selecting this reset delay timing option	A
GND	5	Device will not function	B
SET1	6	Normal operation, configures SET0 to logic high	C
WDI	7	$\overline{\text{WDO}}$ will continuously trigger when the watchdog timeout expires if the watchdog is enabled	C
$\overline{\text{WDO}}$	8	Open-drain output requires a pull-up resistor, I_WDO ABS MAX may be violated if a watchdog fault occurs and the internal FET turns on shorting GND to VDD	A
$\overline{\text{RESET}}$	9	Open-drain output requires a pull-up resistor, I_RESET ABS MAX may be violated if a watchdog fault occurs and the internal FET turns on shorting GND to VDD	A
SENSE	10	Normal operation, VDD is monitored via the SENSE pin	C

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265