Application Report
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UCC25230 Bias Power-Supply Design Review

Hong Huang
Power Management Products

ABSTRACT

This application report reviews the design steps used in the evaluation module (EVM) UCC25230EVM-754. The EVM helps evaluate the UCC25230 pulse-width modulation (PWM) controller in a forward-flyback, or Flybuck™, dc-dc converter topology for a 48-V telecom bias supply. The EVM is a dual-output converter with 1500-VDC isolation between the two outputs. Each output is typically rated as 12 V and 65 mA, for a total output power of 1.5 W.

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1 Design Specifications

Table 1 shows the specifications for the EVM, UCC25230EVM-754.

Table 1. EVM Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
VIN	Input voltage		36	48	72	VDC
IIN	Input current	VIN = 36 V, IOUT = max		65		mA
OUTPUT CHARACTERISTICS						
VOUT1	Output voltage primary	VIN = typ, IOUT = max		12		VDC
VOUT2	Output voltage secondary	VIN = typ, IOUT = max		12		VDC
	Output voltage ripple	VIN = typ, IOUT = max			50	mV_{PP}
IOUT1	Output current primary	VIN = min to max			65	mA
IOUT2	Output current secondary	VIN = min to max			65	mA
	Output power				1.5	W
SYSTEMS CHARACTERSTICS						
f_{SW}	Switching frequency			380		kHz
η	Full-load efficiency	VIN = typ, IOUT = max		80		%
	Isolation level	Primary side to secondary side	1.5			kVDC

2 Design Considerations

The design-targeted application is an auxiliary (bias) supply in 48-V telecom modular designs with isolation of 1500 VDC between the primary and secondary side. The application requires a small footprint and low profile. Traditionally, a low-dropout regulator (LDO) is used to initially bias the primary-side controller. After start-up, the bias is substituted with an auxiliary winding on the main transformer during normal operation. Secondary-side control has recently become more desirable because of the advantages it offers, such as the fast control-loop response (after eliminating the need of the optocoupler) and digital control with communication. Thus, the initial simple LDO bias solution becomes insufficient. In such cases, an independent bias power supply is required.

There are several factors regarding achievable performance when making trade-offs (for example, efficiency and energy losses, transient response, board space, cost, as well as design convenience and consistency). Detailed analysis and comparison are not the purpose of this application report; because increasingly more 48-V telecom modular designs prefer to have an independent bias power supply, the details described in this report are required when using the UCC25230. Figure 1 shows the proposed schematics for the design based on the UCC25230 data sheet.

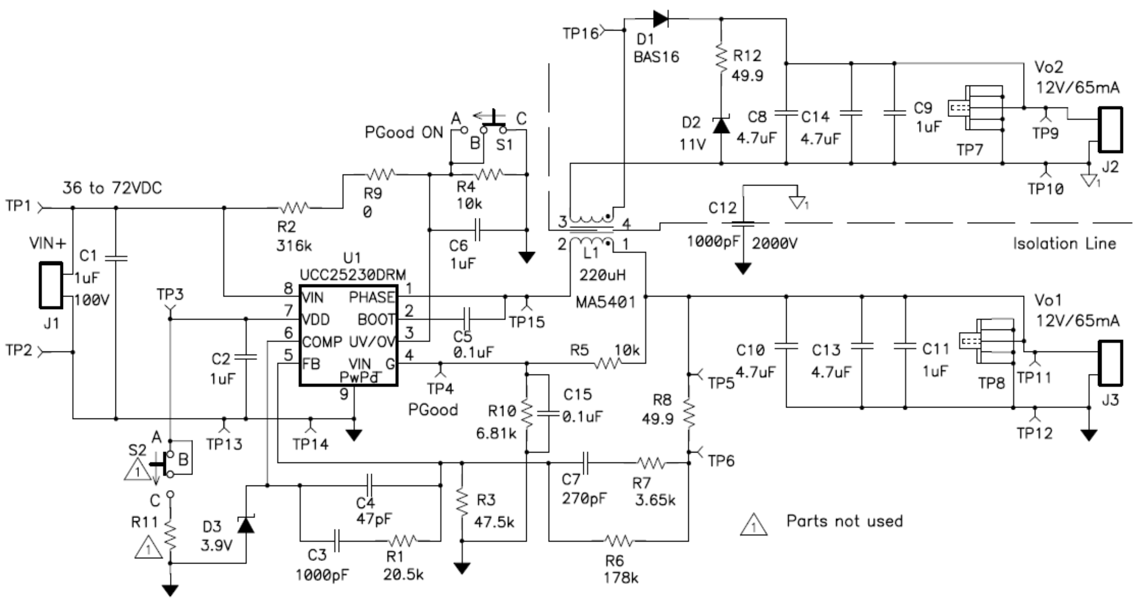

Figure 1. EVM Schematics

3 Design Steps

3.1 Power-Stage Design

Two main parameters of the power stage are primary inductance and output filter capacitance because the converter main switches are integrated inside the device. Determining the primary inductance and filter capacitance are described in this section.

3.1.1 Determining the Primary Inductance

3.1.1.1 Step 1: Inductance Calculation

To maximize device capability, the design is made a bit differently from traditional procedures. The design is made to maximize the ripple current and minimize the inductance while keeping the average current in accordance with the specified 220 mA in the UCC25230 data sheet. It is important to design an acceptable minimal inductance in order to get the optimal physical inductor with a low profile and small footprint. The primary inductance design is based on Equation 1:

$$L_{PRI} = \frac{V_O \times (1 - D_{MIN})}{(2 \times \Delta\% \times I_{PRI}) \times f_{SW}} = \frac{V_O \times \left(1 - \frac{V_O}{V_{IN\_MAX}}\right)}{I_{PK\_PK} \times f_{SW}} \quad (1)$$

In Equation 1, I_{PRI} is the maximum average current that is obtained from the total current of both the primary and secondary load currents (assuming that the windings are ideally coupled).

In our design, I_{PRI} = 65 mA × 2 = 130 mA. Because the maximum peak current allowed is 220 mA, the peak-to-peak current can be determined as Equation 2:

$$I_{PK\_PK} = 2 \times (220\text{ mA} - 130\text{ mA}) = 180\text{ mA} \quad (2)$$

Because the switching frequency is fixed at 380 kHz, V_O = 12 V, and V_{IN_MAX} = 72 V, the minimum primary-side inductance can then be determined as Equation 3:

$$L_{PRI} = \frac{V_O \times \left(1 - \frac{V_O}{V_{IN\_MAX}}\right)}{I_{PK\_PK} \times f_{SW}} = \frac{12\text{ V} \times \left(1 - \frac{12\text{ V}}{72\text{ V}}\right)}{0.18\text{ A} \times 380 \times 10^3\text{ Hz}} = 146.2\ \mu\text{H} \Rightarrow 150\ \mu\text{H} \quad (3)$$

Note that the minimum inductance of 150 µH is the inductance achievable at 220 mA, not the inductance at a no-load condition.

3.1.1.2 Step 2: Turns-Ratio Calculation

For a coupled inductor, the turns-ratio is determined by Equation 4:

$$N_L = \frac{VOUT2}{VOUT1} = \frac{12\text{ V}}{12\text{ V}} = 1 \quad (4)$$

An example of a physical inductor that meets these design results with 1500 VDC isolation is available from Coilcraft™, part number MA5401-AE.

3.1.2 Determining the Output Filter Capacitance

To determine the output filter capacitors, Equation 5 provides a basis:

$$C_{OUT} = \frac{\Delta T}{\frac{\Delta V}{\Delta I} - ESR} = \frac{D_{MAX} \times \frac{1}{f_{SW}}}{\frac{V_{RIPPLE}}{50\% \times I_{PRI}} - ESR} = \frac{\frac{V_O}{V_{IN\_MIN}} \times \frac{1}{f_{SW}}}{\frac{V_{RIPPLE}}{50\% \times I_{PRI}} - ESR} \quad (5)$$

In our intended application, X7R or X5R multilayer ceramic capacitors are typically used. These capacitors (with a typical value of approximately 1.0 µF) have an equivalent serial resistance (ESR) value of approximately 10 mΩ to 50 mΩ at a switching frequency of 380 kHz. From Equation 5 and the design specifications, I_{PRI} = 130 mA, V_{RIPPLE} = 50 mV, V_O = 12 V, and V_{IN_MIN} = 36 V, the output filter capacitance can be obtained as Equation 6:

$$C_{OUT} = \frac{\frac{V_O}{V_{IN\_MIN}} \times \frac{1}{f_{SW}}}{\frac{V_{RIPPLE}}{50\% \times I_{PRI}} - ESR} = \frac{\frac{12\ V}{36\ V} \times \frac{1}{380 \times 10^3\ Hz}}{\frac{0.05\ V}{50\% \times 0.13\ A} - 0.05\ \Omega} = 1.22\ \mu F \quad (6)$$

With some design margin and considering the voltage dependence of the ceramic capacitors, select capacitors rated at 4.7 µF with a voltage rating of 16 V, or 2.2 µF with a voltage rating of 25 V. As a good practice from experience, a high-frequency decoupling capacitor with a 0.1-µF typical value is still required for the devices to be biased. Refer to Figure 1 for additional capacitance based on the bench test to ensure the output voltage ripple meets the design specifications.

3.1.3 Determining the Input Filter Capacitance

The input filter capacitors are designed with an equation similar to the output capacitors, as shown in Equation 7:

$$C_{IN} = \frac{\Delta T}{\frac{\Delta V}{\Delta I} - ESR} = \frac{\frac{V_O}{V_{IN\_MIN}} \times \frac{1}{f_{SW}}}{\frac{5\% \times V_{IN\_MIN}}{50\% \times I_{PRI}} - ESR} = \frac{\frac{12\ V}{36\ V} \times \frac{1}{380 \times 10^3\ Hz}}{\frac{5\% \times 36\ V}{50\% \times 0.13\ A} - 0.05\ \Omega} = 0.032\ \mu F \quad (7)$$

After considering the device internal-circuit requirements, voltage dependence and some design margin, select a 1.0-µF multilayer ceramic capacitor (X5R or X7R) with a voltage rating of 100 V.

3.2 Programming the Device

3.2.1 Determining the Capacitors

There are five critical capacitors when programming the device: C1, C2, C5, C6, and C15.

C1 is the input capacitance. The UCC25230 data sheet specifies the minimum C1 value as 1.0 µF. If the resulting value of C1 from the *Determining the Input Filter Capacitance* section is greater than 1.0 µF, then use the greater value in the design. The voltage rating depends on the maximum input voltage. In typical 48-V telecom modular applications, a 100-V rating should be used.

C2 is the VDD decoupling capacitor and is 1.0 µF, based on the UCC25230 data sheet. Because the VDD typical value is 9 V, a voltage rating of 16 V or greater should be used.

C5 is the bootstrap capacitor and is 1.0 µF, based on the data sheet. The voltage rating for C5 is 16 V or greater, based on the voltage between the BOOT and PHASE pins, as specified in the data sheet.

C6 is a noise reduction capacitor with a value typically in the range of 0.1 µF to 1.0 µF. C6 also introduces turn-on delay. In most applications, this delay presents a desired feature that can allow for a settle-down input voltage transient.

C15 is also a noise reduction capacitor that helps eliminate VIN_G jitter. The C15 typical value range is 0.1 µF to 1.0 µF.

All of these capacitors should be of a multilayer, ceramic X7R or X5R type.

3.2.2 Determining the Resistors

The resistors used around the device are divided in two groups: control loop without feedback, and control loop with feedback.

3.2.2.1 Control Loop without Feedback Design

The resistors used in the control loop without feedback are R2 and R4 and set up the UV/OV pin. These resistors are used to determine the input voltage that makes VIN_G valid. The VIN_G signal notifies the system with the input voltage status when the input voltage reaches the preprogrammed threshold.

Because the threshold for UV on is 36 V of the input voltage and the VIN_G maximum turn-on threshold is 1.10 V (based on the data sheet), it can be assumed that R4 = 10 kΩ. Thus, R2 can be calculated as Equation 8:

$$R2 = R4 \times \frac{V_{IN} - V_{IN\_G}}{V_{IN\_G}} = 10\ k\Omega \times \frac{36\ V - 1.10\ V}{1.10\ V} = 317\ k\Omega \Rightarrow 316\ k\Omega \tag{8}$$

3.2.2.2 Control Loop with Feedback Design

The converter works in voltage mode control; therefore, it requires Type-III compensation to stabilize the feedback control loop. Type-II compensation can be used if the compromised performance allows. For Type-III compensation, a total of seven components are required, including the output voltage set-point resistors. For the Type-II compensation method, the total components required may be dropped to five. Because 0402 package components are typically used, the savings from cost and board space may not show a significant benefit and a concern of sacrificing performance may result. In this report, Type-III is used.

The compensation can be made in a simple way because the converter can be treated as a simple sync-buck converter. The main influence is the coupled inductor. On the primary side, the inductor presents with a parameter of inductance and an equivalent series resistance. The total output capacitance can be estimated by a summation of the total primary and secondary output filter capacitance. In this design, the total output capacitance is 20.8 µF. The output filter inductance at full load is typically 160 µH. After these values are known or approximated, the converter is actually equivalent to a sync-buck converter.

The K-factor method can be used to design the compensation parameters for the starting point. More details about the K-factor method can be found in reference 3 of the References section. The Bode plots of the modulator can be measured before the feedback loop design starts. This method is described in reference 4. The final values of each parameter are shown in Table 2.

Table 2. Design Value of Loop-Compensation Parameters

R1	R3	R6	R7	C3	C4	C7
20.5 kΩ	47.5 kΩ	178 kΩ	3.65 kΩ	1 nF	47 pF	270 pF

The output voltage set point is determined by R3 and R6 with the device internal reference at 2.5 V. To validate this, use Equation 9:

$$\mathrm{VOUT1} = \mathrm{VOUT2} = \frac{\mathrm{R3} + \mathrm{R6}}{\mathrm{R3}} \times V_{REF} = \frac{47.5\ \mathrm{k}\Omega + 178\ \mathrm{k}\Omega}{47.5\ \mathrm{k}\Omega} \times 2.5\ \mathrm{V} = 11.87\ \mathrm{V} \cong 12.0\ \mathrm{V} \tag{9}$$

4 Performance Test

In this section, performance is shown from critical test results. More performance test results can be found in the UCC25230EVM-754 user's guide.

4.1 Power-Conversion Efficiency

Efficiency can be determined with IOUT1 or IOUT2, as shown in Figure 2 and Figure 3, respectively.

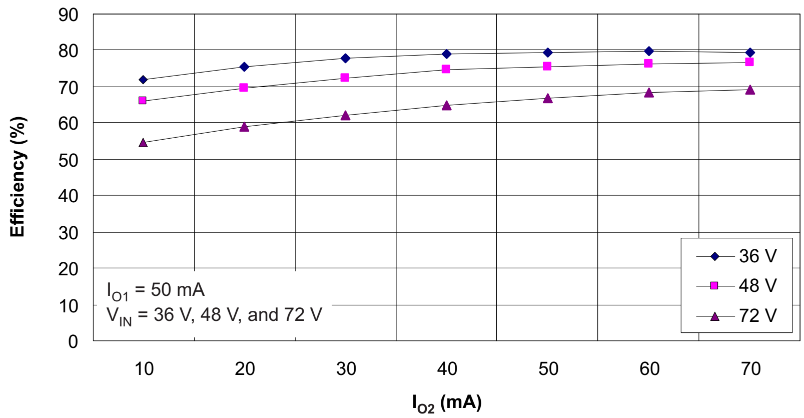

Figure 2. Efficiency with IOUT1 = 50 mA

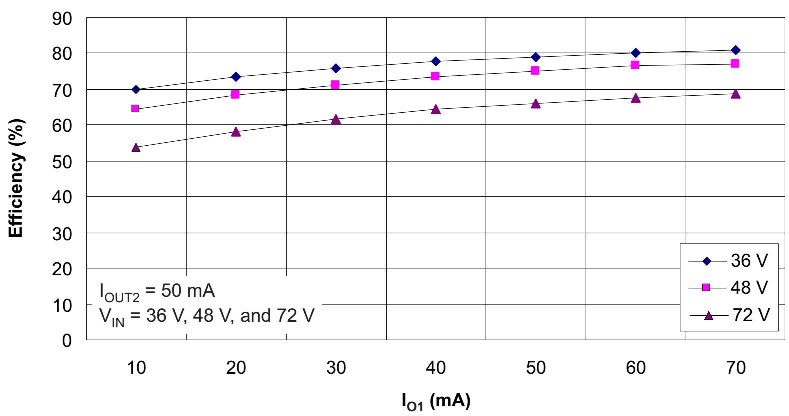

Figure 3. Efficiency with IOUT2 = 50 mA

4.2 Voltage Regulation

Voltage regulation can be determined with IOUT1 and IOUT2, as shown in Figure 4 and Figure 5, respectively.

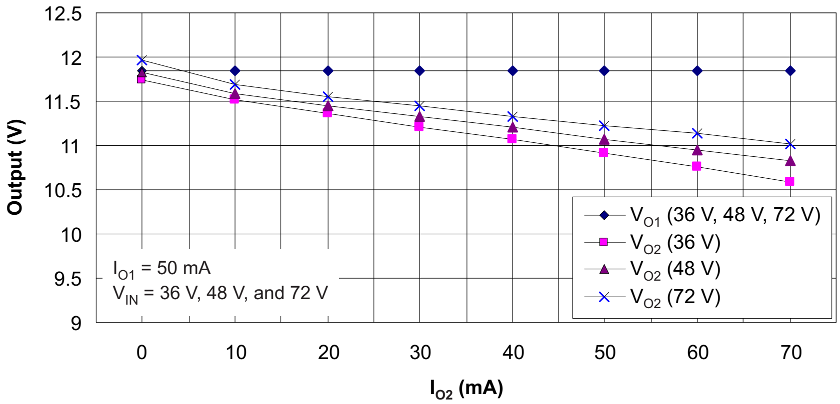

Figure 4. Regulation with IOUT1 = 50 mA

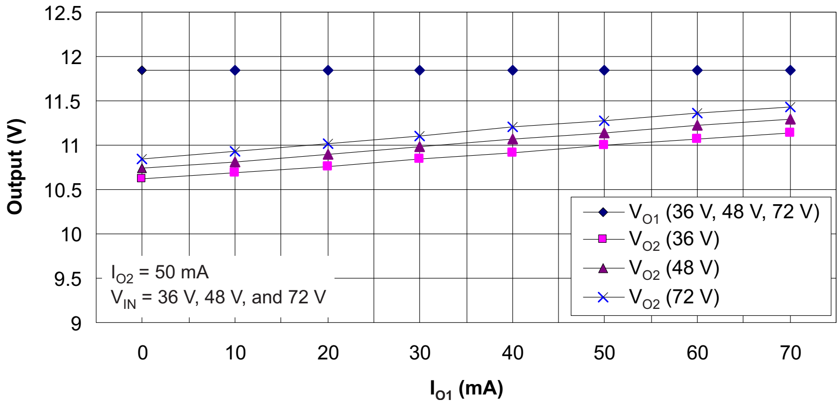

Figure 5. Regulation with IOUT2 = 50 mA

Table 3 lists the voltage regulation at corner conditions.

Table 3. Voltage Regulation at Corner Conditions

V_{IN} (V)	I_{O1} (mA)	I_{O2} (mA)	V_{O1} (V)	V_{O2} (V)
36	0	0	11.85	11.50
		65		9.70
	65	0	11.85	12.10
		65		10.50
72	0	0	11.85	11.75
		65		10.25
	100	0	11.85	12.30
		65		11.10

4.3 Feedback-Loop Compensation

Figure 6 shows the Bode plots at V_{IN} = 48 V and load = 50 mA of each output.

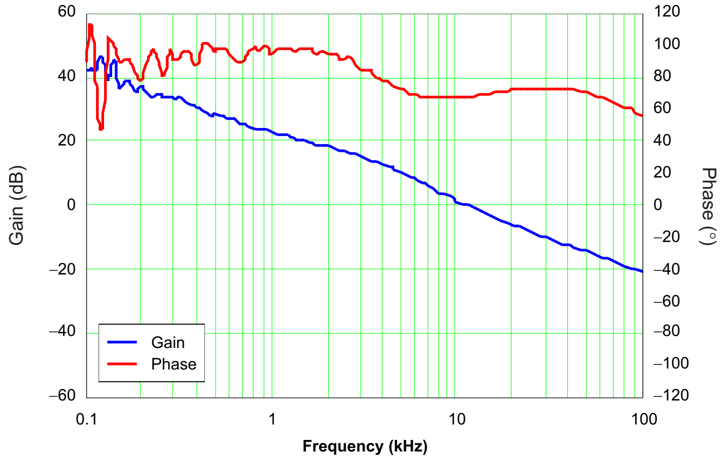

Figure 6. Gain and Phase vs Frequency

4.4 Design Performance Summary

Table 4 summarizes the design performance.

Table 4. Design Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Voltage range		36	48	72	V
Maximum input current	V_{IN} = 36 V and IOUT1 = IOUT2 = 65 mA		70		mA
No load input current			8.5		mA
OUTPUT CHARACTERISTICS					
Output voltage, VOUT1	IOUT1 = 0 mA, IOUT2 = 65 mA	11.5	11.8	12.5	V
	IOUT1 = 65 mA, IOUT2 = 0 mA	11.5	11.8	12.5	V
Output voltage, VOUT2	IOUT1 = 0 mA, IOUT2 = 100 mA	9.5	10.0	11.0	V
	IOUT1 = 100 mA, IOUT2 = 0 mA	9.5	12.0	12.5	V
Output load current, IOUT2 or IOUT2				65	mA
Output 1 voltage regulation (regulated output)	Line regulation: Input voltage = 36 V to 72 V IOUT1 = IOUT2 = 100 mA			10	mV
	Load regulation: Input voltage = 48 V IOUT1 = 0 mA to 100 mA, IOUT2 = 100 mA			10	mV
Output 2 voltage regulation (cross-regulated output)	Line regulation: Input voltage = 36 V to 72 V IOUT1 = IOUT2 = 65 mA			0.75	V
	Load regulation: Input voltage = 48 V IOUT1 = 65 mA, IOUT2 = 0 mA to 65 mA			–1.35	V
Output voltage ripple (outputs 1 and 2)	At IOUT1 = IOUT2 = 65 mA		45	60	mV_{PP}

Table 4. Design Performance Summary (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEMS CHARACTERISTICS					
Switching frequency			380		kHz
Peak efficiency	V_{IN} = 36 V, IOUT1 = IOUT2 = 50 mA		81		%
Full load efficiency	V_{IN} = 48 V, IOUT1 = IOUT2 = 65 mA		80		%
Input status good (TP4)		4.2		5.2	V
Effective bias real estate size	L × W × H		0.6 × 0.5 × 0.15		Inches
Board size	L × W		2.2 × 1.4		Inches
Operating temperature	Natural convection			4.5	°C

5 References

1. UCC25230 Data Sheet, SLUSAQ6A, 2011
2. UCC25230 Evaluation Module and User's Guide, SLUU670, 2011
3. George C. Chryssis, *High-Frequency Switching Power Supplies Theory and Design*, Second Edition, McGraw-Hill, 1989.
4. Hong Huang, Feedback Loop Design of an LLC Resonant Power Converter, Application Report, SLUA582A, 2010.

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