Application Report
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Using New Thermal Metrics

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ABSTRACT

Several TI power management ICs, such as the TPS742xx, TPS743xx, and TPS744xx series of linear regulators, have started using new thermal metrics in the respective product data sheets to describe the thermal characteristics of the device. The technical definitions of these metrics are clearly explained in a separate application report entitled *IC Package Thermal Metrics* (SPRA953).

This document discusses the practical usage of these new thermal metrics using an illustrated analogy of Ohm's law. Additionally, this application report explains why traditional thermal parameters are not recommended for determining the actual thermal performance of many linear power management devices.

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1 Quiz on Ohm's Law

For the straightforward discussion in the balance of this application note, first try to answer this quiz. These questions are simple, and will help the reader understand the analogy used in this report.

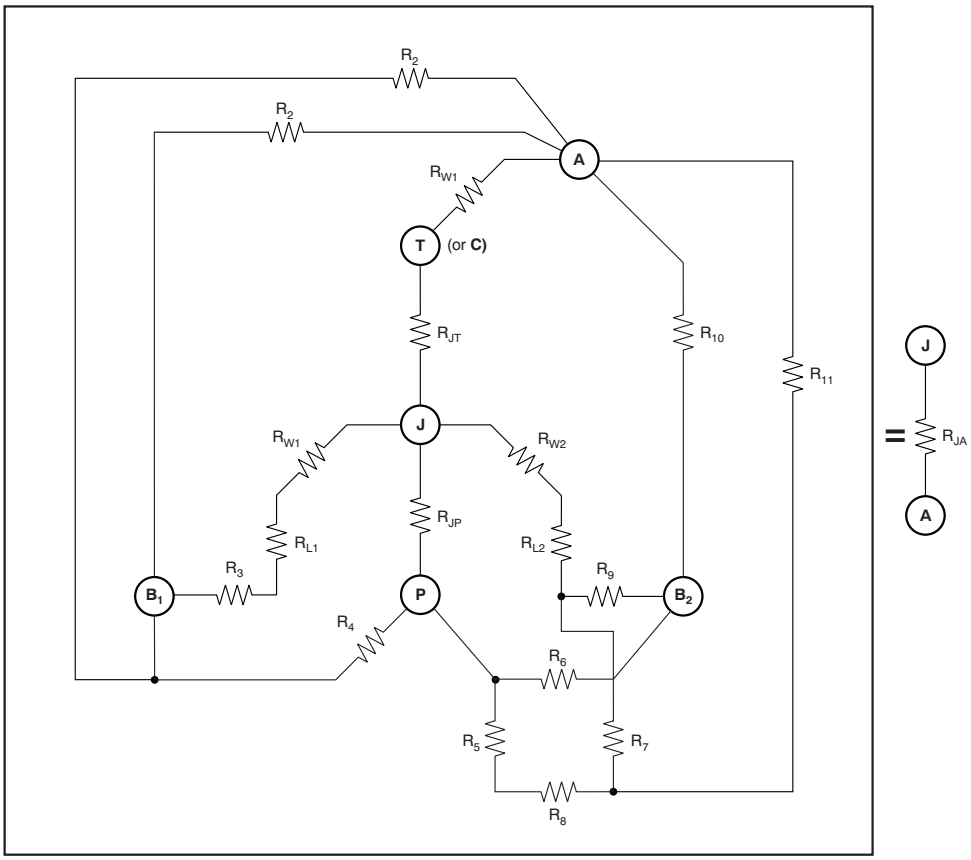

Figure 1. Example Resistor Network

1. Calculate the combined resistance of the resistor network shown in Figure 1. Given that R_{JT}, R_{JP}, R_{W1}, R_{W2}, R_{L1}, and R_{L2} are known, we assume the other resistor values are unknown.
   (a) Can we calculate R_{JA}, the combined resistance between node J and node A?
   (b) If yes, what is the expression of R_{JA} using R_{JT}, R_{JP}, R_{W1}, R_{W2}, R_{L1}, and R_{L2}? If no, why can we not obtain the value of R_{JA}?
2. Calculate voltage from a resistor network. In Figure 1, we assume that R_{JT} and V_{TA} are known and that the other resistor values are unknown. (V_{TA} represents the voltage between node T and node A.)
   (a) When a current source I_{JA} = p(A) is connected from node J to node A, can we calculate V_{JA}, the voltage between node J and node A?
   (b) If yes, what is the expression of V_{JA} using R_{JT}, p, and V_{TA}? If no, why we can we not obtain the V_{JA} value?
3. Calculate voltage from a resistor network. In Figure 1, we know that V_{JT} is X(V) when I_{JA} = Y(A). Assume that all resistance values are constant. (V_{JT} represents the voltage between node J and node T, and I_{JA} represents the current from node J to node A.)
   (a) Can we calculate V_{JT} when I_{JA} = Z(A)?
   (b) If yes, what is the expression of V_{JT} using X, Y, and Z? If no, why can we not obtain the V_{JT} value?
4. Calculate voltage from a resistor network. In Figure 1, we know that V_{JB} is α(V) when I_{JA} = β(V). Assume that all resistance values are constant. (V_{JB} is the voltage between node J and node B; I_{JA} is the current from node J to node A.)
   (a) Can we calculate V_{JB} when I_{JA} = γ(A)?
   (b) If yes, what is the expression of V_{JB} using α, β, and γ? If no, why can we not obtain the value of V_{JB}?

2 Purpose of Thermal Parameters/Metrics

2.1 Objective

The ideal target of thermal management in a new design is to ensure that every silicon device on the board works within its allowable operating junction temperature. More specifically, thermal management attempts to ensure that the IC works within the specifications of the operating maximum junction temperature, or T_J(max). Keep in mind that most IC devices define an *absolute maximum junction temperature* as well as an *operating maximum junction temperature*. Because the parameter *absolute maximum* temperature defines the thermal point at which the device is damaged, we must refer in this document to the *operating maximum* temperature, T_J, which defines the maximum allowable temperature for continuous normal operation of the device.

The greatest difficulty we face in order to achieve this target is that there is no direct way to measure T_J by using a thermocouple or infrared thermometer, because the IC is covered with a mold compound and the actual junction is not exposed. For many large package ICs, such as PC processors or PC graphics processors, there is a built-in function to measure T_J using integrated thermosensors, which in turn provide a read-out to an analog-to-digital (A/D) converter. For small package ICs, however—including most power ICs—there is no such T_J sensor function as a result of silicon size and package pin count limitations. Consequently, we must estimate T_J by thermal calculation and thermal evaluation.

2.2 A Practical Method to Estimate Junction Temperature

On every application board, it is a reasonable, fair, and valid assumption that we can measure several temperature points. The highlighted single letter in each row refers to parameters discussed later in this report.

Parameter	Definition/Measurement Point
T_C *or* T_T	Temperature of the IC device **c**ase, measured at the center **t**op of the IC package ***C*** *ase* is used in old-fashioned, early-generation ICs such as that shown in Figure 2 ***T*** *op* is used for modern surface-mount devices (SMDs).
T_B	Temperature of the **b**oard measured at a point of the board surface close to where the IC is mounted
T_P	Temperature of the IC package thermal **p**ad if it is exposed
T_A	**A**mbient (room) temperature

Our target is to estimate T_J by calculations that use these measurable values. Moreover, we need thermal parameters or metrics to perform those calculations.

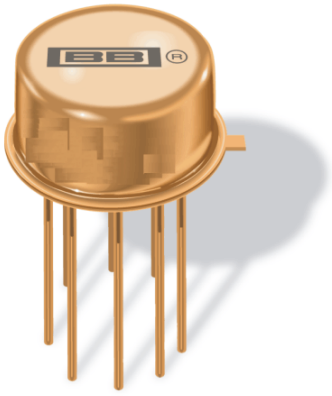

Figure 2. Older IC Package with Case

2.3 Why Not θ_{JC} or θ_{JA}?

By answering each question presented in Section 1, we can explain why TI recommends that designers not use θ_{JC} or θ_{JA}. This section also explains why TI advises designers to use the set of new thermal metrics, Ψ_{JB} and Ψ_{JT}.

2.3.1 Analogy of Electrical and Thermal Resistance

Figure 3 is an example of a detailed thermal resistance network formed by an IC device mounted on a printed circuit board (PCB). Note that Figure 3 is equivalent to Figure 1. However, in Figure 3, resistance values are expressed with lumped parameters, but the physical IC and the PCB material form a distributed parameter network.

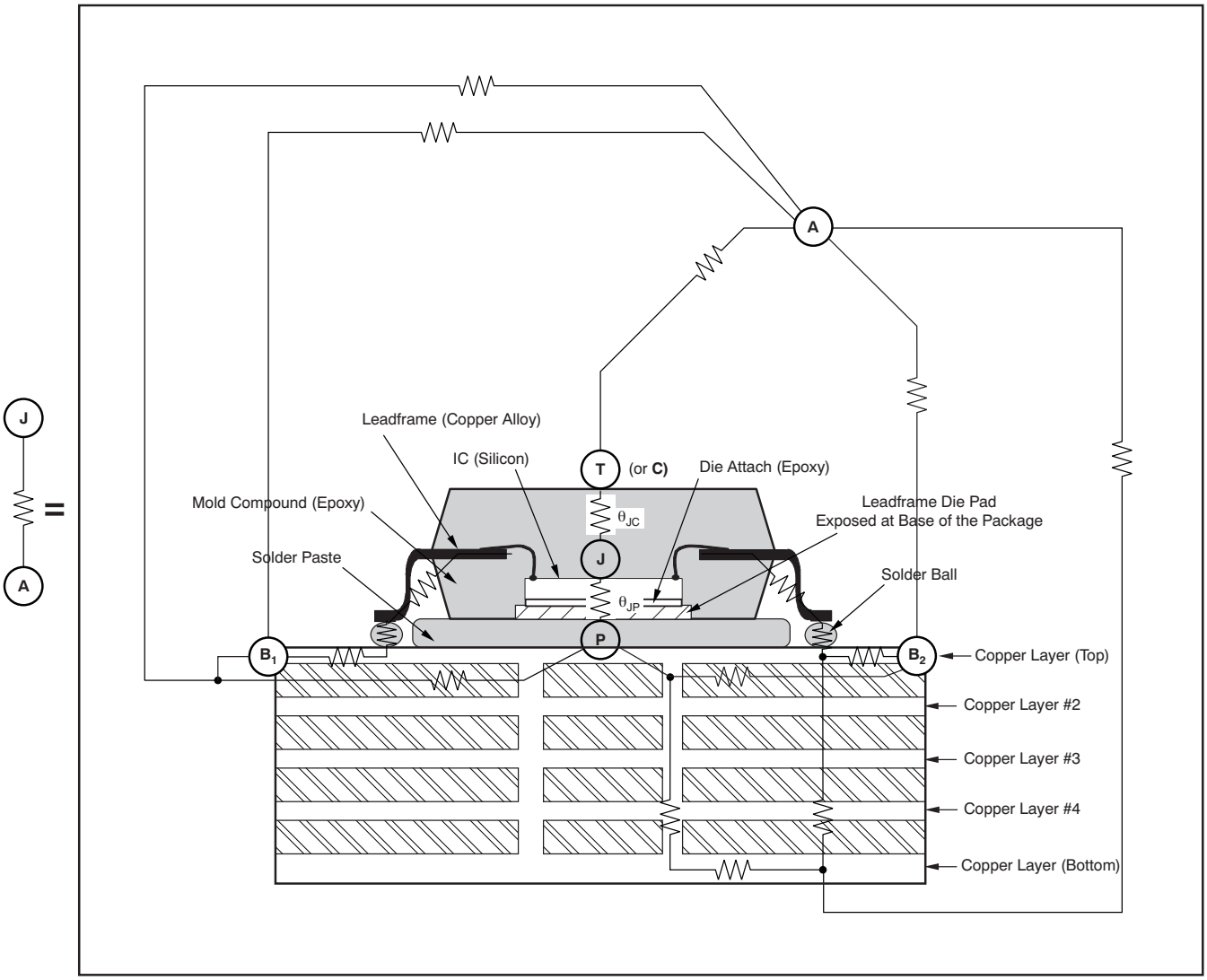

Figure 3. Thermal Resistance Network Example

In the world of electronics and electrical design, resistance value is defined by Ohm's law:

$$R(\Omega) = \frac{E\ (V)}{I\ (A)} \quad (1)$$

The electrical resistance shows a ratio of how much electrical potential difference is caused by (electron) current flow.

In the thermal world, though, resistance is defined by this equation:

$$R_{\theta}\ (°C/W) = \frac{\text{Temperature } (°C)}{\text{Power } (W)} \quad (2)$$

Thermal resistance shows a ratio of how much temperature difference is caused by power (heat) flow.

2.4 Quiz Answers

Now let us consider the answers to the quiz given in Section 1.

2.4.1 Question #1

Answer: **No**

We have too little information to calculate the combination resistance.

To calculate a combination resistance, we need to know all resistor values.

Comparing Figure 1 and Figure 3, R_{JT}, R_{JP}, R_{W1}, R_{W2}, R_{L1}, and R_{L2} are all lumped parameter resistances within the IC. This question shows us that in the thermal world, θ_{JA} cannot be determined only by the IC. It depends greatly on the application board. Every different PCB has a different θ_{JA} value. The primary concern to most IC designers is what happens on their own application boards, so using θ_{JA} is not recommended.

θ_{JA} on virtually all IC device data sheets are generally example values measured or calculated with industrial standard boards. These industrial standard platforms are called *JEDEC High-K* or *JEDEC Low-K* boards. Furthermore, these JEDEC boards (consisting of only one IC device mounted in large, 3-inch by 3-inch area) are significantly different from real-world application PCBs. See Figure 4 for an example of standard industrial boards to be used for θ_{JA} measurements. For 99% of board designers, this situation of only one IC device on a 3-inch × 3-inch board area is not acceptable. The only benefit, then, to using θ_{JA} is to compare the thermal performance of different device packages.

NOTE: It is better to know another aspect of this type of comparison: IC makers use very limited number of IC assembly vendors. Even though some IC makers do in-house assembly, the most common materials used for IC packaging are supplied by a further limited number of material vendors. As long as the package size and dimensions are the same, the thermal performance of two ICs should be very similar.

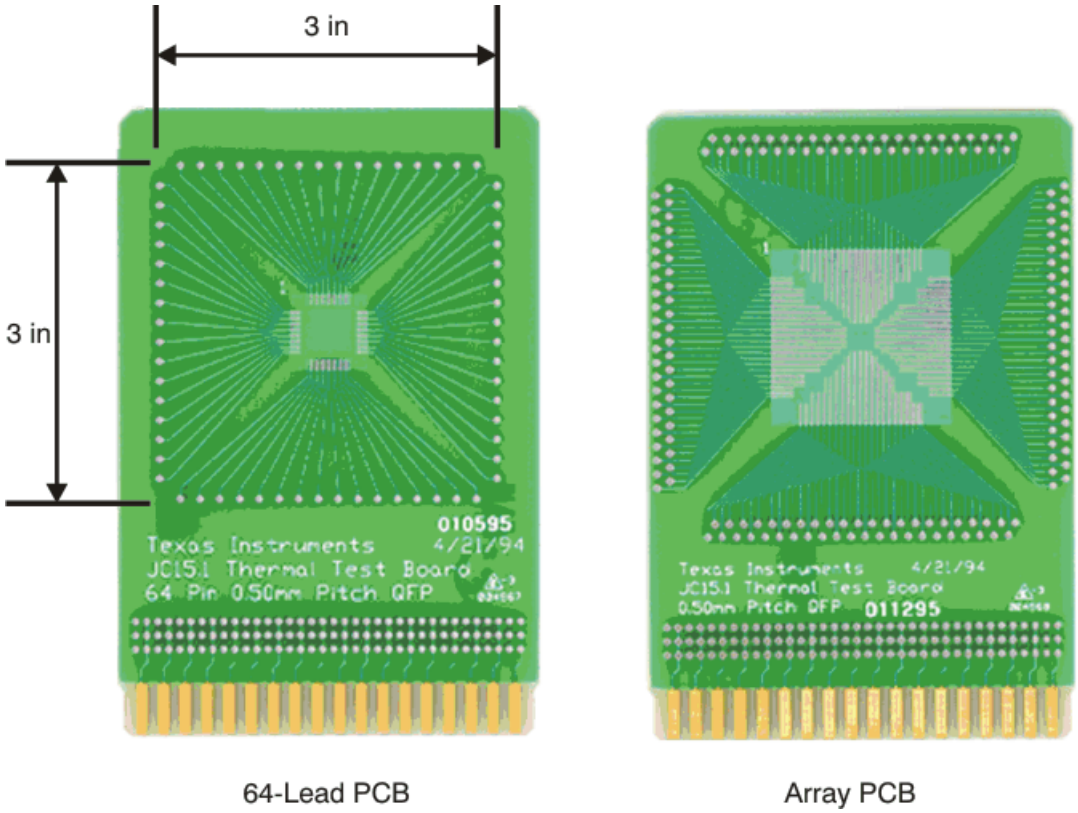

Figure 4. θ_{JA} Measurement PCB Example

2.4.2 Question #2

Answer: **No**

Again, we have too little information, in this case to solve a matrix of Kirchhoff's circuit law.

To calculate the target voltage, we need to know all other resistor values because the current I_{JA} is going through every possible path. In this question, the availability of R_{JA} is intentionally excluded because the answer for the first question shows that a typical R_{JA} value does not necessarily represent a real-world application board for most IC device designers. Additionally, using R_{JA} very quickly gives us a false answer:

$$V_{JA} = R_{JA} \times I_{JA}$$

Let's turn to the thermal world.

In the earlier days of IC devices, using an IC package such as Figure 2 shows, it was a good assumption that the majority of power (heat) dissipated from the surface between the IC case and ambient air. This assumption was based on the fact that the IC package was almost always isolated from the PCB; in another words, the IC was in effect floating on the PCB. In terms of typical measurement, then, R_{JC} is extremely small compared to the other resistance values, and the majority of heat flows through R_{JC} (this practical result is actually the definition of θ_{JC} in the JEDEC standard). When R_{JC} is very small and the other resistors can be ignored, the following formula becomes valid:

$$R_{JA} \approx R_{JC} + R_{CA}$$

This equation illustrates that using θ_{JA} and θ_{JC} could solve most thermal calculations in those days; a backwards-compatibility to this historical perspective is probably the only reason IC makers continue to use θ_{JA} and θ_{JC}.

In contemporary IC manufacturing, SMDs dissipate the majority of heat to the board. It should be evident from this question that θ_{JC} does not give any meaningful information about T_J.

2.4.3 Question #3

Answer: **Yes**

We expect linearity, V_{JT} to be given in this manner:

$$V_{JT} = \frac{X}{Y} \bullet Z \tag{3}$$

In our thermal discussion, this question shows an opportunity to easily estimate T_J; the only step required is to figure out a constant:

$$\Psi_{JT} = \frac{X}{Y}$$

These days, we have very good thermal simulators to calculate this constant, Ψ_{JT}; finding the value is not an issue. The relevant point here is the dependency of this constant to the PCB as with our discussion in the previous answer to question #2. In contrast, the fact that SMDs dissipate the majority of heat to the PCB helps the situation. When most of the device heat goes into the board, there is a very low heat flow through θ_{JT}, so the temperature difference between T_J and T_T should be very small. That slight difference means that the value of the constant Ψ_{JT} should be very small. If it is small, then any error caused by board variation is small, too.

This constant represents one of the new thermal metrics, Ψ_{JT}.

By knowing T_T, we can estimate T_J using Equation 4, where P_D is the power loss at a silicon junction.

$$T_J = T_T + \Psi_{JT} \bullet P_D \tag{4}$$

2.4.4 Question #4

Answer: **Yes**

We expect linearity, V_{JB}, to be given in this manner:

$$V_{JB} = \frac{\alpha}{\beta} \bullet \gamma \tag{5}$$

Comparing the answers to questions 3 and 4, we can have a very similar discussion.

The difference between these answers is a discussion of the error caused by board variation. A path from the junction to the board consists of all metal: silicon and aluminum comprise the IC routing layer; the bonding wire is often gold; the IC lead consists of copper, as does the solder paste; and the PCB pattern also contains metal. Therefore, the combined thermal resistance from junction-to-board is very small. As a result, again, if this thermal resistance is small, the error is small, as well.

This result also generates the other new thermal metric, Ψ_{JB}.

By knowing T_B, we can estimate T_J with Equation 6, where P_D is the power loss at a silicon junction.

$$T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

3 Calculation Example with TPS742xx, TPS743xx, and TPS744xx

In the current revisions of the product data sheets for the TPS742xx, TPS743xx, and TPS744xx series of low-dropout linear regulators, TI introduces Ψ_{JT} and Ψ_{JB}. Consider the TPS74401KTW as we look at an illustration of how to use these new thermal metrics.

Step 1. Calculate Ψ_{JT} and Ψ_{JB} from a graph.

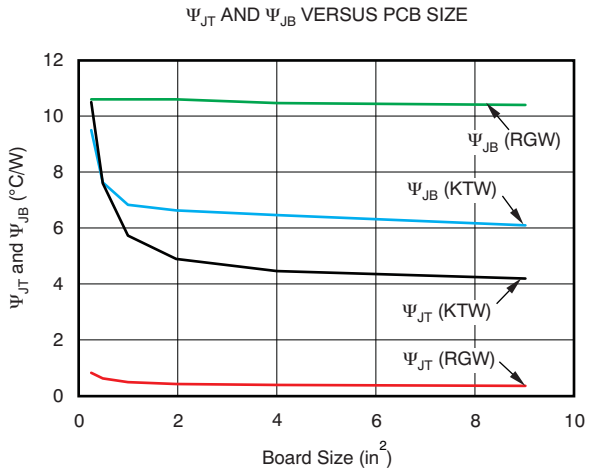

Figure 5. Ψ_{JT} and Ψ_{JB} vs PCB Size

By looking at Figure 5 from the TPS744xx data sheet, we can identify proper Ψ_{JT} and Ψ_{JB} values depending on the target application board size. The board size to be used here is the area of the PCB assigned only for the TPS74401 IC device. This area can include passive components as long as those components are not a heat source, but any other IC devices are not included.

In this example, assume the board size is 2-in^2. Select Ψ_{JT} = 4.5°C/W and Ψ_{JB} = 6.3°C/W.

Step 2. Calculate P_D.

Calculate the power dissipation using Equation 7.

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT} \quad (7)$$

In this example, assuming V_{IN} = 1.5 V, V_{OUT} = 1.2 V, and I_{OUT} = 2.7 A, we get a power dissipation of P_D = 0.81 W.

Step 3. Measure T_T, T_B, and T_A.

Measure T_T and T_B by using a thermo-gun (that is, an infrared thermometer), and measure T_A with a normal thermometer.

In this example, assume that T_T = +76°C, T_B = +74°C, and T_A = +30°C.

Figure 6 and Figure 7 show actual IC images to better illustrate where to measure the values that correspond to Figure 36 of the TPS744xx product data sheet.

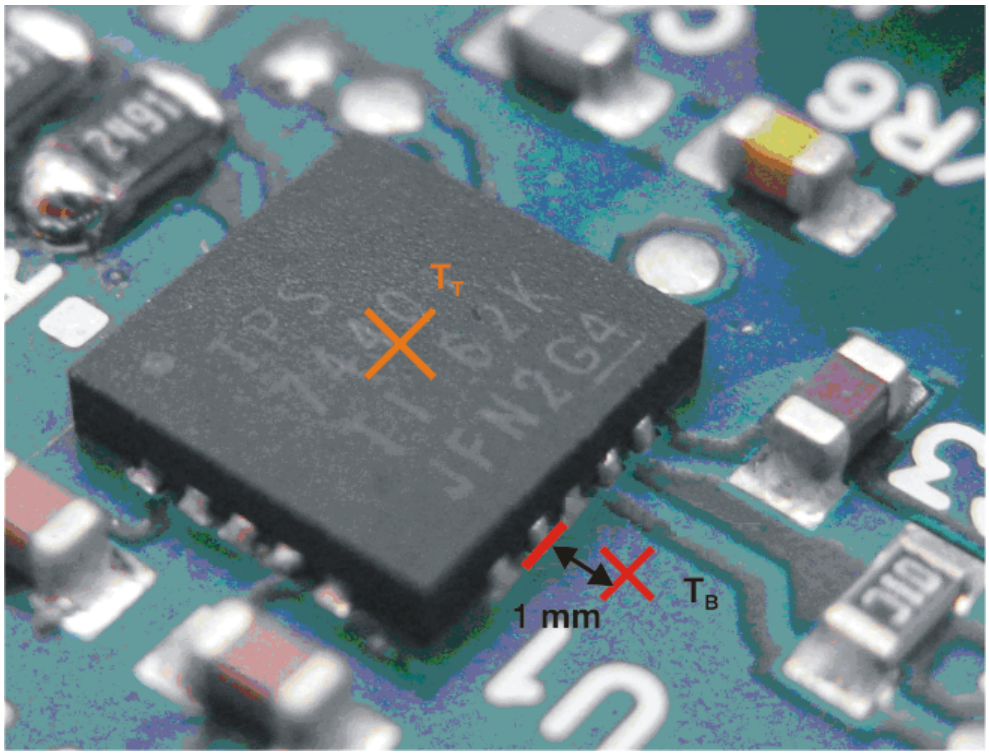

Figure 6. RGW (QFN) Package T_T and T_B Measurement Locations

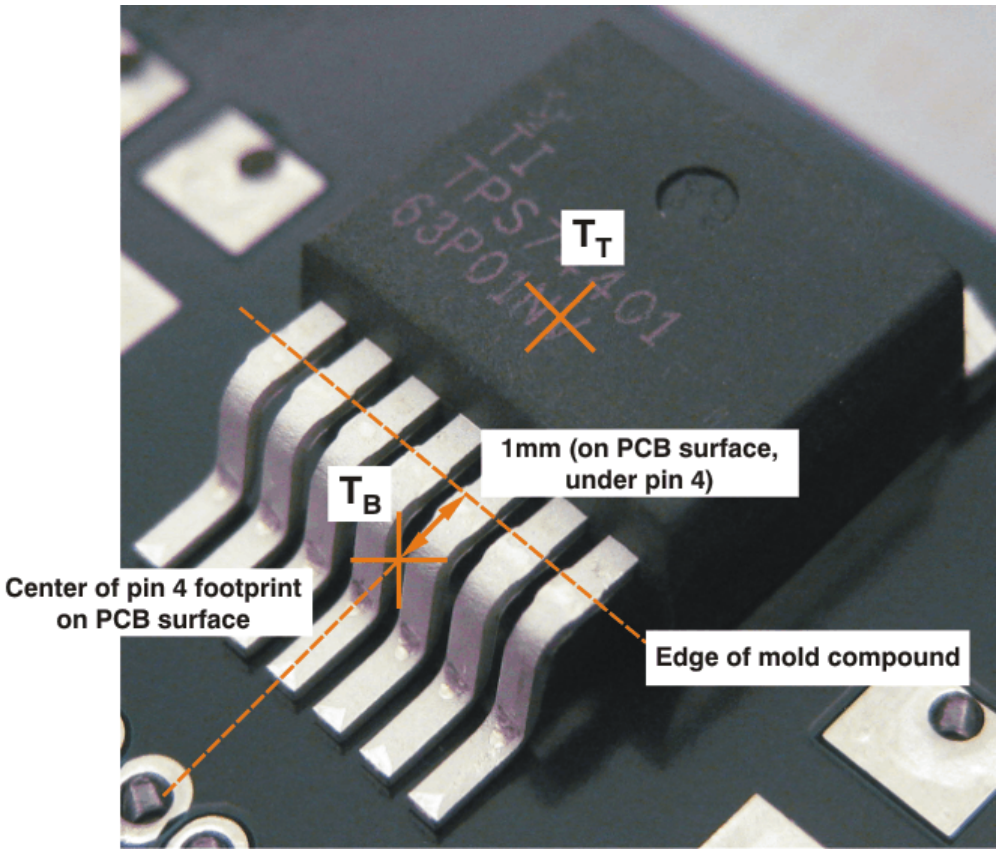

Figure 7. KTW (DDPAK) Package T_T and T_B Measurement Locations

Step 4. Estimate T_J.

Now apply Step 3 to Equation 1 and Equation 2.

In this example, two T_J estimations can be said to be close enough.

$$T_J = T_T + \Psi_{JT} \bullet P_D = 76 + 4.5 \bullet 0.81 = 79.6°C \quad (8)$$

$$T_J = T_B + \Psi_{JB} \bullet P_D = 74 + 6.3 \bullet 0.81 = 79.1°C \quad (9)$$

Step 5. Validate the estimated T_J value.

Compare the results from Equation 8 and Equation 9. The T_J temperature estimates from these two equations should be very close. If these estimated values are close, we can accept that we have a reasonable T_J value; if these estimates are not aligned, however, we must check for something that could cause an error.

3.1 Key Points of This Example Study

We can summarize our discussion with these conclusions:

- T_T, T_B, and T_J are generally very similar values because of very low Ψ_{JT} and Ψ_{JB}.
- Ψ_{JT} and Ψ_{JB} are completely independent of board size compared to θ_{JA}, as Figure 8 (from the TPS744xx data sheet) shows.

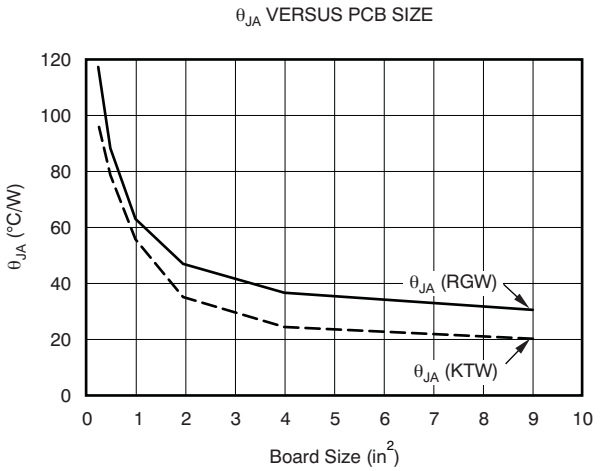

Figure 8. θ_{JA} vs PCB Size

These two points state that measuring T_T and T_B produces a very close and stable estimate of T_J.

4 Appendix

Regarding θ_{JA} and θ_{JC}, closing the gap between an old package (see Figure 2) and a recent SMD device, TI used another thermal parameter, θ_{JP}, in the place of θ_{JC}. Thus, when you see a narrow θ_{JC} range of 1°C/W to 6°C/W on TI data sheets, it is θ_{JP}. Usually, θ_{JC} is greater than 15°C/W.

TI is in the process of revising the practice concerning this point to correct confusion by using Ψ_{JT} and Ψ_{JB}.

Recently, JEDEC has defined the terms θ_{JC},*top* and θ_{JC},*bottom*. The TI term θ_{JP} is now defined as equivalent to θ_{JC},*bottom* to align with industry standards. This report does not use these new JEDEC terms; instead, we continue to use θ_{JP}. This new definition is one reason why TI has mixed θ_{JC} and θ_{JP} in some product data sheets; experienced engineers correctly interpret θ_{JC} as θ_{JC}, *op*, but they also know that θ_{JP} (officially, θ_{JC},*bottom*) will give us a more reasonable meaning as this document explains.

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