# External PNP Transistor Boosts TPS71501 Output Current

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**ABSTRACT**

Using an external PNP transistor together with a low-dropout regulator (LDO), such as the TPS71501, supplies a load current of 1A with an output of 9V.

Some applications require an output current capability greater than what is available in the standard low-dropout regulator (LDO) product line. An example of such an application would be a circuit requiring a 9V output capable of supplying 1A from an input voltage range of 10.5V to 12V. Finding a regulator to meet these requirements presents several difficulties. While most general-purpose linear regulators can handle the input voltage range, the dropout specification is difficult to meet. Other low-dropout solutions may have a limited input or output voltage range that restricts their use in such applications. By using an external PNP transistor, some regulators can be adapted to meet these input and output voltage range requirements. For example, although the TPS71501 output current is only 50mA, using an external PNP transistor increases the output current capability to 1A, as shown in Figure 1.

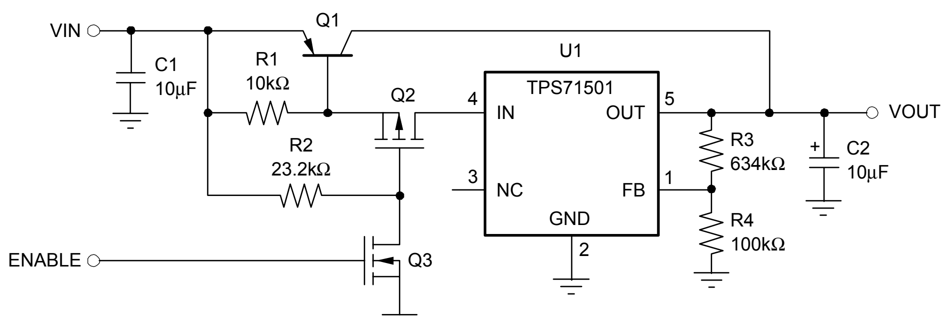


**Figure 1. Output Current Boost and Enable Circuit for the TPS71501**

In Figure 1, resistors R3 and R4 set the output voltage just as in a non-current-boosted design. Resistor R1 and transistor Q1 increase the output current capability. Resistor R2, together with transistors Q2 and Q3, implements an output enable/disable feature. C2 should be a tantalum capacitor; a ceramic capacitor may also be used, as long as a series resistor is added to achieve a similar series resistance (ESR). The circuit in Figure 1 is not suited for output voltages below 9V due to poor transient response and stability concerns.

The base current of Q1 (as well as the current to generate the $V_{BE}$ voltage across R1) must go through the TPS71501 to the output. The total dropout voltage of the design is calculated by adding the $V_{BE}$ voltage of transistor Q1 to the dropout voltage of the TPS71501. Note that the dropout voltage of the LDO in the circuit depends on the current flowing through the IC, not on the total output current delivered to the load. For this design, the output current of the TPS71501 is shown in Equation (1):

$$I_{LDO} = \frac{V_{BE}}{R1} + \frac{I_{LOAD}}{\beta + 1} \tag{1}$$

To minimize the dropout voltage, the current flowing through the LDO regulator should be as small as possible. Equation (1) shows that increasing the value of R1 and choosing a high beta transistor for Q1 can reduce the LDO current, thus decreasing the dropout voltage. Since the $V_{BE}$ voltage of Q1 is approximately 0.7V, increasing R1 above 10kΩ does little to reduce the regulator current. The most important parameter for reducing current through the TPS71501 is the beta of transistor Q1. Since beta is dependent on the $V_{CE}$ of Q1, the selected transistor should have a low saturation voltage with high beta at the desired dropout voltage. The Zetex ZXT2M322 transistor provides good performance in a small package, making it ideal for this scenario. If a different transistor for Q1 is used in the design, the output stability should be re-evaluated over the entire load range.

Once the current through the LDO is known, the designer can calculate the dropout of the LDO. The TPS71501 has a maximum specified dropout voltage of 750mV at 50mA. Since the I/V characteristic in dropout is linear, an equivalent on-resistance of the pass device can be calculated by dividing the rated dropout voltage by the specified output current. This resistance is approximately 15Ω for the TPS71501. The dropout at a lower current can be determined by multiplying the output current by the 15Ω on-resistance of the pass device.

Assuming the voltage across Q2 is negligible, the dropout voltage of the complete design can be calculated by adding the dropout of the TPS71501 with the $V_{BE}$ voltage for Q1. The $V_{BE}$ voltages for transistors are usually around 0.7V. However, this voltage has a temperature coefficient of -2.2mV/°C, so at cold temperatures the $V_{BE}$ voltage increases. The required $V_{BE}$-on voltage also increases with load current. When selecting Q1 for lowest dropout, the characterization curve in the transistor data sheet showing the $V_{BE}$-on voltage versus collector current should be examined to select the transistor with the lowest $V_{BE}$ voltage at the desired load current.

Since many applications require the ability to enable and disable the LDO output, transistors Q2 and Q3 were added to the design. When the enable signal shown in Figure 1 is low, transistor Q3 is off and the Q2 gate is pulled high. This turns off Q2, which greatly reduces the quiescent current and disables the LDO output. When the enable signal is high, the Q2 gate is pulled low, which turns on transistor Q2. If an open drain output is available, transistor Q3 may be omitted. The enable circuit increases the quiescent current while operating, depending on the input voltage and the value of R2. However, with the enable circuit omitted, the quiescent current of the 1A solution shown in Figure 1 is only 17.2 µA typically.

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